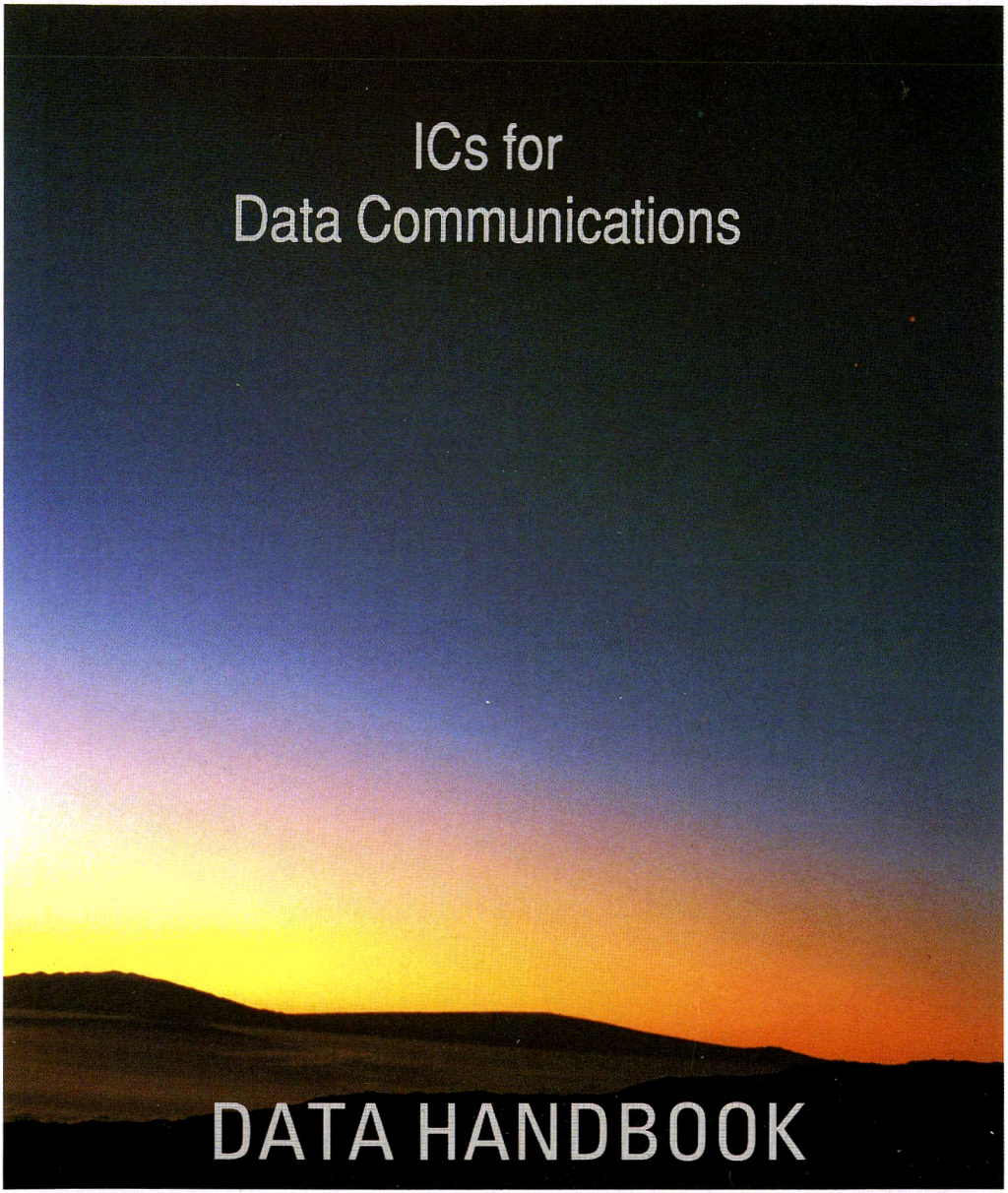
INTEGRATED CIRCUITS



BOOK IC 1991 2

Philips Semiconductors

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QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programs; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility toward the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical,' 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

ICs for Data Communications

Philips Semiconductors

PHILIPS

Signetics reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Signetics assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified. Applications that are described herein for any of these products are for illustrative purposes only. Signetics makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

LIFE SUPPORT APPLICATIONS

Signetics Products are not designed for use in life support appliances, devices, or systems where malfunction of a Signetics Product can reasonably be expected to result in a personal injury. Signetics customers using or selling Signetics' Products for use in such applications do so at their own risk and agree to fully indemnify Signetics for any damages resulting from such improper use or sale.

Signetics registers eligible circuits under
the Semiconductor Chip Protection Act.

Preface

Data Communications is one of the fastest growing markets in electronics and one in which Philips Semiconductors-Signetics has had a leadership position for many years. Our industry standard UARTs are complemented with the advanced architecture of the Dual Universal Serial Communications Controller (DUSCC) products and, more recently, by the innovative I/O Processor family. Taking advantage of an advanced CMOS technology, this entire product line represents the most comprehensive in the industry and it continues to grow.

In addition to the product focus, Philips Semiconductors-Signetics continues its committment to the highest levels of quality to insure our customers of cost effective ownership and world class reliability. In addition to the Digital Data Communication product family, Philips Semiconductors-Signetics offers a very extensive portfolio of semiconductor products, the details of which can be obtained from your local sales office.

Product Status

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	**Formative or in Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data, and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

Contents

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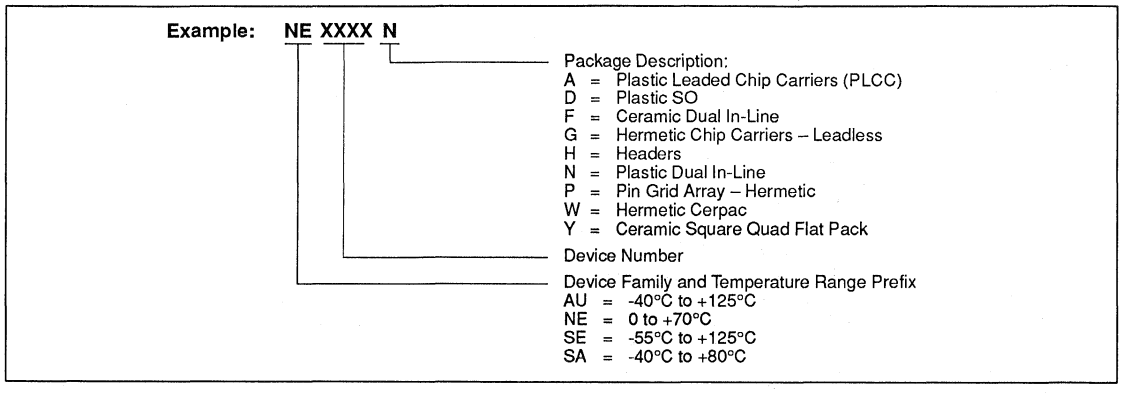
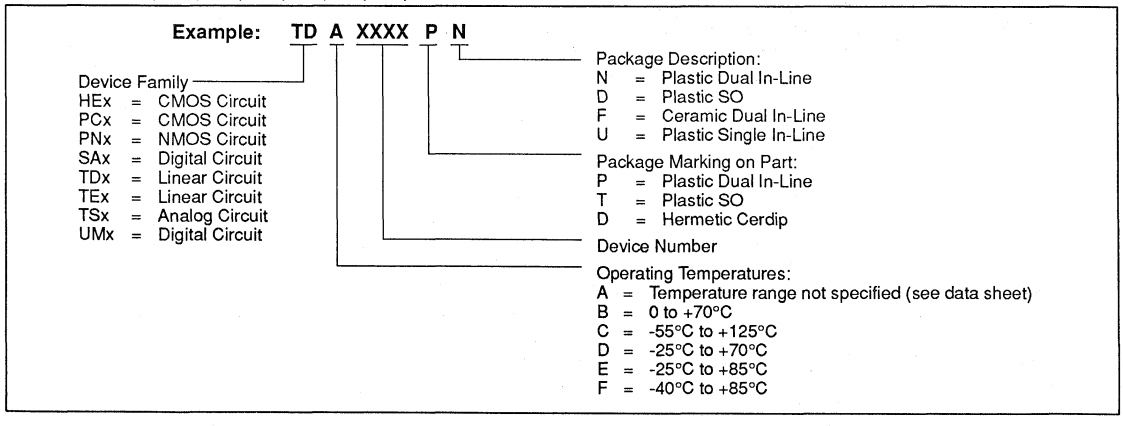
Alphanumeric Product List

Ordering Information

LINEAR PRODUCTS PART NUMBERING SYSTEM



PHILIPS PRODUCTS PART NUMBERING SYSTEM
PREFIXES HE, PC, PN, SA, TD, TE, TS, UM



Section 1
Quality and Reliability

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Quality and reliability

SUMMARY

The Signetics Company was founded in September, 1961 by a group of scientists and engineers who were among the pioneers in the development of integrated circuits. Signetics, acquired by Philips in 1975, was the first company in the world to be established for the sole purpose of designing, developing, manufacturing, and marketing ICs. Philips celebrated its 100th anniversary in 1991. On 1st January 1991, the Integrated Circuits and Discrete Semiconductor Business Units, formerly part of Philips Components, were merged into an autonomous product division (PD)—Philips Semiconductors as part of a major reorganization to focus Philips' semiconductor activities and to strengthen its standing in selected strategic markets. At the heart of this reorganization comes quality.

The Signetics approach to Quality Management has evolved with each evolution building upon the foundation laid. The emphasis in the 1960s and 1970s was quality by policy, documentation, and inspection. The emphasis in the 1980s was quality by employee involvement and process control. In the 1990s quality is achieved by emphasizing process and product Design For Manufacturability (DFM) and to customer requirements. (See Figure 1.) To ensure transformation, a formal Design Development Process (DDP) exists which requires the utilization of Cross-Functional Teams (CFTs) to assure that the customer Dimensions of Performance are met.

The modern Signetics Quality Journey (see Table 1) began in 1980. During the ensuing decade it achieved a 90-fold improvement in product electrical quality, 30-fold improvement in product visual and mechanical quality and a 20-fold improvement in product reliability. The great reduction in defect levels and a continued commitment to our customers made possible the following industry firsts:

- Ship-To-Stock Program
- Self-Qualification Program
- Zero Defects Warranty Policy

The Journey never ends—Signetics continues to strive for **EXCELLENCE** in all aspects of our business through company focus and initiatives aimed at achieving three performance level goals in 1994:

- Industry Leader in Customer Satisfaction
- With Products of Six Sigma Quality and Reliability
- And World Class Responsiveness to Customer Needs and Wants.

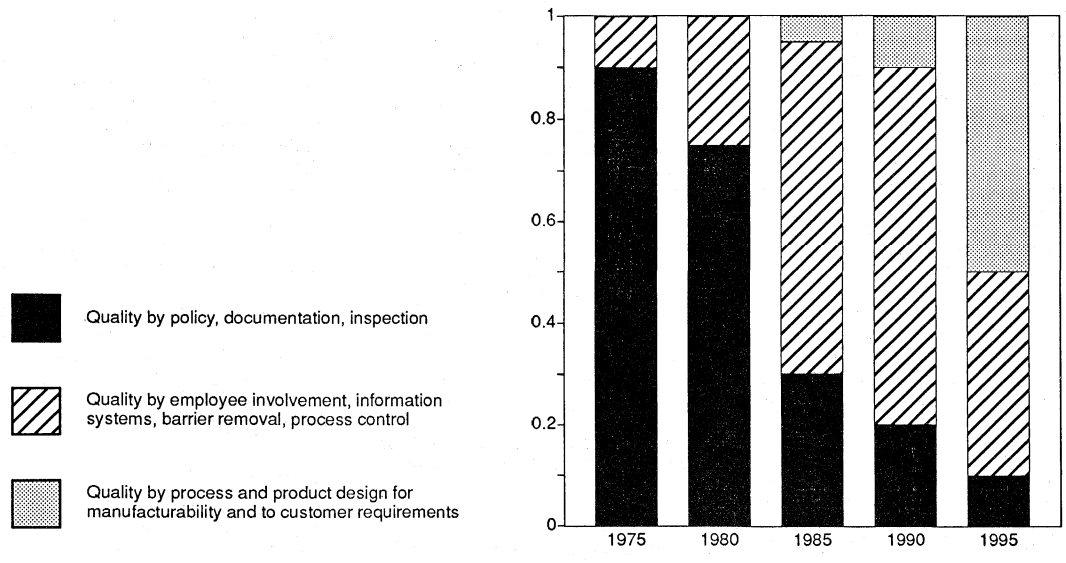


Figure 1. Evolution of Signetics Quality Management

Quality and reliability

SIGNETICS' QUALITY IMPROVEMENT PROCESS

In 1979, Signetics recognized that quality was becoming a major competitive issue, not only in the semiconductor business but also in other industries. Increases in the volume of products imported from the Far East (steel, automobiles, and consumer products) sent strong signals that new competitive forces were at work.

An investigation into a variety of quality programs was started. The company realized that quality improvement would require a contribution from all employees. Management commitment and participation, however, was recognized as the primary prerequisite for this program to work successfully. Resources required for the resolution of defects were under management control.

The "Signetics Quality Journey" from 1980 into the decade of the '90s is summarized in Table 1. In 1980 a program was developed which focused on quality management. Rearranging previous quality control philosophies, we developed a decentralized, distributed quality organization and simultaneously installed a Quality Improvement Process (QIP) based on the 14-Step improvement program advocated by Phil Crosby. The process was formally begun company-wide in 1981. Since then substantial progress has been made in every aspect of our operations. From incoming raw material conformance to improvements in clerical errors — every department and individual is involved and striving for Zero Defects. Zero Accept sampling plans and Zero Defects warranties are evidence of our ongoing commitment to and progress in quality. The Crosby 14 steps evolved into 9 elements as the foundation of the QIP. The QIP continued to expand, including more processes and disciplines as Signetics' vision cleared.

Today the Total Quality Management (TQM) model is applied to the QIP, as illustrated in Figure 2, having a far-reaching impact on all aspects of our business. The customer is at the start (driver) and end (goal) of the TQM model which requires a driver, system, measures and goal. The customer is the primary driver. Leadership is provided by Quality Improvement Teams (QITs) which ensure that customer interaction occurs and that the organization supports the mission, QI policy and customer direction. TQM requires a clear set of management principles which mandate systems and measurements consistent with stated objectives. TQM endorses and utilizes the seven major examination categories of the U.S.A. Malcolm Baldrige National Quality Award. Together, the examination categories address all major components of an integrated, prevention based system built around continuous improvement and customer satisfaction.

ZERO DEFECTS WARRANTY

In the '80s, American industry demanded increased product quality of its IC suppliers in order to meet growing international competitive pressure. As a result of this quality focus, it became clear that what once was thought to be unattainable— Zero Defects— is, in fact, achievable.

Signetics offers a Zero Defects Warranty which states that we will take back an entire lot if a single defective part is found. This precedent setting warranty implemented in 1985 effectively ended the IC industry's "war of the AQLs" (Acceptable Quality Levels). The ongoing efforts of IC suppliers to reduce PPM (Parts Per Million) defect levels is now a competitive customer service measure. This intense commitment to quality provides an advantage to today's electronics OEM. That advantage can be summed up in four words: ***Reduced Cost of Ownership.***

As IC customers look beyond purchase price to the total cost of doing business with a supplier, it is apparent that a quality-conscious supplier represents a viable cost reduction resource. Consistent high-quality circuits reduce requirements for expensive test equipment and personnel, and allow for smaller inventories, less rework, and fewer field failures. Programs such as Self Qualification and Ship-To-Stock implemented in 1984 and Cycle Time Management (CTM) implemented in 1989 help reduce cost of ownership.

STATISTICAL PROCESS CONTROL (SPC)

Although application of statistics in our process development and manufacturing activities goes back to the early 1970's, the corporate-wide emphasis on Statistical Process Control (SPC) did not come until mid-1984.

A natural evolution of our quality improvement process made introduction of SPC and other related programs an inevitable event. SPC was, therefore, introduced under the QIP umbrella. The Crosby definition of Quality, "Conformance To Requirements (Specification)" was expanded to include "Conformance To Specified Targets". The measurement definition of "continuous improvement" was expanded to include "Continuous Reduction of Variability Around the Specified Target".

The objective of SPC is to institutionalize a systematic and scientific approach to business and manufacturing activities. This approach utilizes sound statistical theory. Managers are expected to be able to turn data into information and to make decisions solely on data (not perception).

The most critical and challenging aspect of implementing SPC is the establishment of a discipline within the operating areas so that decision making is fundamentally based on verifiable data and so that actions are documented. The other is the realization that statistical tools merely point out the problems but are not themselves solutions. The burden of action on the process is still on the shoulders of the person that implemented it. In order to implement SPC effectively, three steps are continually followed:

1. Documenting and understanding the process and using process flow charts and component diagrams.
2. Establishing data collection systems and using SPC tools to identify process problems and opportunities for improvement.
3. Acting on the process and establishing guidelines to monitor and maintain process control.

Repeating steps 1-3 again.

These fundamentals are the basis of establishing specifications and operating philosophy with respect to SPC. The management of SPC, be it policy, function deployment or ongoing continuous improvement is accomplished in a systematic way by following the four step Plan, Do, Check, Act – PDCA/Shewart/Deming Cycles of Learning.

Quality and reliability

Table 1. Signetics Quality Journey

FOCUS		• Raw Material Quality • Product Quality • Individual Responsibility for Quality	• Supplier Partnerships • Manufacturing Excellence	• Customer Partnerships • In-process Quality Control • Product Reliability	• Cross Functional Operation • Better Management Practices • Cycle Time Management	• Customer Driven • Design Quality • Involve Everyone • Competitive & Functional Benchmarks
INITIATIVES	**SUPPLIER**	• No Waiver Policy • Audits • Certification Program	• Recognition • Ship-to-Stock (STS)	• SPC Implementation	• Measurement-TQRDC • Supplier Teams	• Cycle Time Management • Broaden to Equipment & Service
	INTERNAL	• Decentralized Q & R Function • Crosby 14 Steps & Absolutes • 33 QITs Formed • All Employees Sign ZD Pledge	• JIT Manufacturing • Zero Accept Sampling Plans • Repeat 14 Steps	• SPC Introduction • Early Failure C/A Program • 14 Steps to 9 Elements • Customer Workshop	• Design Development Cycle Time Reduction • Make Market Cycle Time Reduction • Inventory Reduction • Baldrige Assessment & Planning	• 6 Sigma Strategy • Responsiveness Strategy • Benchmarking – Design Methodology – Mfg. Excellence – Quality & Service • QIP Audits • ISO 9001 Certification • TQE Award
	CUSTOMER	• PPM Program	• ZD Warranty Policy • STS Program • Customer Process Change Notification • Self Qual Program	• Listening Post-TQRDC • Advocate Program • Lot Traceability	• SPC Communications • Customer Certifications • Electronic Data Interchange	• Customer Relationship Management Plan • Customer Survey • Quality Strategy Communications
GOAL		• Conformance to Requirements • Zero Defects	• Zero Defects to Customers	• Conformance to Customer Requirements • Continuous Improvement	• Total Customer Satisfaction • Cycle Time Entitlement	• Industry Leader in Customer Satisfaction • 6 Sigma Quality • World Class Responsiveness
		1980 – 1983	**1984 – 1985**	**1986 – 1988**	**1989 – 1990**	**1991 – 1994**

Quality and reliability

Figure 2. Total Quality Management Model

CYCLE TIME MANAGEMENT (CTM)

Cycle Time Management efforts are focused on Design-Development Process and Make-Market Process Responsiveness. Both are aimed at reducing the cycle time of tasks from current performance (Baseline) to entitlement (Using Existing Resources) then to improved entitlement and theoretical limit.

Design-Development focuses on getting the right products and processes to production within the market window interval. Make-Market concentrates on getting product into the customers hands within Customer Lead Time Requirements. Cycle time management directly links to quality improvement in its requirement for task barrier identification at the root cause level and removal of those barriers (e.g. eliminating causes of rejects thereby eliminating rework or product sort). Also, the acceleration of results from reducing cycle time increases the frequency of events thereby increasing the cycles of learning required for quality improvement.

Quality and reliability

DESIGN FOR MANUFACTURABILITY (DFM) AND SIX SIGMA

A by-product of CTM application to the Design-Development Process (DDP) is the Signetics proprietary DDP manual introduced in January 1991 followed by Cross Functional Team (CFT) training. The DDP applies to all product, package and technology groups in Signetics. CFT's are used to drive the project from planning phase until all objectives of the new product contract are met. The requirements for SPC, DFM and meeting Six Sigma objectives are contained in the DDP manual. The CFTs are responsible for assuring that DFM occurs with an objective of Six Sigma. A Six Sigma design means that any desired characteristic of a part has a yield of 99.9997% or a defect rate of 3.4PPM (C_p of 2 or C_{pk} of 1.5)

QUALITY PERFORMANCE

Our Quality Improvement Process has influenced our entire production cycle - from the purchases of raw materials to the shipment of finished product. The involvement of all areas of the company has resulted in impressive quality improvements. A traditional quality gauge is final electrical and visual/mechanical product defect levels as measured upon first submittal results at outgoing Quality Assurance gates; Estimated Process Quality (EPQ). This is the PPM Level at our outgoing inspection for all accepted and rejected lots. (See Figures 3 and 4.) Current product shipments routinely record below 20PPM (Parts Per Million) electrical defect levels and 150PPM visual/mechanical defect levels. Since we utilize zero accept sampling on all finished product inspection, any lot with one or more rejects is rejected and 100 percent inspected.

The most meaningful measure of our quality is how we measure up to our customer's expectations. Many customers routinely send us incoming inspection data or ratings on our products and services. In 1991, Signetics also implemented a formal annual customer survey to solicit inputs on Signetics performance to the Dimension of Performance deemed relevant by the customer. Signetics is very appreciative of the recognition given by customers. Since 1986, Signetics has received over 70 formal commendation plaques from customers in recognition of Quality, Delivery and Service. Due to this type of performance, a number of our customers have eliminated expensive incoming inspection testing and have subscribed to the Ship-to-Stock Program. (See Figure 5.)

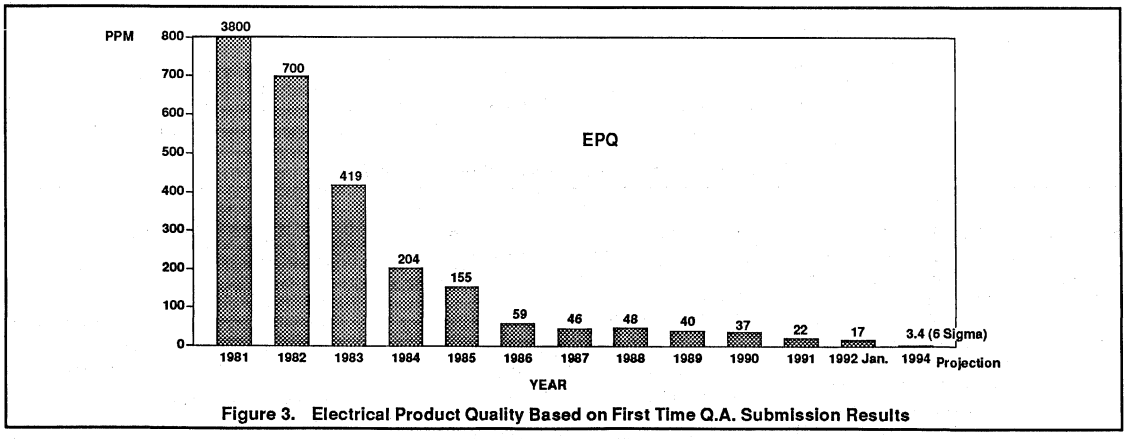


Figure 3. Electrical Product Quality Based on First Time Q.A. Submission Results

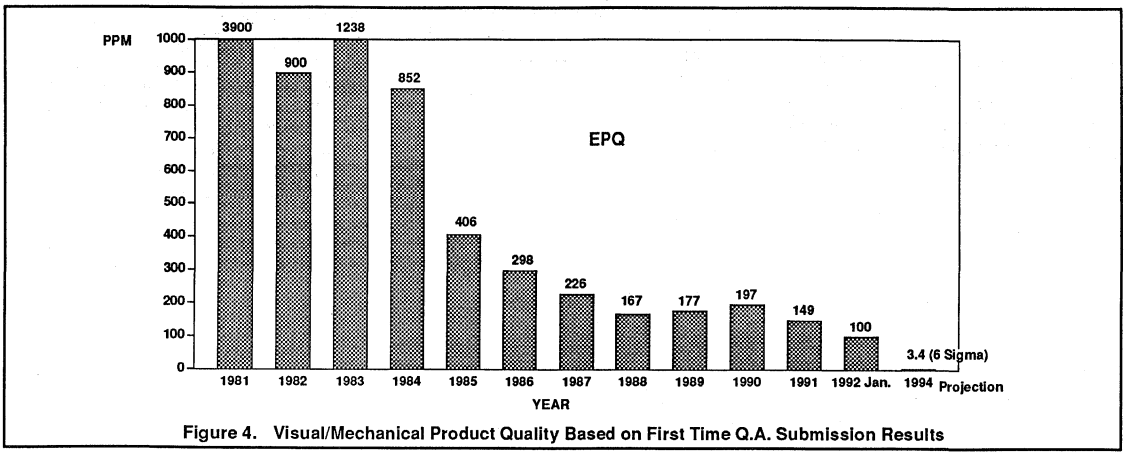
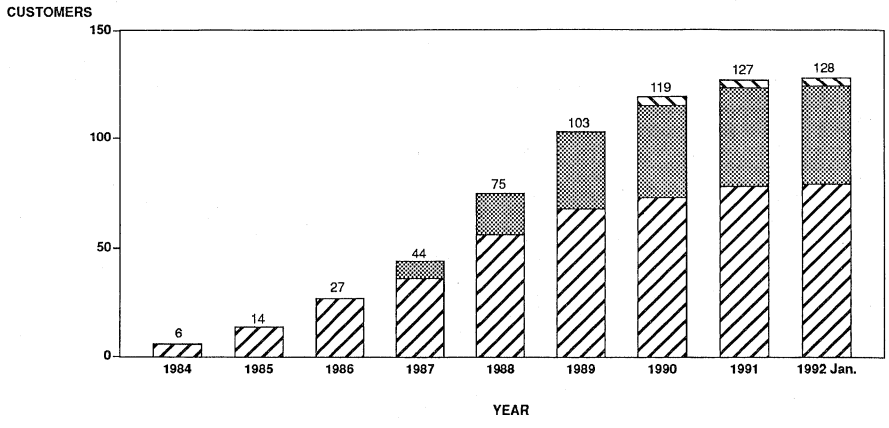


Figure 4. Visual/Mechanical Product Quality Based on First Time Q.A. Submission Results

Quality and reliability



	1984	1985	1986	1987	1988	1989	1990	1991	Jan. 1992
Asia Customers							4	4	4
Euro Customers				8	19	35	42	45	45
U.S. Customers	6	14	27	36	56	68	73	78	79

Figure 5. Signetics Ship-To-Stock Customer Growth

SHIP-TO-STOCK PROGRAM

Ship-to-Stock is a formal program developed at the request of our customers to help them reduce their costs by eliminating incoming test and inspection. Through close work with these customers in our quality improvement program, they became confident that our defect rates were so low that the redundancy of incoming inspections and testing was not only expensive, but unnecessary. They also saw that added component handling increased the potential of causing defects.

Ship-to-Stock is a joint program between Signetics and a customer which formally certifies specific parts to go directly into the customer's assembly line or inventory. This program was developed at the request of several major manufacturers after they had worked with us and had a chance to experience the data exchange and joint corrective action occurring as part of our quality improvement program.

Manufacturers using large volumes of ICs, those who are evaluating Just-in-Time delivery programs, or those who want to reduce or avoid high-cost incoming inspection are strongly encouraged to participate in this worthwhile program. Contact your local sales representative for further assistance and information on how to participate in this program.

RELIABILITY ASSURANCE PROGRAMS

Focus on Product Reliability

From 1981 to 1984, continuing improvements in process and material quality had a significant impact on product reliability.

Since 1984, the company has intensified its effort to markedly improve product reliability. Corporate Reliability Engineering, Group and Plant Reliability Units and Manufacturing Engineering work jointly on numerous improvement activities. These focused activities enhance the reliability of future products by providing improved methods for reliability assessment, increased understanding of failure physics, advanced analytical techniques, and aid in the development of material and processes.

Quality and reliability

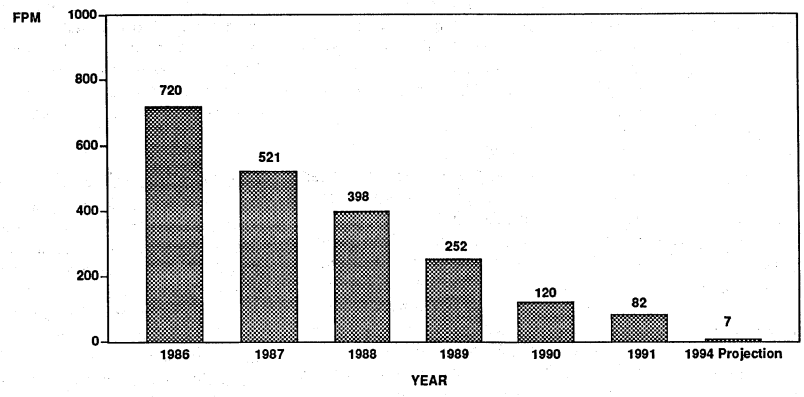


Figure 6. Signetics Early Failure Rate (EFR) Levels

EARLY FAILURE RATE (EFR) FOCUS

In 1986 Signetics intensified the focus on Early Life Reliability because of the significant impact EFR failures have on end system reliability performance. This program, which has now become a standard element in our reliability monitoring activities, provides quality engineering with statistically significant definition of low level process related defects. From these data, focused failure mechanism corrective actions can be developed. Average EFR levels on a broad cross section of processes, have been reduced from 720FPM to less than 100FPM since the corrective action effort was initiated in 1986 (reference Figure 6). Details of that activity are available upon request.

RELIABILITY MEASUREMENT PROGRAMS

Comprehensive product and process qualification programs have been developed to assure that our customers are receiving highly reliable products for their critical applications. Additionally, ongoing reliability monitoring programs, SURE III and Product Monitor, sample standard production on a regularly established basis (see Table 2).

Table 2. Reliability Assurance Programs

RELIABILITY FUNCTION	TYPICAL STRESS	FREQUENCY
New Process Qualification	High Temperature Operating Life Temperature-Humidity, Biased, Static High Temperature Storage Life Pressure Pot Temperature Cycle	Each new wafer fab process (and facility) Each new assembly process (and facility)
New Product Qualification	High Temperature Operating Life Temperature-Humidity, Biased, Static High Temperature Storage Life Pressure Pot Temperature Cycle Electrostatic Discharge Characterization	Each new product family
SURE III	High Temperature Operating Life Temperature-Humidity, Biased, Static Pressure Pot Temperature Cycle	Each fab process family, every four weeks
Product Monitor	Pressure Pot	Each plastic package type and technology family at each assembly plant, every week

Quality and reliability

DESCRIPTION OF STRESSES

High Temperature Operating Life

Static High Temperature Life (SHTL) stressing applies static DC bias to the device. This has specific merit in detecting ionic contamination problems which require continuous uninterrupted bias to drive contaminants to the silicon surface. The voltage bias must be maintained until the devices are cooled down to room temperature from the elevated life test temperature. Dynamic High Temperature Life (DHTL) stressing is not as effective in detecting such problems because the bias continuously changes, intermittently generating and healing the problem. For this reason, SHTL has typically been used as the accelerated life stress for Logic products. DHTL is useful for products such as memory and micro-processor/controller where a large portion of the area can only be accessed by dynamic means.

HTSL-High Temperature Storage Life

This stress exposes the parts to elevated temperatures (150°C-175°C) with no applied bias. For plastic packages, 175°C is the high end of its safe temperature region without accelerating untypical failure mechanisms. This test is intended to accelerate potential mechanical package-related failure mechanisms such as Gold-Aluminum bond integrity and other process instabilities.

THBS-Temperature-Humidity, Biased, Static

The accelerated temperature and humidity bias is performed at 85°C and 85% relative humidity (85°C/ 85% RH). In general, the worst case bias condition is the one which minimizes the device power dissipations and maximizes the applied voltages. Higher power dissipations tend to lower the humidity level at the chip surface and lessen the corrosion susceptibility.

TMCL-Temperature-Cycling, Air to Air

The device is cycled between the specified upper and lower temperature without power in an air or Nitrogen environment. Normal temperature extremes are -65°C and +150°C with a minimum 10 minute dwell and 5 minute transition per MIL-STD-883C, Method 1010.5, Condition C. This is a good test to measure the overall package to die mechanical compatibility, because the thermal expansion coefficients of the plastic are normally very much higher than those of the die and leadframe. However, for large die the stress may be too severe and induce failures that would not be expected in a real application.

PPOT-Pressure Pot

This stress exposes the devices to saturated steam at elevated temperature and pressure. The standard condition is 20 PSIG which occurs at a temperature of 127°C and 100% RH. The stress is used to test the moisture resistance of plastic encapsulated devices. The plastic encapsulant is not a moisture barrier and will saturate with moisture within 72 hours. Since the chip is not powered up the chip temperature and relative humidity will be the same as the autoclave once equilibrium is reached. Because the steam environment has an unlimited supply of moisture and ample temperature to catalyze thermally activated events, it is effective at detecting corrosion problems, contamination induced leakage problems, and general glassivation stability and integrity. It is also a good test for both package integrity (cracks in the package), and for die cracks (the moisture swells the plastic enough to stress the die; also the moisture causes leakage paths in the crack itself).

PRODUCT AND PROCESS QUALIFICATION PROGRAMS

Qualification activity is centered around new products and processes and changes in products and processes. The goal is to assure that the products can meet the qualification requirements prior to general release, and on an ongoing basis to demonstrate conformance to those requirements. The nature and extent of reliability stressing required depends on the type of change and the amount of applicable reliability data available.

A full qualification may include Early Failure Rate (EFR), Intrinsic Failure Rate (IFR), and Environmental Endurance Stressing. Such stress plans are reserved for introductions or changes that involve new or untested material or processes and, as such should be subjected to the maximum reliability interrogation. This normally entails a full range of biased and unbiased temperature and humidity stresses along with thermo-mechanical stresses.

For changes that are of limited scope, the full range of qualification stressing may not be warranted. In these instances, the nature and extent of the change is examined and only those stresses which provide a valuable measure of the change, or those which will detect potential weakness, are performed.

SELF-QUAL PROGRAM (SQP)

Self-Qual, initiated in 1984, is a joint program between Signetics and a customer that formally communicates the qualification activities for a new or changed product, process, or material. The Self Qual process provides our customer's engineering groups an opportunity to participate in the development of the qualification plan. During the qualification process, customers may audit the project, and can receive interim updates of qualification progress. Upon completion, formal detailed engineering reports are provided.

The major impact to the customer comes from the reduced workload on the component engineering and qualification groups. These engineering resources generally divide their time between routine qualification activity and problem resolution on critical components. By eliminating the need to perform qualification for one of the basic supplier changes the customer component engineer can spend more of his time resolving the critical product issues. In addition, the total amount of stress hardware needed to perform qualification life tests and other environmental evaluations can be reduced, saving the customer facility costs and reducing operating expense.

Self-Qual is a no-risk proposition for the customer. Each Self-Qual proposal provides a detailed description of what we are changing and why. It includes a detailed plan of what we intend to do to establish the reliability of the products affected. If the customer wishes to have product added to the plan or select some additional stresses, or prefers alternative stress conditions, Signetics will do everything possible to accommodate those requests. After that, if the customer is still uncomfortable with the recommended change, they are under no obligation to accept our data, and they may also perform their own qualification program. Customers who are interested in participating in this program should contact their local sales representative or the Corporate Reliability Engineering department directly.

Quality and reliability

SURE III RELIABILITY MONITORING PROGRAM

In order to implement an improvement program, a standard measure of performance was needed. The results from the SURE III Reliability Monitoring Program are used as basic ongoing measures of product reliability performance. This program samples all generic families of products manufactured and utilizes standardized stress methods and test procedures. A measurement philosophy was adopted based on the premise of continual improvement toward our performance standard of zero defects. We also increased our standard Pressure Pot stress conditions from 15 PSIG/121°C to 20 PSIG/127°C. This reduced stress duration from 168 hours to 72 hours, and increased high volume sampling, which increased sensitivity to low defect levels. Our standard monitoring program, SURE III, includes the stress conditions as described in Table 3. The continuous improvement results are shown in Figure 7 Signetics Reliability Index as Failure Per Million (FPM). The FPM value includes all rejects from all accelerated stresses divided by total units submitted to all stresses. This is a relative number used to manage continuous reliability improvement. It should not be interpreted as an expected failure rate. Figure 8 shows the continuous improvement in the SURE III 1000 Hour High-Temperature (T_J > 150°C) Operating Life Test FPM (includes early and intrinsic failure rates) for all technologies combined.

The 428 FPM for 1991 derates to 1 FIT at 45°C ambient temperature when assumptions of 0.7eV, 60% UCL and an 8°C junction rise above ambient are used. Admittedly the 1 FIT calculation for 1991 includes all technologies and unsubstantiated assumptions, but is a plausible number. Detailed FIT calculations by family do exist. Failure rate information is provided in the Signetics Product Reliability Summary Report available to all customers. In addition, the Signetics Reliability Handbook and the Signetics Process Technology and Manufacturing Facility Roadmap publications further define the rationale for methods used and the formation of process, product and package families.

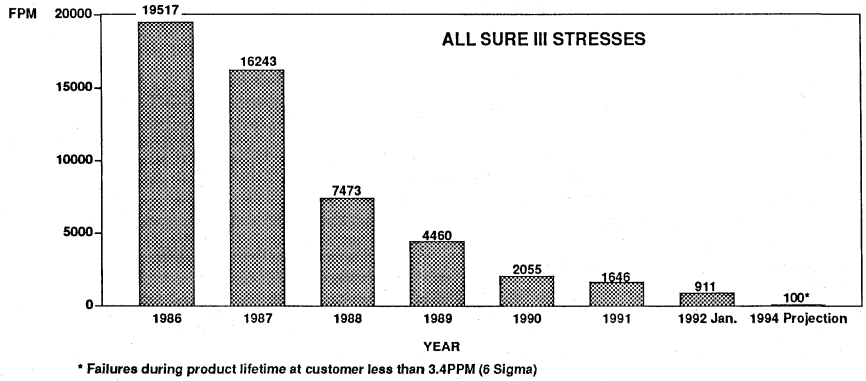


Figure 7. Signetics Reliability Index

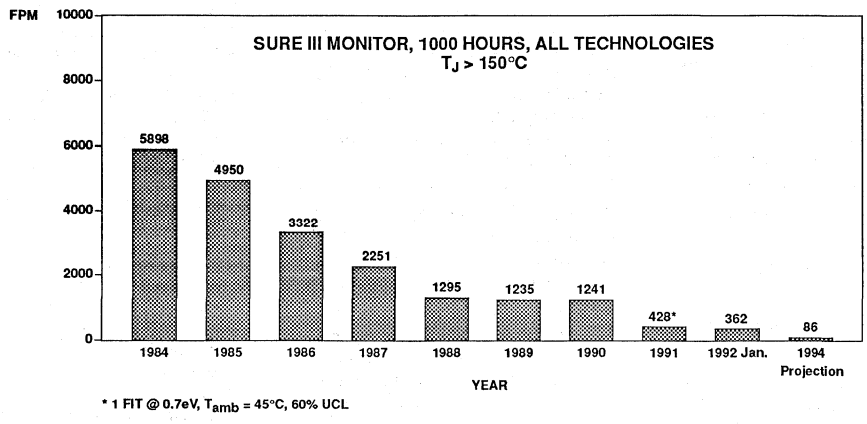


Figure 8. High-Temperature Operating Life Test FPM

Quality and reliability

Table 3. SURE III Reliability Monitoring Program

RELIABILITY FUNCTION	STRESS CONDITIONS	# UNITS
Static High Temperature Operating Life (SHTL)	$Tj \geq 150°C$, $T_{amb} = 125°C$ to 150°C, Biased condition = Static, V_{CC} = MAX, Duration = 1000 hours	135/150 Monthly
Temperature-Humidity, Biased, Static (THBS)	$T_{amb} = 85°C \pm 3°C$, Humidity = 85% RH ± 5%, Biased condition = Static, V_{CC} = MAX, Duration = 1000 hours	100 Monthly
Temperature Cycling (TMCL)	T_{amb} = -65°C (+0°C -10°C) to +150°C (+10°C -0°C), Air-to-Air, Dwell time = 10 minutes minimum each extreme, Biased condition = None, Duration = 1000 cycles for plastic package, 300 cycles for ceramic package	100 Monthly
Pressure Pot	$T_{amb} = 127°C \pm 2°C$, 20 PSIG ±0.5 PSIG (PPOT). 100% saturated steam, Biased condition = None, Duration = 72 hours	100 Weekly
		435/450 per Family

NOTE: V_{CC} = MAX is generally equal to V_{CC} = MAX as specified in data handbook

PRODUCT MONITOR

In addition to the SURE III program, each assembly plant performs Pressure Pot (20PSIG, 127°C, 72hours) reliability monitors on a weekly basis for each molded package type by pin count. The purpose of this program is to monitor the consistency of the assembly operations for such attributes as molding quality and die attach and wire bond integrity. This data is reported back to manufacturing operations and corporate and group reliability and quality assurance departments by electronic mail each week.

RELIABILITY EVALUATION

In addition to the product performance monitors encompassed in the SURE III program, Corporate and Group Reliability Engineering departments sustain a broad range of evaluation and qualification activities. Included in the engineering process are:

- Evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities, and subcontractors.
- Devices or generic group failure rate studies.
- Advanced environmental stress development.
- Failure mechanism characterization and corrective action/prevention reporting.

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE III program; however, more highly accelerated conditions and extended durations typify these engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity, are included in some evaluation programs.

STRESS FACILITY QUALITY

Quality improvement has reached all functional areas of the company, and the reliability stress laboratories are no exception. Corporate Reliability Laboratory (CRL) is one of the many areas where the benefits of the quality improvement process pays repeated dividends.

CRL utilizes stress which accelerate failure rates hundreds to thousands of times, requiring precision and control to make reliability data meaningful. Stress loading schedules are maintained with absolute regularity and chambers are never off-line beyond scheduled loading plans. Board currents are recorded prior to and at each interval on biased stresses, and monitoring of in-oven currents is conducted daily.

Thermal modeling of the Temperature Cycling systems has been accomplished and all loads are carefully weighed to ensure that thermal ramps are consistent.

Pressure Pot and Biased Pressure Pot systems utilize microprocessor controllers, and are accurate to within 0.1 degree centigrade. Saturation is guaranteed via automatic timing circuits, and a host of fail-safe controls ensure that test groups are never damaged.

Electrostatic discharge (ESD) handling precautions are standard procedures in the laboratories, and the occurrences of devices lost, zapped, or overstressed have become almost non-existent.

MANUFACTURING FACILITIES

Signetics, as part of a multinational corporation, utilize manufacturing facilities for wafer fabrication, package assembly, and test in three states and six overseas countries as shown in Table 4. Wafer fabrication is performed in fabs which report to the Product Groups. Assembly operations in Korea and Thailand report to Assembly Manufacturing Operations (AMO). Assembly subcontractors are scheduled and controlled through the AMO organization. Assembly subcontractors process all product to Signetics' specifications and materials. We have on-site quality assurance personnel at each subcontractor site to audit assembly processes and procedures.

TYPICAL IC MANUFACTURING FLOW

The manufacturing process for integrated circuits begins with wafer fabrication. The wafers are then electrically sorted, assembled, and tested prior to customer shipment. Quality assurance inspections are utilized throughout the manufacturing process, with manufacturing being responsible for the process/product quality.

Quality and reliability

Table 4. Product Manufacturing

FACILITIES	DESIGNATION	LOCATION	PROCESS OR PACKAGE FAMILIES
Wafer Fabrication	Fab 01	Sunnyvale, California, USA	Bipolar, Linear, Junction Isolated and Quality Assurance
	Fab 21	Orem, Utah, USA	Bipolar Gold Doped, Schottky, Oxide Isolated, ECL, PLD and Quality Assurance
	Fab 22	Albuquerque, New Mexico, USA	NMOS, CMOS, ACMOS, BiCMOS, EPROM and Quality Assurance
	Fab 23	Albuquerque, New Mexico, USA	CMOS EPROM, Flash EPROM, BiCMOS, and Quality Assurance
	MOS #2	Nijmegen, The Netherlands	HC(T) CMOS Logic and Quality Assurance
Assembly	Alphatec (R)	Bangkok, Thailand	Ceramic DIP and Quality Assurance
	Anam (L)	Seoul, Korea	Plastic DIP, SO, PLCC, Metal Can and Quality Assurance
	ASAT (C)	Hong Kong	Plastic QFP, SO, and Quality Assurance
	HANA (M)	Bangkok, Thailand	Plastic DIP and Quality Assurance
	Hyundai (W)	Ichon, Kyungki, Korea	Plastic DIP, SO, PLCC, Ceramic DIP and Quality Assurance
	MEC (T)	Osaka, Japan	Plastic SO EIAJ, QFP and Quality Assurance
	Orem (P)	Orem, Utah, USA	Ceramic DIP, Flat Pack, QFP, PGA and Quality Assurance
	Pebei (B)	Kaosiung, Taiwan	Plastic DIP, SO, SSOP, PLCC, and Quality Assurance
	SigKor (K)	Seoul, Korea	Plastic DIP, SO, PLCC, and Quality Assurance
	Sig Thai (V)	Bangkok, Thailand	Plastic DIP, SO, and Quality Assurance
	Rohm (G)	Kyoto, Japan	Plastic QFP and Quality Assurance
Test	TA05	Sunnyvale, California, USA	Wafer Sort, Final Test and Quality Assurance
	SigKor	Seoul, Korea	Final Test and Quality Assurance
	SigThai	Bangkok, Thailand	Final Test and Quality Assurance
	Albuquerque	Albuquerque, New Mexico, USA	Wafer Test and Quality Assurance
	Orem	Orem, Utah, USA	Wafer Test, Military Final Test and Quality Assurance

Table 5. Package Construction

ITEMS	PLASTIC DIP	SO AND PLCC	CERAMIC DIP(CERDIP)	CERAMIC FLAT PACK
Lead Frame	Copper, 194 Alloy	Copper, 194 or PMC102	Alloy-42	Alloy-42
Lead Finish	Tin/Lead Solder Dip (60/40)	Tin/Lead Solder Dip (60/40) or Solder Plate (80/20)	Tin/Lead Solder Dip (60/40)	Tin/Lead Solder Dip (60/40)
Bond Area Finish	Silver Spot	Silver Spot	Silver Spot	Silver Spot
Die Attach	Silver Filled Polymide or Thermoplastic	Silver Filled Polymide or Thermoplastic	Silver Filled Glass	Silver Filled Glass
Bond Wire	Gold, 1.0-1.3 mils in Diameter	Gold, 1.0-1.3 mils in Diameter	Aluminum, 1.0-1.3 mils in Diameter	Aluminum, 1.0-1.3 mils in Diameter
Wire Bonding Die Lead Frame	Thermosonic Ball Stitch	Thermosonic Ball Stitch	Ultrasonic Stitch Stitch	Ultrasonic Stitch Stitch
Package Material	Novolac Epoxy	Novolac Epoxy	Ceramic	Ceramic

SPECIAL PROCESSING

SUPR II LEVEL B –

For our customers who require an infant mortality rate level less than that normally provided for our standard products (typically less than 1000PPM), we offer our Signetics Upgraded Product Reliability (SUPR) program.

Devices are burned-in per Signetics specification 850-227 schematics for a minimum of 21 hours at junction temperature between 155°C to 175°C. For a 1.0eV activation energy, 21 hours at 155°C is equivalent to 168 hours at 125°C.

Following burn-in, all devices are cooled down under bias and tested within 96 hours. All devices are tested before and after burn-in, yield calculated and compared to Percent Defective Allowed (PDA). If a lot fails PDA, it is investigated and good units submitted to a second burn-in. All "SUPR II B" devices carry a "B" marking.

The SUPR program was introduced in 1972 to improve quality and reliability and was expanded in 1975 to SUPR II A which included the burn-in option, SUPR II B. With the implementation of the Signetics Quality Improvement Process in 1980, standard product quality levels and guarantees caught up and passed SUPR II. All processing,

Quality and reliability

except for burn-in, is now standard. The Signetics standard warranty is Zero Defects.

"Evaluation of Early Failure Levels and The Effectiveness of Burn-In" is available upon request through your local sales office. This brochure is an aid for those users and purchasers of integrated circuits who need to make a decision regarding burn-in.

PUBLICATIONS

Signetics routinely publishes documents supporting the Quality and Reliability Improvement Process. The following significant documents are currently available.

IC Quality Series

Quality and Reliability Policy Manual (850-8000)

This manual is the starting point for understanding the policies of Signetics pursuant to constantly improving the high standards of quality and reliability in the manufacture of monolithic integrated circuits. Responsibilities and authority of organizations are defined along with governing specifications and operator instruction documents.

Signetics QIP Total Quality Management

This booklet describes the TQM model, patterned after the U.S.A. Malcom Baldrige National Quality Award criteria and how the model is applied to the Signetics Quality Improvement Process.

Supplier Partnership Guide

This booklet defines Signetics philosophy, policy and requirements for establishing strategic partnerships with raw material suppliers.

Product Symbol Formats

This publication provides a guide for determining standard product symbol format and content for decoding inventory and product in field usage since 1980. Since date code 8717, Signetics has symbolized the assembly start computer Lot ID on commercial products providing full traceability back to start of wafer fabrication.

Quality Attributes EDI System

This manual defines system requirements for Electronic Data Interchange (EDI) of Quality Attributes (pass/fail) Data.

Monthly Product Outgoing Quality Summary Reports

Estimated Process Quality (EPQ) in PPM for electrical, visual/ mechanical and hermeticity by part number or by family.

Statistical Process Control

This booklet introduces the Signetics SPC system including terminologies, philosophy, organization, training and implementation strategy and status.

Ship-To-Stock Program

This booklet defines the "joint program" requirements of Signetics and the customer to formally certify specific products to go directly into the assembly line or inventory with reduced or no incoming inspection thereby reducing cost of ownership.

Customer Return Immediate Service Program (CRISP)

This booklet defines the joint responsibilities of Signetics and the customer to assure that correlation samples are investigated and results reported per the Signetics 1-4-5 cycle time commitments.

IC Reliability Series

Signetics Reliability Handbook

This handbook is a detailed guide to Signetics Reliability Qualification and Monitoring activities. It includes reference sections that deal with the application and statistics of integrated circuit reliability issues.

Product Reliability Summary

Yearly, SURE III monitoring data is summarized and published for all product families in a Product Reliability Summary. Summaries like this one provide a detailed overview of product family performance and estimates the reliability of those products in use conditions.

Quarterly Reliability Update

Detailed results, by part number, package type, date code, assembly location, and by stress and test interval are routinely published in the Signetics Quarterly Reliability Update. The "Update" is available at the end of each quarter, and contains the results of reliability monitors which completed during the previous quarter, plus approximately 3 years of history for each product family.

SMD Reliability (The Reliability and Durability of Surface Mount Packages)

In support of Signetics' leadership in Surface Mount Device (SMD) technology, we have published in-depth studies and evaluations on the reliability and durability of SMD packages. The Surface Mount Reliability report covers evaluation of products after exposure to the unique environments created by various SMD soldering and cleaning processes.

Process Technology and Manufacturing Facility Roadmap

This document defines the various process technologies in production in Signetics manufacturing facilities, and defines in detail, the fab and assembly processes and locations qualified to produce all released products.

Thermal Characteristics of Integrated Circuit Packages

This is a comprehensive collection of thermal characterization data for all packages manufactured by Signetics. Thermal resistance data to *Case*, and to *Ambient* are provided. Details on airflow effects and die size are included.

SSQP – Signetics Self-Qual Program-Reports

In addition to the regular publications of reliability monitor results, a special program for the publication of qualification proposals and final engineering reports has been in place since January of 1984. Self-Qual Reports are available on all major process changes and introductions, thereby reducing customer cost of ownership.

Evaluation of Early Failure Levels and the Effectiveness of Burn-In

This report provides results of the Signetics Early Failure Rate (EFR) program implemented in 1986 to identify and eliminate root causes of infant mortality and to aid users of IC components faced with a decision regarding Burn-In of purchased integrated circuits.

DATA AVAILABILITY

The previously referenced documents are available to all our customers. Many are available in your local sales office, or from:

Corporate Quality System Group
Mail Stop #35
811 East Arques Avenue
P. O. Box 3409
Sunnyvale, CA 94088-3409, USA

where you can be placed on a standard mailing list for all documentation which meet your requirement(s).

The Quality and Reliability section is applicable to those products manufactured under the auspices of Signetics Company.

Section 2
Digital Data Communications Data Sheets

INDEX

Programmable communications interface (PCI) SCN2651

DESCRIPTION

The Signetics SCN2651 PCI is a universal synchronous/asynchronous data communications controller chip designed for microcomputer systems. It interfaces directly to the Signetics SCN2650 microprocessor and may be used in a polled or interrupt driven system environment. The SCN2651 accepts programmed instructions from the microprocessor and supports many serial data communication disciplines, synchronous and asynchronous, in the full or half-duplex mode.

The PCI serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data characters for input to the microcomputer.

The SCN2651 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode.

The PCI is constructed using Signetics n-channel silicon gate depletion load technology and is packaged in a 28-pin DIP.

FEATURES

- Synchronous operation
  - 5- to 8-bit characters
  - Single or double SYN operation
  - Internal character synchronization
  - Transparent or non-transparent mode
  - Automatic SYN or DLE-SYN insertion
  - SYN or DLE stripping
  - Odd, even, or no parity
  - Local or remote maintenance loopback mode
  - Baud rate: DC to 1Mbps (1X clock)
- Asynchronous operation
  - 5- to 8-bit characters
  - 1, 1-1/2 or 2 stop bits
  - Odd, even, or no parity
  - Parity, overrun and framing error detection
  - Line break detection and generation
  - False start bit detection
  - Automatic serial echo mode
  - Local or remote maintenance loopback mode
  - Baud rate: DC to 1Mbps (1X clock)
    DC to 62.5kbps (16X clock)
    DC to 15.625kbps (64X clock)

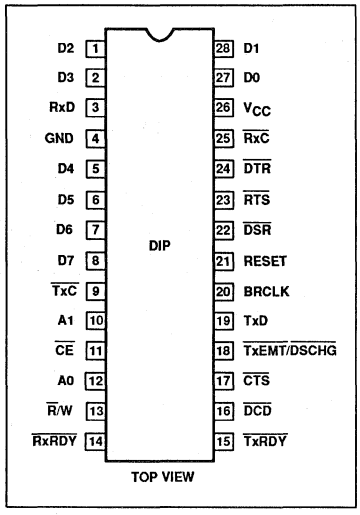
OTHER FEATURES

- Internal or external baud rate clock
- 16 internal rates – 50 to 19,200 baud
- Double buffered transmitter and receiver
- Full or half duplex operation
- TTL compatible inputs and outputs
- Single 5V power supply
- No system clock required
- 28-pin dual in-line package

APPLICATIONS

- Intelligent terminals
- Network processors
- Front-end processors
- Remote data concentrators
- Computer to computer links
- Serial peripherals

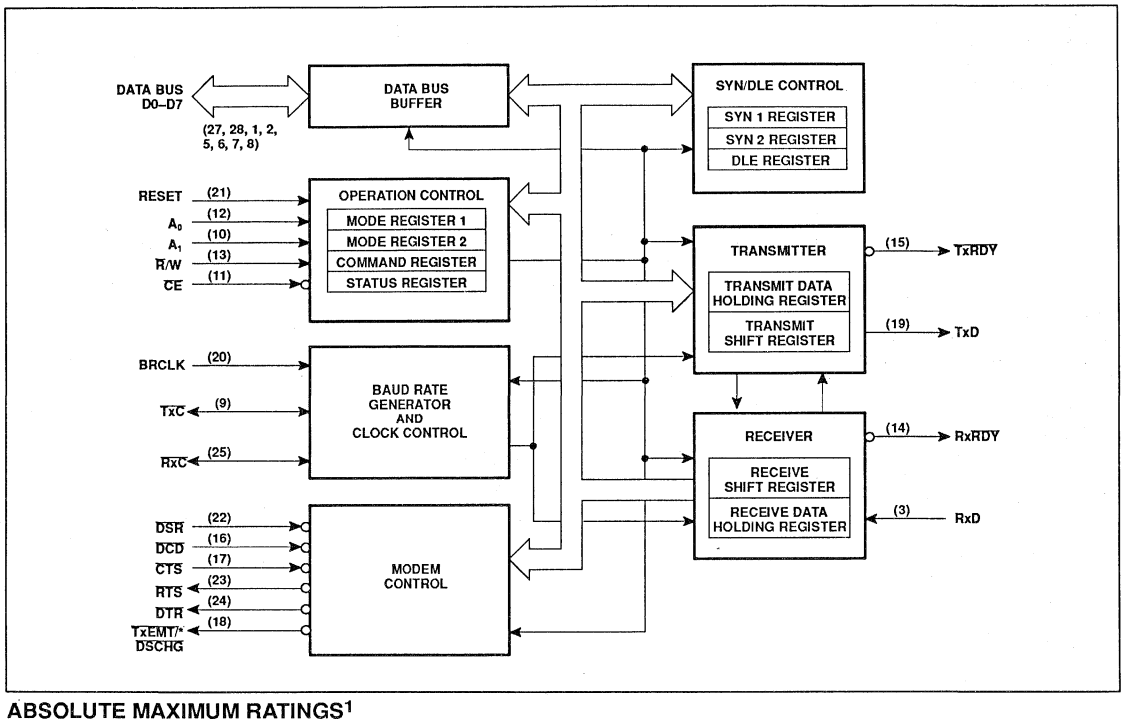
PIN CONFIGURATIONS



ORDERING CODE

PACKAGES	V_{CC} = 5V ±5%	
	Commercial	Automotive
	0°C to +70°C	-40°C to +85°C
Plastic DIP	SCN2651CC1N28	Not available

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	Note 4	°C
Storage temperature	-65 to +150	°C
All voltages with respect to ground[3]	-0.5 to +6.0	V

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effect of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over operating temperature range unless otherwise specified. See ordering code table for applicable temperature range and operating supply range.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
Output voltage						
V_{OL}	Low	I_{OL} = 1.6mA			0.4	V
V_{OH}	High	I_{OH} = -100µA	2.4			V
I_{IL}	Input leakage current	V_{IN} = 0 to 5.25V	-10		10	µA
3-State output leakage current						
I_{LH}	Data bus high	V_O = 4.0V	-10		10	µA
I_{LL}	Data bus low	V_O = 0.45V	-10		10	µA
I_{CC}	Power supply current				150	mA

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified. See ordering code table for applicable temperature range and operating supply range.
2. All voltage measurements are referenced to ground. All time measurements are at the 50% level for inputs (except t_{BRH} and t_{BRL}) and at 0.8V and 2.0V for outputs. Input levels for testing are 0.45V and 2.4V.
3. Typical values are at +25°C, typical supply voltages and typical processing parameters.

CAPACITANCE T_A = 25°C, V_{CC} = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Capacitance						
C_{IN}	Input				20	pF
C_{OUT}	Output	f_C = 1MHz			20	pF
$C_{I/O}$	Input/Output	Unmeasured pins tied to ground			20	pF

AC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Pulse width						
t_{RES}	Reset		1000			ns
t_{CE}	Chip enable		300			ns
Set-up and hold time						
t_{AS}	Address setup		20			ns
t_{AH}	Address hold		20			ns
t_{CS}	R/W control setup		20			ns
t_{CH}	R/W control hold		20			ns
t_{DS}	Data setup for write		225			ns
t_{DH}	Data hold for write		0			ns
t_{RXS}	RX data setup		300			ns
t_{RXH}	RX data hold		350			ns
t_{DD}	Data delay time for read	C_L = 100pF			250	ns
t_{DF}	Data bus floating time for read	C_L = 100pF			150	ns
t_{CED}	$\overline{CE}$ to $\overline{CE}$ delay		700			ns
Input clock frequency						
f_{BRG}	Baud rate generator		1.0	5.0688	5.0738	MHz
$f_{R/T}$[6]	$\overline{TxC}$ or $\overline{RxC}$		dc		1.0	MHz
Clock width						
t_{BRH}[5]	Baud rate high		70			ns
t_{BRL}[5]	Baud rate low		70			ns
$t_{R/TH}$	$\overline{TxC}$ or $\overline{RxC}$ high		500			ns
$t_{R/TL}$[6]	$\overline{TxC}$ or $\overline{RxC}$ low		500			ns
t_{TXD}	TxD delay from falling edge of $\overline{TxC}$	C_L = 100pF			650	ns
t_{TCS}	Skew between TxD changing and falling edge of $\overline{TxC}$ output[4]	C_L = 100pF		0		ns

NOTES:

1. Parameters are valid over operating temperature range unless otherwise specified. See ordering code table for applicable temperature range and operating supply range.
2. All voltage measurements are referenced to ground. All time measurements are at the 50% level for inputs (except t_{BRH} and t_{BRL}) and at 0.8V and 2.0V for outputs. Input levels for testing are 0.45V and 2.4V.
3. Typical values are at +25°C, typical supply voltages and typical processing parameters.
4. Parameter applies when internal transmitter clock is used.
5. Under test conditions of 5.0688MHz, f_{BRG}, t_{BRH}, and t_{BRL} measured at V_{IH} and V_{IL} respectively.
6. $t_{R/T}$ and $t_{R/TL}$ shown for all modes except local loopback. For local loopback mode $f_{R/T}$ = 0.7MHz and $t_{R/TL}$ = 700ns min.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	TYPE
27, 28, 1, 2, 5–8	D_0–D_7	8-bit data bus	I/O
21	RESET	Reset	I
12, 10	A_0–A_1	Internal register select lines	I
13	R/$\overline{W}$	Read or write command	I
11	$\overline{CE}$	Chip enable input	I
22	$\overline{DSR}$	Data set ready	I
24	$\overline{DTR}$	Data terminal ready	O
23	$\overline{RTS}$	Request to send	O
17	$\overline{CTS}$	Clear to send	I
16	$\overline{DCD}$	Data carrier detected	I
18	TxEMT/$\overline{DSCHG}$	Transmitter empty or data set change	O
9	$\overline{TxC}$	Transmitter clock	I/O
25	$\overline{RxC}$	Receiver clock	I/O
19	TxD	Transmitter data	O
3	RxD	Receiver data	I
15	$\overline{TxRDY}$	Transmitter ready	O
14	$\overline{RxRDY}$	Receiver ready	O
20	BRCLK	Baud rate generator clock	I
26	V_{CC}	+5V supply	I
4	GND	Ground	I

Table 1. Baud Rate Generator Characteristics Crystal Frequency = 5.0688MHz

BAUD RATE	THEORETICAL FREQUENCY 16X CLOCK	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
50	0.8KHz	0.8KHz	–	6336
75	1.2	1.2	–	4224
110	1.76	1.76	–	2880
134.5	2.152	2.1523	0.016	2355
150	2.4	2.4	–	2112
300	4.8	4.8	–	1056
600	9.6	9.6	–	528
1200	19.2	19.2	–	264
1800	28.8	28.8	–	176
2000	32.0	32.081	0.253	158
2400	38.4	38.4	–	132
3600	57.6	57.6	–	88
4800	76.8	76.8	–	66
7200	115.2	115.2	–	44
9600	153.6	153.6	–	33
19200*	307.2	316.8	3.125	16

NOTE:
*Error at 19200 can be reduced to zero by using crystal frequency 4.9152MHz.
16X clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1X.

BLOCK DIAGRAM

The PCI consists of six major sections. These are the transmitter, receiver, timing, operation control, modem control and SYN/DLE control. These sections communicate with each other via an internal data bus and an internal control bus. The internal data bus interfaces to the microprocessor data bus via a data bus buffer.

Operation Control

This functional block stores configuration and operation commands from the CPU and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with the microprocessor via the data bus and contains mode registers 1 and 2, the command register, and the status register. Details of register addressing and protocol are presented in the PCI programming section of this data sheet.

Timing

The PCI contains a baud rate generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full-duplex operation. See Table 1.

Receiver

The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU.

Transmitter

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

Modem Control

The modem control section provides interfacing for three input signals and three output signals used for "handshaking" and status indication between the CPU and a modem.

SYN/DLE Control

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the CPU. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

INTERFACE SIGNALS

The PCI interface signals can be grouped into two types: the CPU-related signals (shown in Table 2), which interface the SCN2651 to the microprocessor system, and the device-related signals (shown in Table 3), which are used to interface to the communications device or system.

Table 2. CPU-Related Signals

PIN NAME	PIN NO.	INPUT/OUTPUT	FUNCTION
V_{CC}	26	I	+5V supply input
GND	4	I	Ground
RESET	21	I	A high on this input performs a master reset on the SCN2651. This signal asynchronously terminates any device activity and clears the mode, command and status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.
$A_1 - A_0$	10, 12	I	Address lines used to select internal PCI registers.
$\overline{R}/W$	13	I	Read command when low, write command when high.
$\overline{CE}$	11	I	Chip enable command. When low, indicates that control and data lines to the PCI are valid and that the operation specified by the $\overline{R}W$, A_1 and A_0 inputs should be performed. When high, places the D_0–D_7 lines in the 3-State condition.
$D_7 - D_0$	8, 7, 6, 5 2, 1, 28, 27	I/O	8-bit, three-state data bus used to transfer commands, data and status between PCI and the CPU. D_0 is the least significant bit, D_7 the most significant bit.
$\overline{TxRDY}$	15	O	This output is the complement of status register bit SR0. When low, it indicates that the transmit data holding register (THR) is ready to accept a data character from the CPU. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be used as an interrupt to the CPU.
$\overline{RxRDY}$	14	O	This output is the complement of status register bit SR1. When low, it indicates that the receive data holding register (RHR) has a character ready for input to the CPU. It goes high when the RHR is read by the CPU, and also when the receiver is disabled. It is an open drain output which can be used as an interrupt to the CPU.
$\overline{TxEMT}$/ $\overline{DSCHG}$	18	O	This output is the complement of status register bit SR2. When low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. This output goes high when the status register is read by the CPU, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the CPU for this line to go high. It is an open drain output which can be used as an interrupt to the CPU.

OPERATION

The functional operation of the SCN2651 is programmed by a set of control words supplied by the CPU. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc. The programming procedure is described in the PCI programming section of the data sheet.

After programming, the PCI is ready to perform the desired communications functions. The receiver performs serial to parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the CPU to a serial bit stream. These actions are accomplished within the framework specified by the control words.

Receiver

The SCN2651 is conditioned to receive data when the $\overline{DCD}$ input is low and the RxEN bit in the command register is true. In the asynchronous mode, the receiver looks for a high to low transition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit-time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and one stop bit(s) have been assembled. The data is then transferred to the receive data holding register, the RxRDY bit in the status register is set, and the $\overline{RxRDY}$ output is asserted. If the character length is less than 8 bits, the high order unused bits in the holding register are set to zero. The parity error, framing error, and overrun error status bits are strobed into the status register on the positive going edge of $\overline{RxC}$ corresponding to the received character boundary. If a break condition is detected (RxD is low for the entire character as well as the stop bit[s]), only one character consisting of all zeros (with the FE status bit set) will be transferred to the holding register. The RxD input must return to a high condition before a search for the next start bit begins.

When the PCI is initialized into the synchronous mode, the receiver first enters the hunt mode on a 0 to 1 transition of RxEN (CR2). In this mode, as data is shifted into the receiver shift register a bit at a time, the contents of the register are compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly mode begins. If single SYN operation is programmed, the SYN detect status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN detect bit to be set. Otherwise, the PCI returns to the hunt mode. (Note that the sequence SYN1–SYN1–SYN2 will not achieve synchronization.) When synchronization has been achieved, the PCI continues to assemble characters and transfer them to the holding register, setting the RxRDY status bit and asserting the $\overline{RxRDY}$ output each time a character is transferred. The PE and OE status bits are set as appropriate. Further receipt of the appropriate SYN sequence sets the SYN detect status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the Holding Register. Note that the SYN characters used to establish initial synchronization are not transferred to the holding register in any case.

Table 3. Device-Related Signals

PIN NAME	PIN NO.	INPUT/OUTPUT	FUNCTION
BRCLK	20	I	5.0688MHz clock input to the internal baud rate generator. Not required if external receiver and transmitter clocks are used.
$\overline{RxC}$	25	I/O	Receiver clock. If external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. Data are sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin becomes an output at 1X the programmed baud rate.*
$\overline{TxC}$	9	I/O	Transmitter clock. If external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. The transmitted data changes on the falling edge of the clock. If internal transmitter clock is programmed, the pin becomes an output at 1X the programmed baud rate.*
RxD	3	I	Serial data input to the receiver. "Mark" is high, "Space" is low.
TxD	19	O	Serial data output from the transmitter. "Mark" is high, "space" is low. Held in mark condition when the transmitter is disabled.
$\overline{DSR}$	22	I	General purpose input which can be used for data set ready or ring indicator condition. Its complement appears as status register bit SR7. Causes a low output on $\overline{TxEMT/DSCHG}$ when its state changes.
$\overline{DCD}$	16	I	Data carrier detect input. Must be low in order for the receiver to operate. Its complement appears as status register bit SR6. Causes a low output on $\overline{TxEMT/DSCHG}$ when its state changes.
$\overline{CTS}$	17	I	Clear to send input. Must be low in order for the transmitter to operate. If it goes high during transmission, the character in the transmit shift register will be transmitted before termination.
$\overline{DTR}$	24	O	General purpose output which is the complement of command register bit CR1. Normally used to indicate data terminal ready.
$\overline{RTS}$	23	O	General purpose output which is the complement of command register bit CR5. Normally used to indicate request to send.

NOTE:
*$\overline{RxC}$ and $\overline{TxC}$ outputs have short circuit protection max. C_L = 100pF

Transmitter

The PCI is conditioned to transmit data when the $\overline{CTS}$ input is Low and the TxEN command register bit is set. The SCN2651 indicates to the CPU that it can accept a character for transmission by setting the TxRDY status bit and asserting the $\overline{TxRDY}$ output. When the CPU writes a character into the transmit data holding register, these conditions are negated. Data is transferred from the holding register to the transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again. Thus, one full character time of buffering is provided.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the transmit holding register, the TxD output remains in the marking (high) condition and the $\overline{TxEMT/DSCHG}$ output and its corresponding status bit are asserted. Transmission resumes when the CPU loads a new character into the holding register. The transmitter can be forced to output a continuous low (BREAK) condition by setting the send break command bit high.

In the synchronous mode, when the SCN2651 is initially conditioned to transmit, the TxD output remains high and the TxRDY condition is asserted until the first character to be transmitted (usually a SYN character) is loaded by the CPU. Subsequent to this, a continuous stream of characters is transmitted. No extra bits (other than parity, if commanded) are generated by the PCI unless the CPU fails to send a new character to the PCI by the time the transmitter has completed sending the previous character.

Since synchronous communication does not allow gaps between characters, the PCI asserts TxEMT and automatically "fills" the gap by transmitting SYN1s, SYN1–SYN2 doublets, or DLE–SYN1 doublets, depending on the state of MR16 and MR17. Normal transmission of the message resumes when a new character is available in the transmit data holding register. If the send DLE bit in the command register is true, the DLE character is automatically transmitted prior to transmission of the message character in the THR.

PCI PROGRAMMING

Prior to initiating data communications, the SCN2651 operational mode must be programmed by performing write operations to the mode and command registers. In addition, if synchronous operation is programmed, the appropriate SYN/DLE registers must be loaded. The PCI can be reconfigured at any time during program execution. However, if the change has an effect on the reception of a character the receiver should be disabled. Alternatively if the change is made 1 1/2 RxC periods after RxRDY goes active it will affect the next character assembly. A flowchart of the initialization process appears in Figure 1.

The internal registers of the PCI are accessed by applying specific signals to the $\overline{CE}$, R/$\overline{W}$, A_1 and A_0 inputs. The conditions necessary to address each register are shown in table 4.

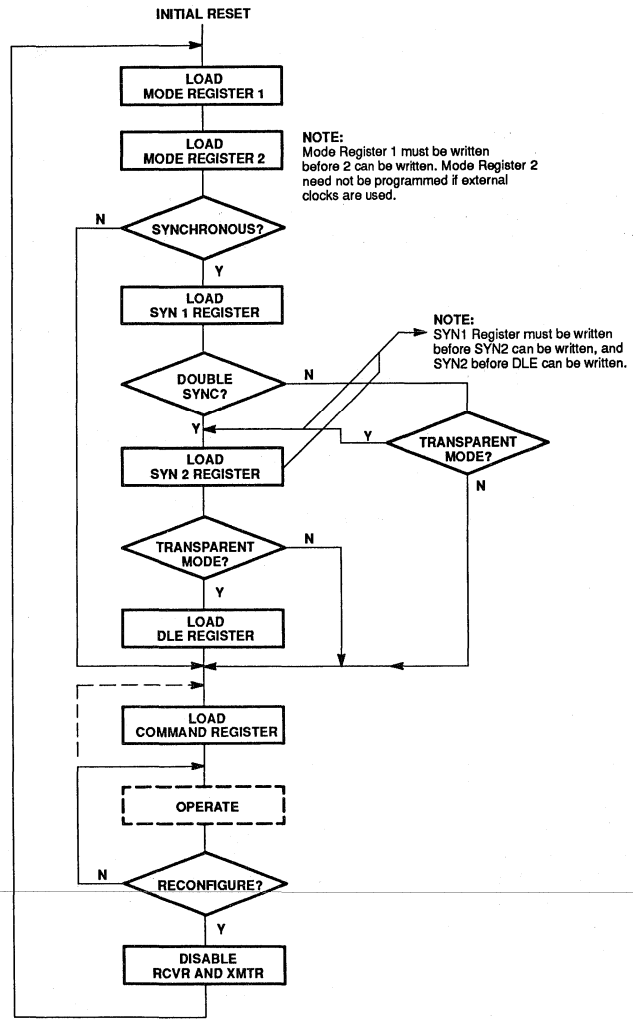


Figure 1. SCN2651 Initialization Flowchart

Table 4. SCN2651 Register Addressing

$\overline{CE}$	A_1	A_0	$\overline{R}/W$	FUNCTION
1	X	X	X	3-State data bus
0	0	0	0	Read receive holding register
0	0	0	1	Write transmit holding register
0	0	1	0	Read status register
0	0	1	1	Write SYN1/SYN2/DLE registers
0	1	0	0	Read mode registers 1/2
0	1	0	1	Write mode registers 1/2
0	1	1	0	Read command register
0	1	1	1	Write command register

NOTE:
See AC Characteristics section for timing requirements.

The SYN1, SYN2, and DLE registers are accessed by performing write operations with the conditions $A_1 = 0$, $A_0 = 1$, and $\overline{R}/W = 1$. The first operation loads the SYN1 register. The next loads the SYN2 register, and the third loads the DLE register. Reading or loading the mode registers is done in a similar manner. The first write (or read) operation addresses mode register 1, and a subsequent operation addresses mode register 2. If more than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointers are reset to SYN1 register and mode register 1 by a RESET input or by performing a "read command register" operation, but are unaffected by any other read or write operation.

The SCN2651 register formats are summarized in Tables 5, 6, 7 and 8. Mode registers 1 and 2 define the general operational characteristics of the PCI, while the command register controls the operation within this basic framework. The PCI indicates its status in the status register. These registers are cleared when a RESET input is applied.

Mode Register 1 (MR1)

Table 5 illustrates mode register 1. Bits MR11 and MR10 select the communication format and baud rate multiplier. 00 specifies synchronous mode and 1X multiplier. 1X, 16X, and 64X multipliers are programmable for asynchronous format. However, the multiplier in asynchronous format applies only if the external clock input option is selected by MR24 or MR25.

MR13 and MR12 select a character length of 5, 6, 7, or 8 bits. The character length does not include the parity bit, if programmed, and does not include the start and stop bits in asynchronous mode.

MR14 controls parity generation. If enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR15 selects odd or even parity when parity is enabled by MR14.

In asynchronous mode, MR17 and MR16 select character framing of 1, 1.5, or 2 stop bits. (If 1X baud rate is programmed, 1.5 stop bits default to 1 stop bit on transmit.) In synchronous mode, MR17 controls the number of SYN characters used to establish synchronization and for character fill when the transmitter is idle. SYN1 alone is used if MR17 = 1, and SYN1–SYN2 is used when MR17 = 0. If the transparent mode is specified by MR16, DLE–SYN1 is used for character fill and SYN detect, but he normal synchronization sequence is used. Also DLE

stripping and DLE detect (with MR14 = 0) are enabled.

Mode Register 2 (MR2)

Table 6 illustrates mode register 2. MR23, MR22, MR21, and MR20 control the frequency of the internal baud rate generator (BRG). Sixteen rates are selectable. When driven by a 5.0688MHz input at the BRCLK input (Pin 20), the BRG output has zero error except at 134.5 2000, and 19,200 baud, which have errors of +0.016%, +0.235%, and +3.125% respectively.

MR25 and MR24 select either the BRG or the eexternal inputs $\overline{TxC}$ and $\overline{RxC}$ as the clock source for the transmitter and receiver, respectively. If the BRG clock is selected, the baud rate factor in asynchronous mode is 16X regardless of the factor selected by MR11 and MR10. In addition, the corresponding clock pin provides an output at 1X the baud rate.

Table 5. Mode Register 1 (MR1)

MR17	MR16	MR15	MR14	MR13	MR12	MR11	MR10
		Parity Type	**Parity Control**	**Character Length**		**Mode and Baud Rate Factor**	
Async: Stop bit length 00 = Invalid 01 = 1 Stop bit 10 = 1 1/2 Stop bits 11 = 2 Stop bits		0 = Odd 1 = Even	0 = Disabled 1 = Enabled	00 = 5 Bits 01 = 6 Bits 10 = 7 Bits 11 = 8 Bits		00 = Synchronous 1X rate 01 = Asynchronous 1X rate 10 = Asynchronous 16X rate 11 = Asynchronous 64X rate	
Sync: Number of SYN char 0 = Double SYN 1 = Single SYN	**Sync: Transparency control** 0 = Normal 1 = Transparent						

NOTE:
Baud rate factor in asynchronous applies only if external clock is selected. Factor is 16X if internal clock is selected. Mode must be selected (MR11, MR10) in any case.

Table 6. Mode Register 2 (MR2)

MR27	MR26	MR25	MR24	MR23	MR22	MR21	MR20
		Transmitter Clock	**Receiver Clock**	**Baud Rate Selection**			
Not used		0 = External 1 = Internal	0= External 1 = Internal	0000 = 50 Baud 0001 = 75 0010 = 110 0011 = 134.5 0100 = 150 0101 = 300 0110 = 600 0111 = 1200		1000 = 1800 Baud 1001 = 2000 1010 = 2400 1011 = 3600 1100 = 4800 1101 = 7200 1110 = 9600 1111 = 19,200	

Table 7. Command Register (CR)

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
Operating Mode		**Request to Send**	**Reset Error**		**Receive Control (RxEN)**	**Data Terminal Ready**	**Transmit Control (TxEN)**
00 = Normal operation 01 = Async: automatic echo mode Sync: SYN and/or DLE stripping mode 10 = Local Loopback 11 = Remote Loopback		0 = Force $\overline{RTS}$ output high 1 = Force $\overline{RTS}$ output low	0 = Normal 1 = Reset error flag in status reg (FE, OE, PE/DLE DETECT)	**Async: Force Break** 0 = Normal 1 = Force break **Sync Send DLE** 0 = Normal 1 = Send DLE	0 = Disable 1 = Enable	0 = Force $\overline{DTR}$ output high 1 = Force $\overline{DTR}$ output low	0 = Disable 1 = Enable

Table 8. Status Register (SR)

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
Data Set Ready	**Data Carrier Detect**	**FE/SYN Detect**	**Overrun**	**PE/DLE Detect**	**TxEMT/ DSCHG**	**RxRDY**	**TxRDY**
0 = $\overline{DSR}$ input is high 1 = $\overline{DSR}$ input is low	0 = $\overline{DCD}$ input is high 1 = $\overline{DCD}$ input is low	**Async:** 0 = Normal 1 = Framing ERROR **Sync:** 0 = Normal 1 = SYN char detected	0 = Normal 1 = Overrun error	**Async:** 0 = Normal 1 = Parity error **Sync:** 0 = Normal 1 = Parity error or DLE char received	0 = Normal 1 = Change in $\overline{DSR}$ or $\overline{DCD}$, or transmit shift register is empty	0 = Receive holding register empty 1 = Receive holding register has data	0 = Transmit holding register busy 1 = Transmit holding register empty

Command Register (CR)

Table 7 illustrates the command register. Bits CR0 (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. A 0 to 1 transition of CR2 forces start bit search (async mode) or hunt mode (sync mode) on the second $\overline{RxC}$ rising edge. Disabling the receiver causes $\overline{RxRDY}$ to go high (inactive). If the transmitter is disabled, it will complete the transmission of the character in the transmit shift register (if any) prior to terminating operation. The TxD output will then remain in the marking state (high) while $\overline{TxRDY}$ and $\overline{TxEMT}$ will go high (inactive). If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be neglected.

Bits CR1 (DTR) and CR5 (RTS) control the $\overline{DTR}$ and $\overline{RTS}$ outputs. Data at the outputs is the logical complement of the register data.

In asynchronous mode, setting CR3 will force and hold the TxD output low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The TxD line will go high for at least one bit time before beginning transmission of the next character in the transmit data holding register. In synchronous mode, setting CR3 causes the transmission of the DLE register contents prior to sending the character in the transmit data holding register. CR3 should be reset in response to the next TxRDY.

Setting CR4 causes the error flags in the status register (SR3, SR4, and SR5) to be cleared. This is a one time command. There is no internal latch for this bit.

The PCI can operate in one of four submodes within each major mode (synchronous or asynchronous). The operational submode is determined by CR7 and CR6. CR7 – CR6 = 00 is the normal mode, with the transmitter and receiver operating independently in accordance with the mode and status register instructions.

In asynchronous mode, CR7 – CR6 = 01 places the PCI in the automatic echo mode. Clocked,

regenerated received data are automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2 = 1), but the transmitter need not be enabled. CPU to receiver communications continues normally, but the CPU to transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected.

The following conditions are true while in automatic echo mode:

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. $\overline{TxRDY}$ output = **1.**
4. The $\overline{TxEMT/DSCHG}$ pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In synchronous mode, CR7 – CR6 = 01 places the PCI in the automatic SYN/DLE stripping mode. The exact action taken depends on the setting of bits MR17 and MR16:

1. In the non-transparent, single SYN mode (MR17 – MR16 = 10), characters in the data stream matching SYN1 are not transferred to the receive data holding register (RHR).
2. In the non-transparent, double SYN mode (MR17 – MR16 = 00), characters in the data stream matching SYN1, or SYN2 if immediately preceded by SYN1, are not transferred the RHR. However, only the first SYN1 of an SYN1 – SYN1 pair is stripped.
3. In transparent mode (MR16 = 1), character in the data stream matching DLE, or SYN1 if immediately preceded by DLE, are not transferred to the RHR. However, only the first DLE of a DLE–DLE pair is stripped.

Note that automatic stripping mode does not affect the setting of the DLE detect and SYN detect status bits (SR3 and SR5).

Two diagnostic submodes can also be configured. In local loopback mode (CR7 – CR6 = 10), the following loops are connected internally:

1. The transmitter output is connected to the receiver input.
2. $\overline{DTR}$ is connected to $\overline{DCD}$ and $\overline{RTS}$ is connected to $\overline{CTS}$.
3. The receiver is clocked by the transmit clock.
4. The $\overline{DTR}$, $\overline{RTS}$ and $\overline{TxD}$ outputs are held high.
5. The $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ and RxD inputs are ignored.

Additional requirements to operate in the local loopback mode are that CR0 (TxEN), CR1 (DTR), and CR5 (RTS) must be set to 1. CR2 (RxEN) is ignored by the PCI.

The second diagnostic mode is the remote loopback mode (CR7 – CR6 = 11). In this mode:

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. No data is sent to the local CPU, but he error status conditions (PE, OE, FE) are set.
4. The $\overline{RxRDY}$, $\overline{TxRDY}$, and $\overline{TxEMT/DSCHG}$ outputs are held high.

5. CR0 (TxEN) is ignored.
6. All other signals operate normally.

Status Register

The data contained in the status register (as shown in Table 8) indicate receiver and transmitter conditions and modem/data set status.

SR0 is the transmitter ready (TxRDY) status bit. It, and its corresponding output, are valid only when the transmitter is enabled. If equal to 0, it indicates that the transmit data holding register has been loaded by the CPU and the data has not been transferred to the transmit shift register. If set equal to 1, it indicates that the Holding Register is ready to accept data from the CPU. This bit is initially set when the transmitter is enabled by CR0, unless a character has previously been loaded into the holding register. It is not set when the automatic echo or remote loopback modes are programmed. When this bit is set, the $\overline{\text{TxRDY}}$ output pin is low. In the automatic echo and remote loopback modes, the output is held high.

SR1, the receiver ready (RxRDY) status bit, indicates the condition of the receive data holding register. If set, it indicates that a character has been loaded into the holding register from the receive shift register and is ready to be read by the CPU. If equal to zero, there is no new character in the holding register. This bit is cleared when the CPU reads the receive data holding register or when the receiver is disabled by CR2. When set, the $\overline{\text{RxRDY}}$ output is low.

The TxEMT/DSCHG bit, SR2, when set, indicates either a change of state of the $\overline{\text{DSR}}$ or $\overline{\text{DCD}}$ inputs or that the transmit shift register has completed transmission of a character and no new character has been loaded into the transmit data holding register. Note that in synchronous mode this bit will be set even though the appropriate "fill" character is transmitted. TxEMT will not go active until at least one character has been transmitted. It is cleared by loading the transmit data holding register. The DSCHG condition is enabled when TxEN = 1 or RxEN = 1. If the status register is read twice and SR2 = 1 while SR6 and SR7 remain unchanged, then a TxEMT condition exists. It is cleared when the status register is read by the CPU. When SR2 is set, the $\overline{\text{TxEMT/DSCHG}}$ output is low.

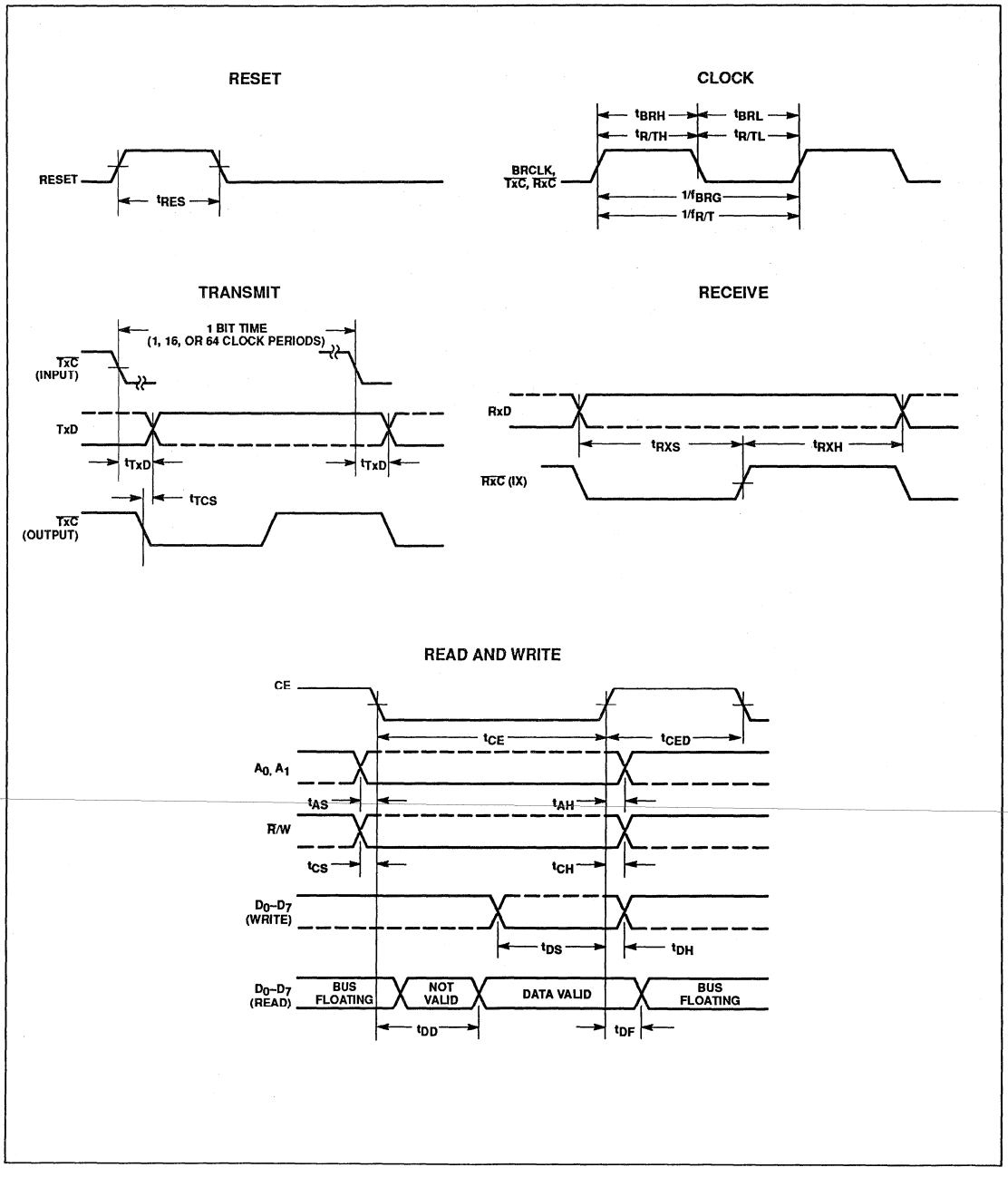
SR3, when set, indicates a received parity error when parity is enabled by MR14. In synchronous transparent mode (MR16 = 1), with parity disabled, it indicates that a character matching the DLE register has been received. However, only the first DLE of two successive DLEs will set SR3. This bit is cleared when the receiver is disabled and by the reset error command, CR4.

The overrun error status bit, SR4, indicates that the previous character loaded into the receive holding register was not read by the CPU at the time a new received character was transferred into it. This bit is cleared when the receiver is disabled and by the reset error command, CR4.

In asynchronous mode, bit SR5 signifies that the received character was not framed by the programmed number of stop bits. (If 1.5 stop bits are programmed, only the first stop bit is checked.) If RHR = 0 when SR5 = 1, a break condition is present. In synchronous non-transparent mode (MR16 = 0), it indicates receipt of the SYN1 character in single SYN mode or the SYN1 – SYN2 pair in double SYN mode. In synchronous transparent mode (MR16 = 1), this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1 – SYN2) and, after synchronization has been achieved, when a DLE–SYN1 pair is received. The bit is reset when the receiver is disabled, when the reset error command is given in asynchronous mode, and when the status register is read by the CPU in the synchronous mode.

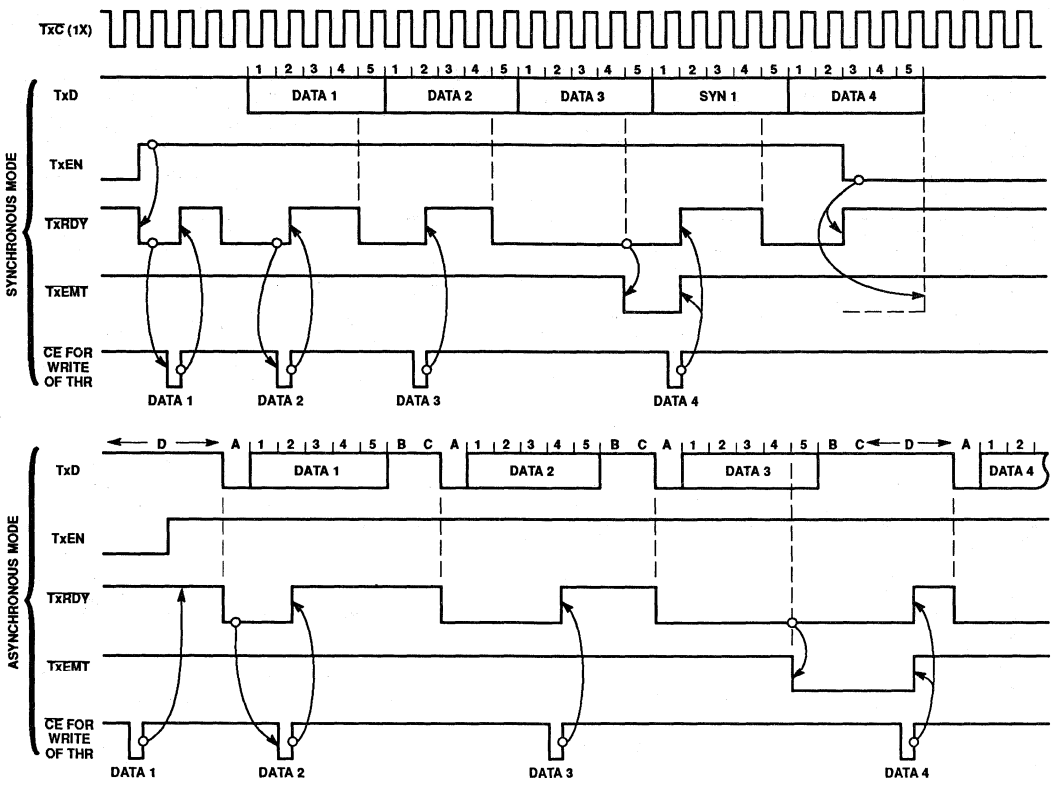
SR6 and SR7 reflect the conditions of the $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$ inputs respectively. A low input sets its corresponding status bit and a high input clears it.

TIMING DIAGRAMS



TIMING DIAGRAMS (Continued)

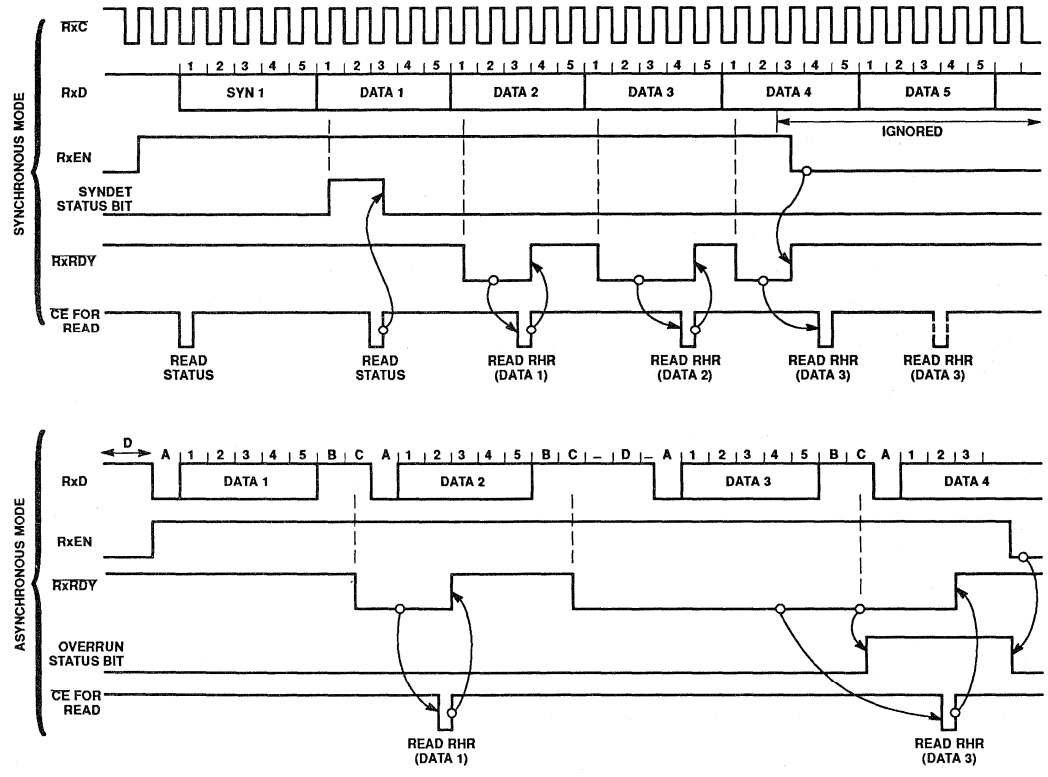
TxRDY, TxEMT (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])



NOTES:
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition
TxEMT goes low at the beginning of the last data bit, or, if parity is enabled, at the beginning of the parity bit.

TIMING DIAGRAMS (Continued)

RxRDY (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])

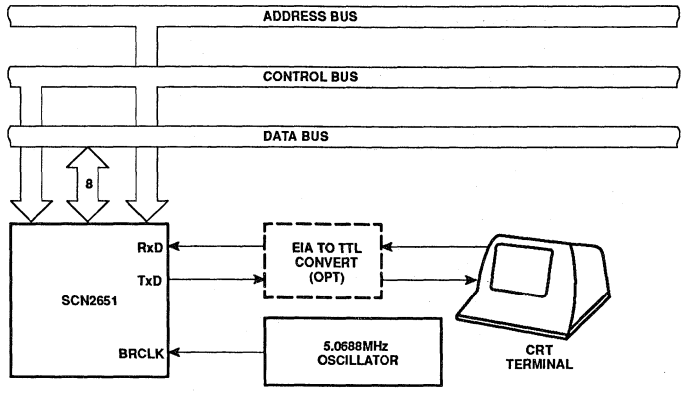


NOTES:

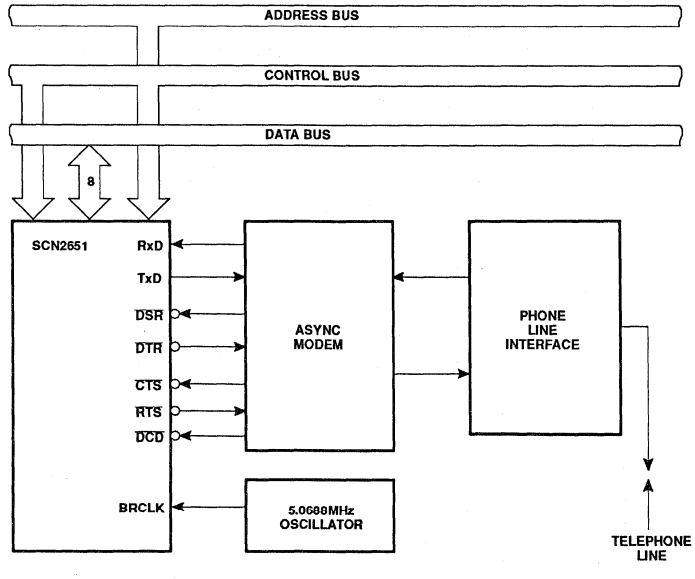
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition

TYPICAL APPLICATIONS

ASYNCHRONOUS INTERFACE TO CRT TERMINAL

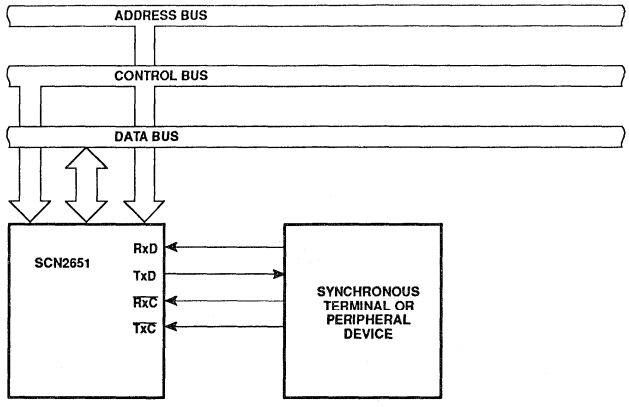


ASYNCHRONOUS INTERFACE TO TELEPHONE LINES

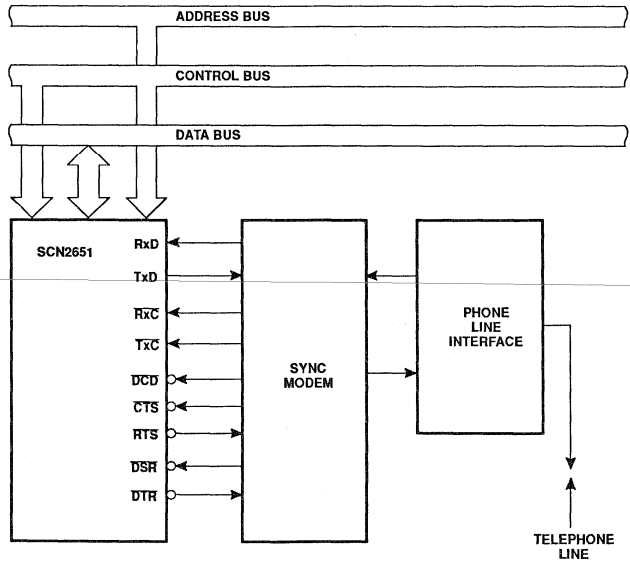


TYPICAL APPLICATIONS (Continued)

SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



SYNCHRONOUS INTERFACE TO TELEPHONE LINES



Multi-protocol communications controller (MPCC) SCN2652/SCN68652

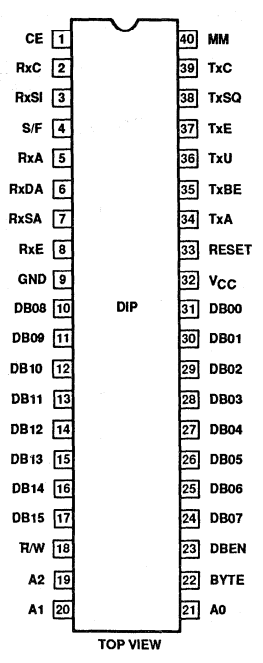
DESCRIPTION

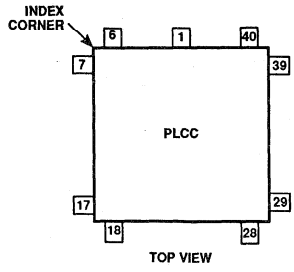
The SCN2652/68652 Multi-Protocol Communications Controller (MPCC) is a monolithic n-channel MOS LSI circuit that formats, transmits and receives synchronous serial data while supporting bit-oriented or byte control protocols. The chip is TTL compatible, operates from a single +5V supply, and can interface to a processor with an 8 or 16-bit bidirectional data bus.

FEATURES

- DC to 2Mbps data rate
- Bit-oriented protocols (BOP): SDLC, ADCCP, HDLC
- Byte-control protocols (BCP): DDCMP, BISYNC (external CRC)
- Programmable operation
  - 8 or 16-bit tri-state data bus
  - Error control – CRC or VRC or none
  - Character length – 1 to 8 bits for BOP or 5 to 8 bits for BCP
  - SYNC or secondary station address comparison for BCP-BOP
  - Idle transmission of SYNC/FLAG or MARK for BCP-BOP
- Automatic detection and generation of special BOP control sequences, i.e., FLAG, ABORT, GA
- Zero insertion and deletion for BOP
- Short character detection for last BOP data character
- SYNC generation, detection, and stripping for BCP
- Maintenance mode for self-testing
- TTL compatible
- Single +5V supply

PIN CONFIGURATION





Pin	Function	Pin	Function
1	NC	23	NC
2	CE	24	A0
3	RxC	25	BYTE
4	RxSI	26	DBEN
5	S/F	27	DB07
6	RxA	28	DB06
7	RxDA	29	DB05
8	RxSA	30	DB04
9	RxE	31	DB03
10	GND	32	DB02
11	DB08	33	DB01
12	NC	34	NC
13	DB09	35	DB00
14	DB10	36	V_{CC}
15	DB11	37	RESET
16	DB12	38	TxA
17	DB13	39	TxBE
18	DB14	40	TxU
19	DB15	41	TxE
20	R/W	42	TxSQ
21	A2	43	TxC
22	A1	44	MM

NOTE: 00 is least significant bit, highest number (that is, DB15, A2) is most significant bit.

APPLICATIONS

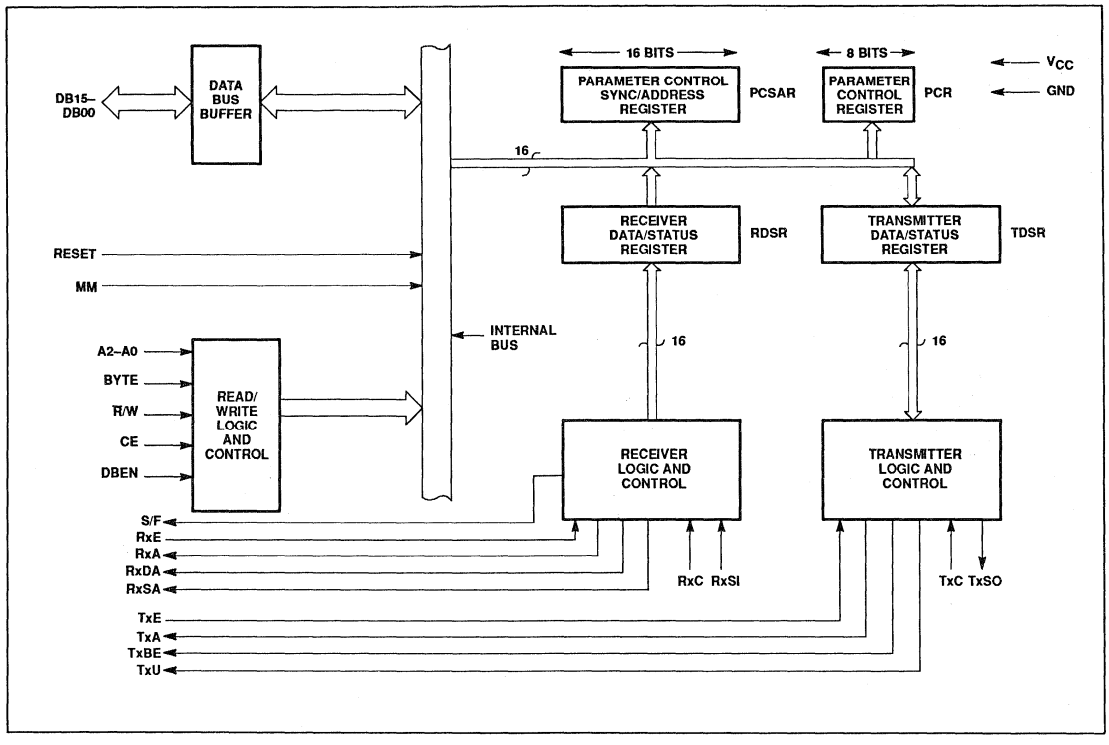
- Intelligent terminals
- Line controllers
- Network processors
- Front end communications
- Remote data concentrators
- Communication test equipment
- Computer to computer links

ORDERING CODE

PACKAGES		V_{CC} = 5V ±5%	
		Commercial	Automotive
		0°C to +70°C	–40°C to +85°C
Ceramic DIP	2MHz	SCN2652AC2F40	
Plastic DIP	2MHz	SCN2652AC2N40	Contact Factory
Plastic LCC	2MHz	SCN2652AC2A44	Contact Factory

NOTE:
SCN68652 is identical to SCN2652. Order using part numbers shown above.

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
DB15–DB00	17–10 24–31	I/O	**Data Bus:** DB07–DB00 contain bidirectional data while DB15–DB08 contain control and status information to or from the processor. Corresponding bits of the high and low order bytes can be wire OR'ed onto an 8-bit bus. The data bus is floating if either CE or DBEN are low.
A2–A0	19–21	I	**Address Bus:** A2–A0 select internal registers. The four 16-bit registers can be addressed on a word or byte basis. See Register Address section.
BYTE	22	I	**Byte:** Single byte (8-bit) data bus transfers are specified when this input is high. A low level specifies 16-bit data bus transfers.
CE	1	I	**Chip Enable:** A high input permits a data bus operation when DBEN is activated.
$\overline{R}$/W	18	I	**Read/Write:** $\overline{R}$/W controls the direction of data bus transfer. When high, the data is to be loaded into the addressed register. A low input causes the contents of the addressed register to be presented on the data bus.
DBEN	23	I	**Data Bus Enable:** After A2–A0, CE, BYTE and $\overline{R}$/W are set up, DBEN may be strobed. During a read, the 3-state data bus (DB) is enabled with information for the processor. During a write, the stable data is loaded into the addressed register and TxBE will be reset if TDSR was addressed.
RESET	33	I	**Reset:** A high level initializes all internal registers (to zero) and timing.
MM	40	I	**Maintenance Mode:** MM internally gates TxSO back to RxSI and TxC to RxC for off line diagnostic purposes. The RxC and RxSI inputs are disabled and TxSO is high when MM is asserted.
RxE	8	I	**Receiver Enable:** A high level input permits the processing of RxSI data. A low level disables the receiver logic and initializes all receiver registers and timing.
RxA	5	O	**Receiver Active:** RxA is asserted when the first data character of a message is ready for the processor. In the BOP mode this character is the address. The received address must match the secondary station address if the MPCC is a secondary station. In BCP mode, if strip-SYNC ($PCSAR_{13}$) is set, the first non-SYNC character is the first data character; if strip-SYNC is zero, the character following the second SYNC is the first data character. In the BOP mode, the closing FLAG resets RxA. In the BCP mode, RxA is reset by a low level at RxE.
RxDA*	6	O	**Receiver Data Available:** RxDA is asserted when an assembled character is in $RDSR_L$ and is ready to be presented to the processor. This output is reset when $RDSR_L$ is read.
RxC	2	I	**Receiver Clock:** RxC (1X) provides timing for the receiver logic. The positive going edge shifts serial data into the RxSR from RxSI.
S/F	4	O	**SYNC/FLAG:** S/F is asserted for one RxC clock time when a SYNC or FLAG character is detected.
RxSA*	7	O	**Receiver Status Available:** RxSA is asserted when there is a zero to one transition of any bit in $RDSR_H$ except for RSOM. It is cleared when $RDSR_H$ is read.
RxSI	3	I	**Receiver Serial Input:** RxSI is the received serial data. Mark = '1', space = '0'.
TxE	37	I	**Transmitter Enable:** A high level input enables the transmitter data path between $TDSR_L$ and TxSO. At the end of a message, a low level input causes TxSO = 1(mark) and TxA = 0 after the closing FLAG (BOP) or last character (BCP) is output on TxSO.
TxA	34	O	**Transmitter Active:** TxA is asserted after TSOM ($TDSR_8$) is set and TxE is raised. This output will reset when TxE is low and the closing FLAG (BOP) or last character (BCP) has been output on TxSO.
TxBE*	35	O	**Transmitter Buffer Empty:** TxBE is asserted when theTDSR is ready to be loaded with new control information or data. The processor should respond by loading theTDSR which resets TxBE.
TxU*	36	O	**Transmitter Underrun:** TxU is asserted during a transmit sequence when the service of TxBE has been delayed for one character time. This indicates the processor is not keeping up with the transmitter. Line fill depends on $PCSAR_{11}$. TxU is reset by RESET or setting of TSOM ($TDSR_8$), synchronized by the falling edge of TxC.
TxC	39	I	**Transmitter Clock:** TxC (1X) provides timing for the transmitter logic. The positive going edge shifts data out of the TxSR to TxSO.
TxSO	38	O	**Transmitter Serial Output:** TxSO is the transmitted serial data. Mark = '1', space = '0'.
V_{CC}	32	I	**+5V:** Power supply.
GND	9	I	**Ground:** 0V reference ground.

*Indicates possible interrupt signal

Table 1. Glossary

REGISTERS		NO. OF BITS	DESCRIPTION*
Addressable			
PCSAR	Parameter control sync/ address register	16	$PCSAR_H$ and PCR contain parameters common to the receiver and transmitter. $PCSAR_L$ contains a programmable SYNC character (BCP) or secondary station address (BOP).
PCR	Parameter control register	8	
RDSR	Receive data/status register	16	$RDSR_H$ contains receiver status information. $RDSR_L$ = RxDB contains the received assembled character.
TDSR	Transmit data/status register	16	$TDSR_H$ contains transmitter command and status information. TDSRL = TxDB contains the character to be transmitted
Internal			
CCSR	Control character shift register	8	These registers are used for character assembly (CSSR, HSR, RxSR), disassembly (TxSR), and CRC accumulation/generation (RxCRC, TxCRC).
HSR	Holding shift register	16	
RxSR	Receiver shift register	8	
TxSR	Transmitter shift register	8	
RxCRC	Receiver CRC accumulation register	16	
TxCRC	Transmitter CRC generation register	16	

NOTES:
*H = High byte – bits 15–8
L = Low byte – bits 7–0

FUNCTIONAL DESCRIPTION

The MPCC can be functionally partitioned into receiver logic, transmitter logic, registers that can be read or loaded by the processor, and data bus control circuitry. The register bit formats are shown in Figure 1 while the receiver and transmitter data paths are depicted in Figures 2 and 3.

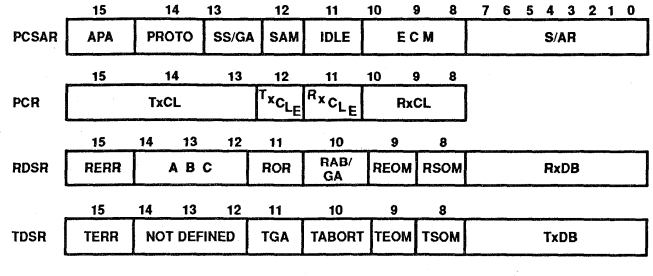
Table 2. Error Control

CHARACTER	DESCRIPTION
FCS	Frame check sequence is transmitted/received as 16 bits following the last data character of a BOP message. The divisor is usually CRC–CCITT ($X^{16} + X^{12} + X^5 + 1$) with dividend preset to 1's but can be other wise determined by ECM. The inverted remainder is transmitter as the FCS.
BCC	Block check character is transmitted/received as two successive characters following the last data character of a BCP message. The polynomial is CRC–16 ($X^{16} + X^{15} + X^2 + 1$) or CRC–CCITT with dividend preset to 0's (as specified by ECM). The true remainder is transmitted as the BCC.

Table 3. Special Characters

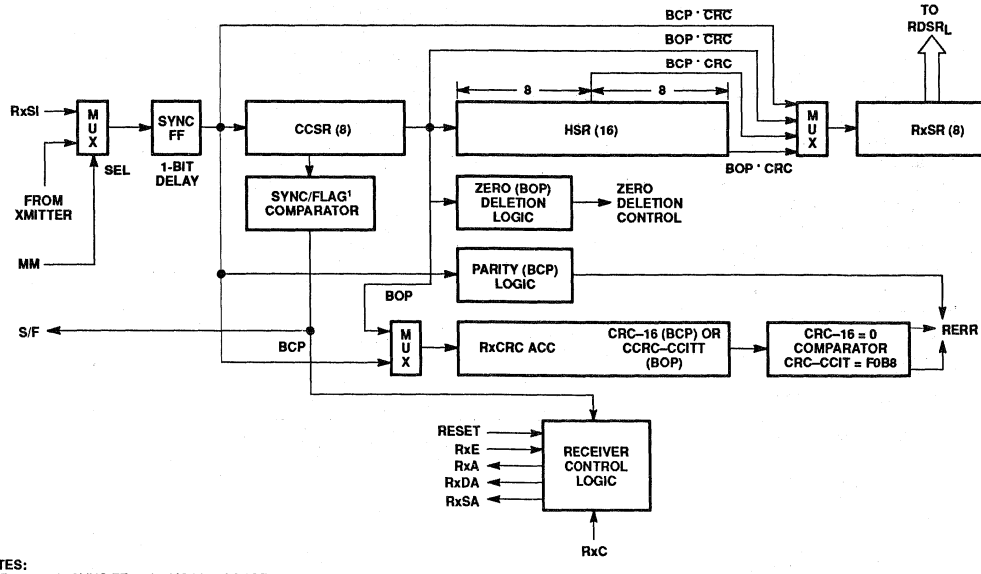
OPERATION	BIT PATTERN	FUNCTION
BOP		
FLAG	0 1 1 1 1 1 1 0	Frame message
ABORT	1 1 1 1 1 1 1 1 generation 0 1 1 1 1 1 1 1 detection	Terminate communication
GA	0 1 1 1 1 1 1 1	Terminate loop mode repeater function
Address	$(PCSAR_L)^1$	Secondary station address
BCP		
SYNC	$(PCSAR_L)$ or $(TxDB)^2$ generation	Character synchronization

NOTES:
1. ( ) = contents of.
2. For IDLE = 0 or 1 respectively.



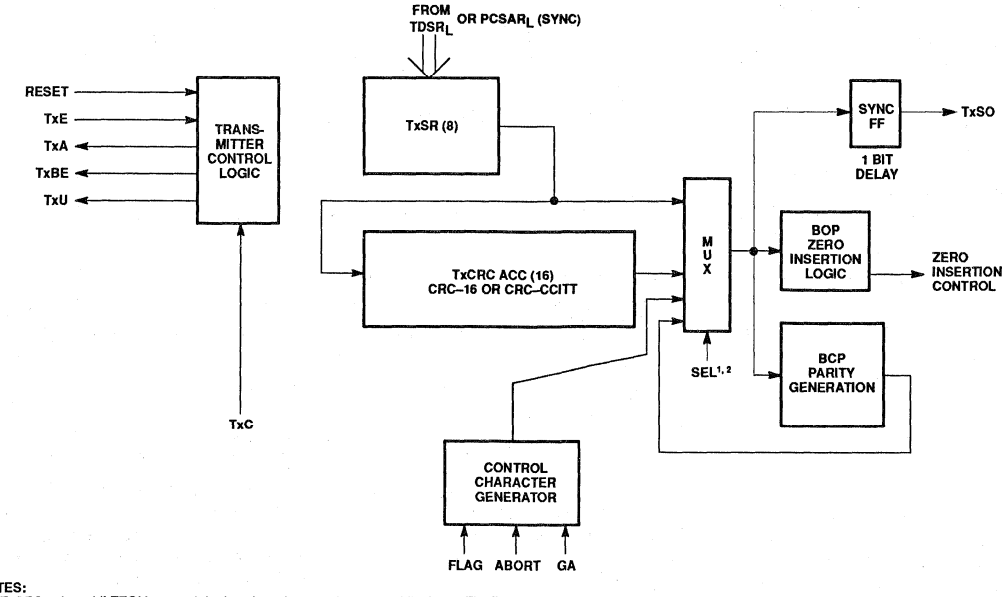
NOTE:
Refer to Register Formats for mnemonics and description.

Figure 1. Short Form Register Bit Formats



NOTES:
1. Detected in SYNC FF and 7 MS bits of CCSR.
2. In BOP mode, a minimum of two data characters must be received to turn the receiver active.

Figure 2. MPCC Receiver Data Path



NOTES:
1. TxCRC selected if TEOM = 1 and the last data character has been shifted out ofTxSR.
2. In BCP parity selected will be generated after each character is shifted out of TxSR.

Figure 3. MPCC Transmitter Data Path

RECEIVER OPERATION

General

After initializing the parameter control registers (PCSAR and PCR), the RxE input must be set high to enable the receiver data path. The serial data on the RxSI is synchronized and shifted into an 8-bit Control Character Shift Register (CCSR) on the rising edge of RxC. A comparison between CCSR contents and the FLAG (BOP) or SYNC (BCP) character is made until a match is found. At that time, the S/F output is asserted for one RxC time and the 16-bit Holding Shift Register (HSR) is enabled. The receiver then operates as described below.

BOP Operation

A flowchart of receiver operation in BOP mode appears in Figure 4. Zero deletion (after five ones are received) is implemented on the received serial data so that a data character will not be interpreted as a FLAG, ABORT, or GA. Bits following the FLAG are shifted through the CCSR, HSR, and into the Receiver Shift Register (RxSR). A character will be assembled in the RxSR and transferred to the $RDSR_L$ for presentation to the processor. At that time the RxDA output will be asserted and the processor must take the character no later than one RxC time after the next character is assembled in the RxSR. If not, an overrun ($RDSR_{11}$ = 1) will occur and succeeding characters will be lost.

The first character following the FLAG is the secondary station address. If the MPCC is a secondary station ($PCSAR_{12}$ = 1), the contents of RxSR are compared with the address stored in $PCSAR_L$. A match indicates the forthcoming message is intended for the station; the RxA output is asserted, the character is loaded into $RDSR_L$, RxDA is asserted and the Receive Start of Message bit (RSOM) is set. No match indicates that another station is being addressed and the receiver searches for the next FLAG.

If the MPCC is a primary station, ($PCSAR_{12}$ = 0), no secondary address check is made; RxA is asserted and RSOM is set once the first non-FLAG character has been loaded into $RDSR_L$ and RxDA has been asserted. Extended address field can be supported by software if $PCSAR_{12}$ = 0.

When the 8 bits following the address character have been loaded into $RDSR_L$ and RxDA has been asserted, RSOM will be cleared. The processor should read this 8-bit character and interpret it as the Control field.

Received serial data that follows is read and interpreted as the information field by the processor. It will be assembled into character

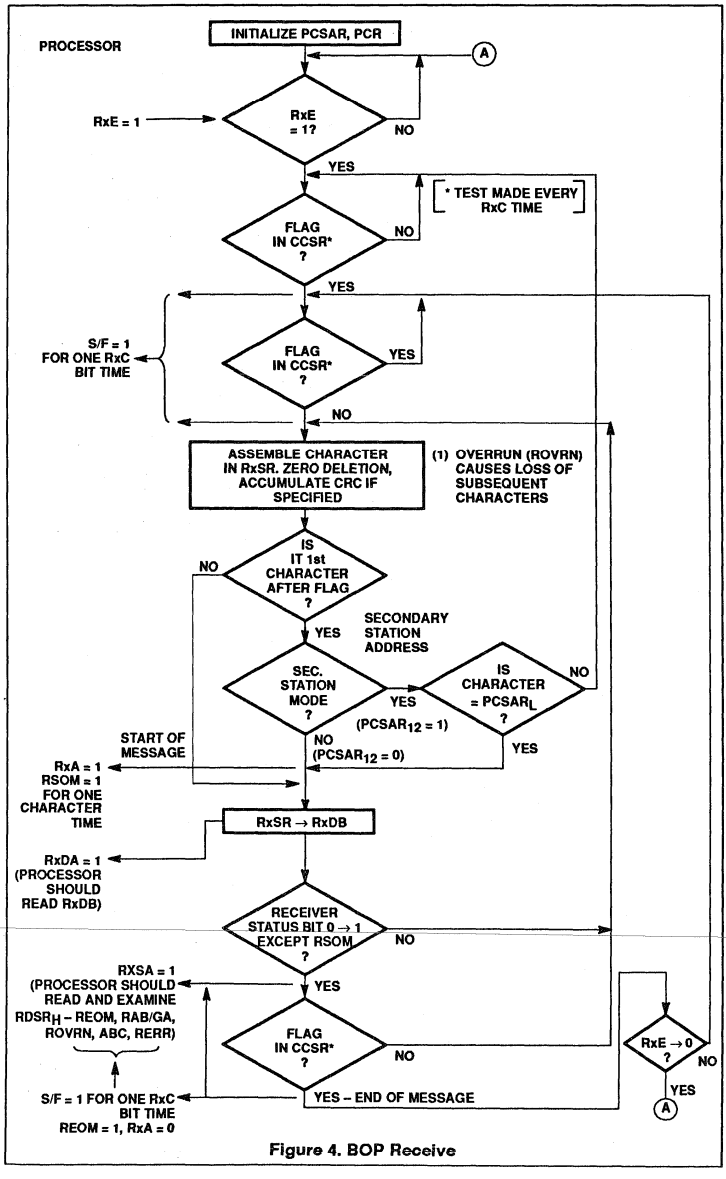


Figure 4. BOP Receive

lengths as specified by PCR_{8-10}. As before, RxDA is asserted each time a character has been transferred into $RDSR_L$ and is cleared

when $RDSR_L$ is read by the processor. $RDSR_H$ should only be read when RxSA is asserted. This occurs on a zero to one transition of any bit in $RDSR_H$ except for RSOM. RxSA and all bits in $RDSR_H$ except RSOM are cleared when $RDSR_H$ is read. The processor should check $RDSR_{9-15}$ each time RxSA is asserted. If $RDSR_9$ is set, then $RDSR_{12-15}$ should be examined.

Receiver character length may be changed dynamically in response to RxDA: read the character in RxDB and write the new

character length into RxCL. The character length will be changed on the next receiver character boundary. A received residual (short) character will be transferred into RxDB after the previous character in RxDB has been read, i.e. there will not be an overrun. In general the last two characters are protected from overrun.

The CRC–CCITT, if specified by $PCSAR_{8-10}$, is accumulated in RxCRC on each character following the FLAG. When the closing FLAG is detected in the CCSR, the received CRC is in the 16-bit HSR. At that time, the Receive End of Message bit (REOM) will be set; RxSA and RxDA will be asserted. The processor should read the last data character in $RDSR_L$ and the receiver status in $RDSR_{9-15}$. If $RDSR_{15} = 1$, there has been a transmission error; the accumulated CRC–CCITT is incorrect. If $RDSR_{12-14} \neq 0$, last data character is not of prescribed length. Neither the received CRC nor closing FLAG are presented to the processor. The processor may drop RxE or leave it active at the end of the received message.

BCP Operation

The operation of the receiver in BCP mode is shown in Figure 5. The receiver initially searches for two successive SYNC characters, of length specified by PCR_{8-10}, that match the contents of $PCSAR_L$. The next non-SYNC character or next SYNC character, if stripping is not specified ($PCSAR_{13} = 0$), causes RxA to be asserted and enables the receiver data path. Once enabled, all characters are assembled in RxSR and loaded into $RDSR_L$. RxDA is active when a character is available in $RDSR_L$. RxSA is active on a 0 to 1 transition of any bit in $RDSR_H$. The signals are cleared when RDSRl or $RDSR_H$ are read respectively.

If CRC–16 error control is specified by $PCSAR_{8-10}$, the processor must determine the last character received prior to the CRC field. When that character is loaded into $RDSR_L$ and RxDA is asserted, the received CRC will be in CCSR and HSR_L. To check for a transmission error, the processor must read the receiver status ($RDSR_H$) and examine $RDSR_{15}$. This bit will be set for one character time if an error free message has been received. If $RDSR_{15} = 0$, the CRC–16 is in error. The state of $RDSR_{15}$ in BCP CRC mode does not set RxSA. Note that this bit should be examined only at the end of a message. The accumulated CRC will include all characters starting with the first non-SYNC character if $PCSAR_{13} = 1$, or the character after the opening two SYNCs if $PCSAR_{13} = 0$. This necessitates external CRC generation/checking when supporting IBM's BISYNC. This can be accomplished using the Signetics SCN2653 Polynomial Generator/Checker. See Typical Applications.

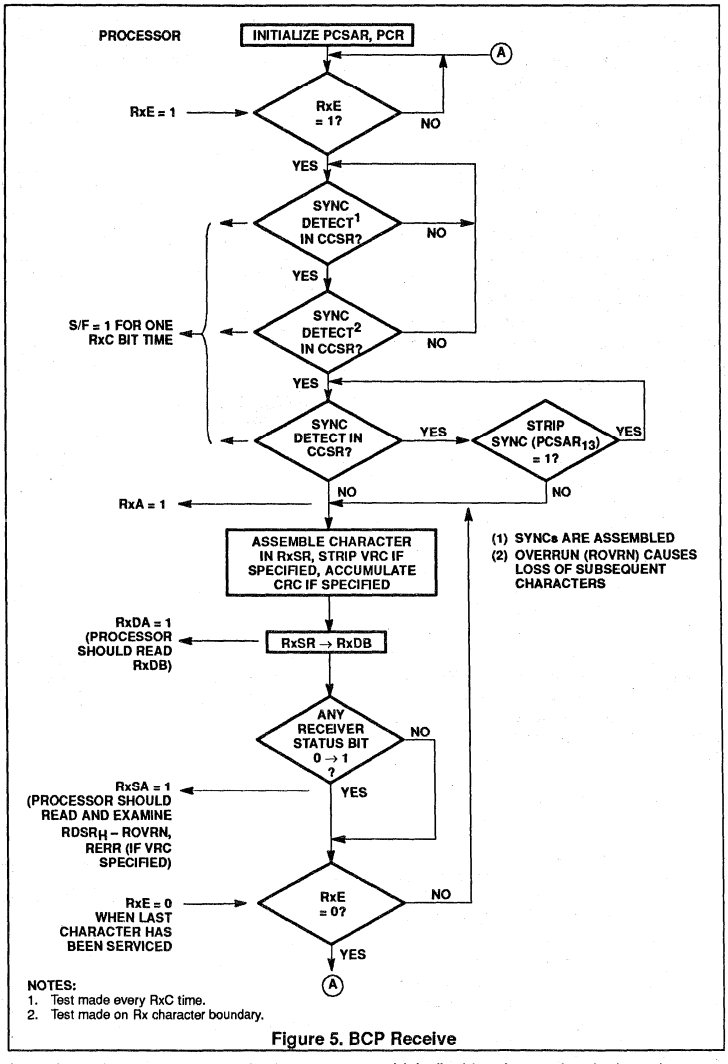


Figure 5. BCP Receive

If VRC has been selected for error control, parity (odd or even) is regenerated on each character and checked when the parity bit is received. A discrepancy causes $RDSR_{15}$ to be set and RxSA to be asserted. This must be sensed by the processor. The received parity bit is stripped before the character is presented to the processor.

When the processor has read the last character of the message, it should drop RxE which disables the receiver logic and initializes all receiver registers and timing.

TRANSMITTER OPERATION

General

After the parameter control registers (PCSAR and PCR) have been initialized, TxSO is held at mark until TSOM ($TDSR_8$) is set and TxE is raised. Then, transmitter operation depends on protocol mode.

BOP Operation

Transmitter operation for BOP is shown in Figure 6. A FLAG is sent after the processor sets the Transmit Start of Message bit (TSOM) and raises TxE. The FLAG is used to synchronize the message that follows. TxA will also be asserted. When TxBE is asserted by the MPCC, the processor should load $TDSR_L$ with the first character of the message. TSOM should be cleared at the same time $TDSR_L$ is loaded (16-bit data bus) or immediately thereafter (8-bit data bus). FLAGS are sent as long as TSOM = 1. For counting the number of FLAGs, the processor should reassert TSOM in response to the assertion of TxBE.All succeeding characters are loaded into $TDSR_L$ by the processor when TxBE = 1. Each

character is serialized in TxSR and transmitted on TxSO. Internal zero insertion logic stuffs a "0" into the serial bit stream after five successive "1s" are sent. This insures a data character will not match a FLAG, ABORT, or GA reserved control character. As each character is transmitted, the Frame Check Sequence (FCS) is generated as specified by Error Control Mode ($PCSAR_{8-10}$). The FCS should be the CRC–CCITT polynomial ($X^{16} + X^{12} + X^5 + 1$) preset to 1s. If an underrun occurs (processor is not keeping up with the transmitter), TxU and TERR ($TDSR_{15}$) will be asserted with ABORT or FLAG used as the TxSO line fill depending on the state of IDLE ($PCSAR_{11}$). The processor must set TSOM to reset the underrun condition. To retransmit the message, the processor should proceed with the normal start of message sequence.

A residual character of 1 to 7 bits may be transmitted at the end of the information field. In response to TxBE, write the residual character length into TxCL and load TxDB with the residual character. Dynamic alteration of character length should be done in exactly the same sequence. The character length will be changed on the next transmit character boundary.

After the last data character has been loaded into $TDSR_L$ and sent to TxSR (TxBE = 1), the processor should set TEOM ($TDSR_9$). The MPCC will finish transmitting the last character followed by the FCS and the closing FLAG. The processor should clear TEOM and drop TxE when the next TxBE is asserted. This corresponds to the start of closing FLAG transmission. When TxE has been dropped. TxA will be low 1 1/2 bit times after the last bit of the closing FLAG has been transmitted. TxSO will be marked after the closing FLAG has been transmitted.

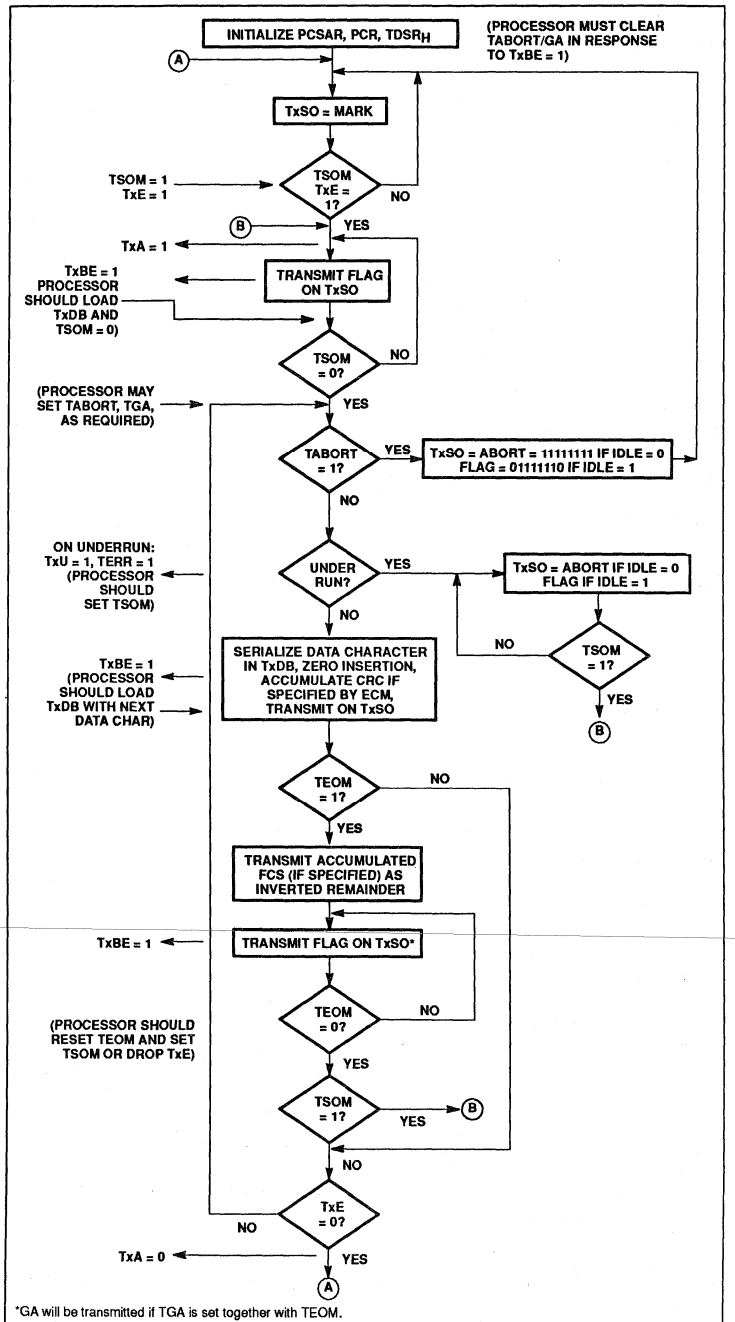


Figure 6. BOP Transmit

If TxE and TEOM are high, the transmitter continues to send FLAGs. The processor may initiate the next message by resetting TEOM and setting TSOM, or by loading $TDSR_L$ with a data character and then simply resetting TSOM (without setting TSOM).

BCP Operation

Transmitter operation for BCP mode is shown in Figure 7. TxA will be asserted after TSOM = 1 and TxE is raised. At that time SYNC characters are sent from $PCSAR_L$ or $TDSR_L$ (IDLE = 0 or 1) as long as TSOM = 1. TxBE is asserted at the start of transmission of the first SYNC character. For counting the number of SYNCs, the processor should reassert TSOM in response to the assertion of TxBE. When TSOM = 0 transmission is from $TDSR_L$, which must be loaded with characters from the processor each time TxBE is asserted. If this loading is delayed for more than one character time, an underrun results: TxU and TERR are asserted and the

TxSO line fill depend on IDLE ($PCSAR_{11}$). The processor must set TSOM and retransmit the message to recover. This is not compatible with IBM's BISYNC, so that the user must not underrun when supporting that protocol.

CRC–16, if specified by $PCSAR_{8-10}$, is generated on each character transmitted from $TDSR_L$ when TSOM =0. The processor must set TEOM = 1 after the last data character has been sent to TxSR (TxBE = 1). The MPCC will finish transmitting the last data character and the CRC–16 field before sending SYNC characters which are transmitted as long as TEOM = 1. If SYNCs are not desired after CRC–16 transmission, the processor should clear TEOM and lower TxE when the TxBE corresponding to the start of CRC–16 transmission is asserted. When TEOM = 0, the line is marked and a new message may be initiated by setting TSOM and raising TxE.

If VRC is specified, it is generated on each data character and the data character length must not exceed 7 bits. For software LRC or CRC, TEOM should be set only if SYNC's are required at the end of the message block.

Special Case

The capability to transmit 16 spaces is provided for line turnaround in half duplex mode or for a control recovery situation. This is achieved by setting TSOM and TEOM, clearing TEOM when TxBE = 1, and proceeding as required.

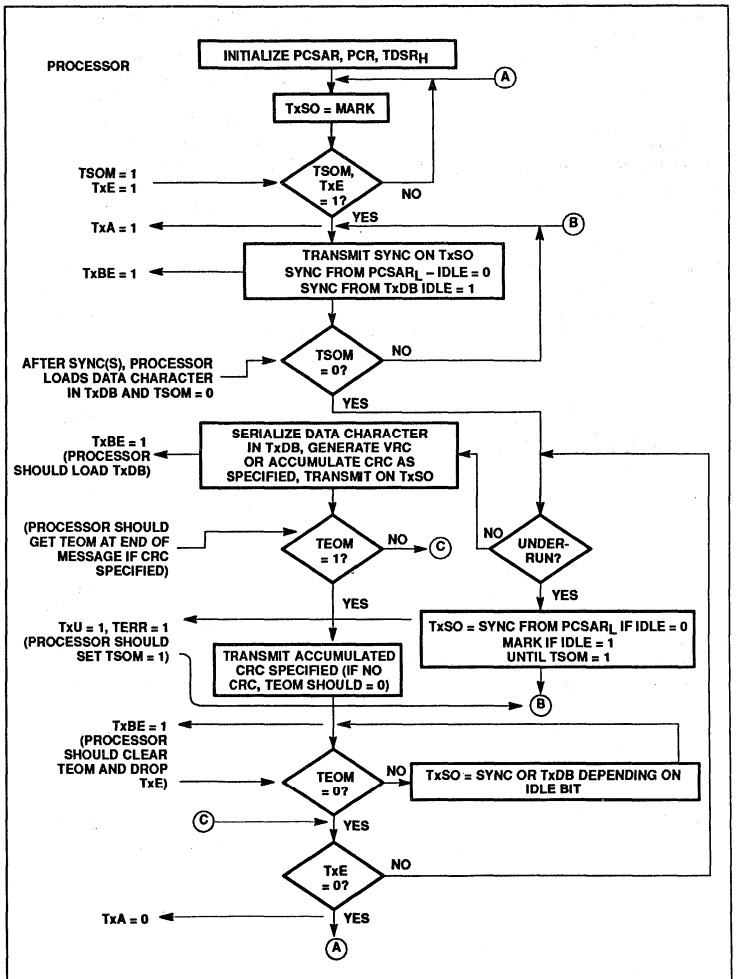


Figure 7. BCP Transmit

PROGRAMMING

Prior to initiating data transmission or reception, PCSAR and PCR must be loaded with control information from the processor. The contents of these registers (see Register Format section) will configure the MPCC for the user's specific data communication environment. These registers should be loaded during power-on initialization and after a reset operation. They can be changed at any time that the respective transmitter or receiver is disabled.

The default value for all registers is zero. This corresponds to BOP, primary station mode,
8-bit character length, FCS = CRC–CCITT preset to 1s.

For BOP mode the character length register (PCR) may be set to the desired values during system initialization. The address and control fields will automatically be 8-bits. If a residual character is to be transmitted, TxCL

should be changed to the residual character length prior to transmission of that character.

DATA BUS CONTROL

The processor must set up the MPCC register address (A2–A0), chip enable (CE), byte select (BYTE), and read/write ($\overline{R}$/W) inputs before each data bus transfer operation.

During a read operation ($\overline{R}$/W = 0), the leading edge of DBEN will initiate an MPCC read cycle. The addressed register will place its contents on the data bus. If BYTE = 1, the 8-bit byte is placed on DB15–08 or DB07–00 depending on the H/L status of the register addressed. Unused bits in $RDSR_L$ are zero. If BYTE = 0, all 16 bits (DB15–00) contain MPCC information. The trailing edge of DBEN will reset RxDA and/or RxSA if $RDSR_L$ or $RDSR_H$ is addressed respectively.

DBEN acts as the enable and strobe so that the MPCC will not begin its internal read cycle until DBEN is asserted.

During a write operation ($\overline{R}$/W = 1), data must be stable on DB_{15-08} and/or DB_{07-00} prior to the leading edge of DBEN. The stable data is strobed into the addressed register by DBEN. TxBE will be cleared if the addressed register was $TDSR_H$ or $TDSR_L$.

Table 4. MPCC Register Addressing

	A2	A1	A0	REGISTER
BYTE = 0	16-BIT DATA BUS = $DB_{15} - DB_{00}$			
	0	0	X	RDSR
	0	1	X	TDSR
	1	0	X	PCSAR
	1	1	X	PCR*
BYTE = 1	8-BIT DATA BUS = DB_{7-0} or DB_{15-8}**			
	0	0	0	$RDSR_L$
	0	0	1	$RDSR_H$
	0	1	0	$TDSR_L$
	0	1	1	$TDSR_H$
	1	0	0	$PCSAR_L$
	1	0	1	$PCSAR_H$
	1	1	0	PCR_L*
	1	1	1	PCR_H

NOTES:
* PCR lower byte does not exist. It will be all "0"s when read.
** Corresponding high and low order pins must be tied together.

Table 5. Parameter Control Register (PCR)–(R/W)

BIT	NAME	MODE	FUNCTION
00–07	Not Defined		
08–10	RxCL	BOP/BCP	Receiver character length is loaded by the processor when RxCLE = 0. The character length is valid after transmission of single byte address and control fields have been received.

10	9	8	Char length (bits)
0	0	0	8
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

11	RxCLE	BOP/BCP	Receiver character length enable should be zero when the processor loads RxCL. The remaining bits of PCR are not affected during loading. Always 0 when read.
12	TxCLE	BOP/BCP	Transmitter character length enable should be zero when the processor loads TxCL. The remaining bits of PCR are not affected during loading. Always 0 when read.
13–15	TxCL	BOP/BCP	Transmitter character length is loaded by the processor when TxCLe = 0. Character bit length specification format is identical to RxCL. It is valid after transmission of single byte address and control fields.

Table 6. Parameter Control SYNC/Address Register (PCSAR)–(R/W)

BIT	NAME	MODE	FUNCTION
00–07	S/AR	BOP	SYNC/address register. Contains the secondary station address if the MPCC is a secondary station. The contents of this register is compared with the first received non-FLAG character to determine if the message is meant for this station.
		BCP	SYNC character is loaded into this register by the processor. It is used for receive and transmit bit synchronization with bit length specified by RxCL and TxCL.
08–10	ECM	BOP/BCP	**Error Control Mode** / **10** / **9** / **8** / **Suggested Mode** / **Char. length** CRC–CCITT preset to 1's / 0 / 0 / 0 / BOP / 1–8 CRC–CCITT preset to 0's / 0 / 0 / 1 / BCP / 8 Not used / 0 / 1 / 0 / — / CRC–16 preset to 0's / 0 / 1 / 1 / BCP / 8 VRC odd / 1 / 0 / 0 / BCP / 5–7 VRC even / 1 / 0 / 1 / BCP / 5–7 Not used / 1 / 1 / 0 / — / No error control / 1 / 1 / 1 / BCP/BOP / 5–8 ECM should be loaded by the processor during initialization or when both data paths are idle.
11	IDLE		Determines line fill character to be used if transmitter underrun occurs (TxU asserted and TERR set) and transmission of special characters for BOP/BCP.
		BOP	IDLE = 0, transmit ABORT characters during underrun and when TABORT = 1. IDLE = 1, transmit FLAG characters during underrun and when TABORT = 1.
		BCP	IDLE = 0 transmit initial SYNC characters and underrun line fill characters from theS/AR. IDLE = 1 transmit initial SYNC characters from TxDB and marks TxSO during underrun.
12	SAM	BOP	Secondary Address Mode = 1 if the MPCC is a secondary station. This facilitates automatic recognition of the received secondary station address. When transmitting, the processor must load the secondary address into TxDB. SAM = 0 inhibits the received secondary address comparison which serves to activate the receiver after the first non-FLAG character has been received.
13	SS/GA		Strip SYNC/Go Ahead. Operation depends on mode.
		BOP	SS/GA = 1 is used for loop mode only and enables GA detection. When a GA is detected as a closing character, REOM and RAB/GA will be set and the processor should terminate the repeater function. SS/GA = 0 is the normal mode which enables ABORT detection. It causes the receiver to terminate the frame upon detection of an ABORT or FLAG.
		BCP	SS/GA = 1, causes the receiver to strip SYNC's immediately following the first two SYNC's detected. SYNC's in the middle of a message will not be stripped. SS/GA = 0, presents any SYNC's after the initial two SYNC's to the processor.
14	PROTO		Determines MPCC Protocol mode
		BOP BCP	PROTO = 0 PROTO = 1
15	APA	BOP	All parties address. If this bit is set, the receiver data path is enabled by an address field of '11111111' as well as the normal secondary station address.

Table 7. Transmit Data/Status Register (TDSR) (R/W except TDSR15)

BIT	NAME	MODE	FUNCTION
00–07	TxDB	BOP/BCP	Transmit data buffer. Contains processor loaded characters to be serialized in TxSR and transmitted on TxSO.
08	TSOM		Transmitter start of message. Set by the processor to initiate message transmission provided TxE = 1.
		BOP	TSOM = 1 generates FLAGs. When TSOM = 0 transmission is from TxDB and FCS generation (if specified) begins. FCS, as specified by $PCSAR_{8-10}$, should be CRC–CCITT preset to 1's.
		BCP	TSOM = 1 generates SYNCs from $PCSAR_L$ or transmits from TxDB for IDLE = 0 or 1 respectively. When TSOM = 0 transmission is from TxDB and CRC generation (if specified) begins.
09	TEOM		Transmit end of message. Used to terminate a transmitted message.
		BOP	TEOM = 1 causes the FCS and the closing FLAG to be transmitted following the transmission of the data character in TxSR. FLAGs are transmitted until TEOM = 0. ABORT or GA are transmitted if TABORT or TGA are set when TEOM = 1.
		BCP	TEOM = 1 causes CRC–16 to be transmitted (if selected) followed by SYNCs from $PCSAR_L$ or TxDB (IDLE = 0 or 1). Clearing TEOM prior to the end of CRC–16 transmission (when TxBE = 1) causes TxSO to be marked following the CRC–16. TxE must be dropped before a new message can be initiated. If CRC is not selected, TEOM should not be set.
10	TABORT	BOP	Transmitter abort = 1 will cause ABORT or FLAG to be sent (IDLE = 1 or 1) after the current character is transmitted. (ABORT = 11111111)
11	TGA	BOP	Transmit go ahead (GA) instead of FLAG when TEOM = 1. This facilitates repeater termination in loop mode. (GA = 01111111)
12–14	Not Defined		
15	TERR	Read only	Transmitter error = 1 indicates the TxDB has not been loaded in time (one character time–1/2 TxC period after TxBE is asserted) to maintain continuous transmission. TxU will be asserted to inform the processor of this condition. TERR is cleared by setting TSOM. See timing diagram.
		BOP	ABORT's or FLAG's are sent as fill characters (IDLE = 0 or 1)
		BCP	SYNC's or MARK's are sent as fill characters (IDLE = 0 or 1). For IDLE = 1 the last character before underrun is not valid.

Table 8. Receiver Data/Status Register (RDSR)–(Read Only)

BIT	NAME	MODE	FUNCTION
00–07	RxDB	BOP/BCP	Receiver data buffer. Contains assembled characters from the RxSR. If VRC is specified, the parity bit is stripped.
08	RSOM	BOP	Receiver start of message = 1 when a FLAG followed by a non-FLAG has been received and the latter character matches the secondary station if SAM = 1. RxA will be asserted when RSOM = 1. RSOM resets itself after one character time and has no affect on RxSA.
09	REOM	BOP	Receiver end of message = 1 when the closing FLAG is detected and the last data character is loaded into RxDB or when an ABORT/GA character is received. REOM is cleared on reading $RDSR_H$, reset operation, or dropping of RxE.
10	RAB/GA	BOP	Received ABORT or GA character = 1 when the receiver senses an ABORT character if SS/GA = 0 or a GA character if SS/GA = 1. RAB/GA is cleared on reading $RDSR_H$, reset operation, or dropping of RxE. A received abort does not set RxDA.
11	ROR	BOP/BCP	Receiver overrun = 1 indicates the processor has not read last character in the RxDB within one character time + 1/2 RxC period after RxDA is asserted. Subsequent characters will be lost. ROR is cleared on reading $RDSR_H$, reset operation, or dropping of RxE.
12–14	ABC	BOP	Assembled bit count. Specifies the number of bits in the last received data character of a message and should be examined by the processor when REOM = 1(RxDA and RxSA asserted). ABC = 0 indicates the message was terminated (by a flag or GA) on a character boundary as specified by PCR_{8-10}. Otherwise, ABC = number of bits in the last data character. ABC is cleared when $RDSR_H$ is read, reset operation, or dropping RxE. The residual character is right justified in $RDSR_L$.
15	RERR	BOP/BCP	Receiver error indicator should be examined by the processor when REOm = 1 in BOP, or when the processor determines the last data character of the message in BCP with CRC or when RxSA is set in BCP with VRC. CRC–CCITT preset to 1's/0's as specified by $PCSAR_{8-10}$: RERR = 1 indicates FCS error (CRC ≠ F0B8 or ≠ 0) RERR = 0 indicates FCS received correctly (CRC = F0B8 or = 0) CRC–16 preset to 0's on 8-bit characters specified by $PSCAR_{8-10}$: RERR = 1 indicates CRC–16 received correctly (CRC = 0). RERR = 0 indicates CRC–16 error (CRC≠0) VRC specified by $PCSAR_{8-10}$: RERR = 1 indicates VRC error RERR = 0 indicates VRC is correct.

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
T_A	Operating ambient temperature[2]	Note 4	°C
T_{STG}	Storage temperature	–65 to +150	°C
	Input or output voltages with respect to GND[3]	–0.3 to +15	V
V_{CC}	With respect to GND	–0.3 to +7	V

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over operating temperature range unless otherwise specified. See ordering code table for applicable temperature range and operating supply range.

DC ELECTRICAL CHARACTERISTICS[1, 2]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage						V
V_{IL}	Low				0.8	
V_{IH}	High		2.0			
Output voltage						V
V_{OL}	Low	I_{OL} = 1.6mA			0.4	
V_{OH}	High	I_{OH} = –100µA	2.4			
I_{CC}	Power supply current	V_{CC} = 5.25V, T_A = 0°C			150	mA
Leakage current						µA
I_{IL}	Input	V_{IN} = 0 to 5.25V			10	
I_{OL}	Output	V_{OUT} = 0 to 5.25V			10	
Capacitance						pF
C_{IN}	Input	V_{IN} = 0V, f = 1MHz			20	
C_{OUT}	Output	V_{OUT} = 0V, f = 1MHz			20	

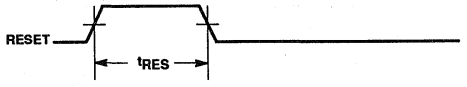
AC ELECTRICAL CHARACTERISTICS[1, 2, 3]

PARAMETER		2MHz CLOCK			UNIT
		Min	Typ	Max	
Set-up and hold time					ns
t_{ACS}	Address/control set-up	50			
t_{ACH}	Address/control hold	0			
t_{DS}	Data bus set-up (write)	50			
t_{DH}	Data bus hold (write)	0			
t_{RXS}	Receiver serial data set-up	150			
t_{RxH}	Receiver serial data hold	150			
Pulse width					ns
t_{RES}	RESET	250			
t_{DBEN}	DBEN	250		m[4]	
Delay Time					ns
t_{DD}	Data bus (read)			170	
t_{TxD}	Transmit serial data			250	
t_{DBEND}	DBEN to DBEN delay	200			
t_{DF}	Data bus float time (read)			150	ns
f	Clock (RxC, TxC) frequency			2.0	MHz
t_{CLK1}	Clock high (MM = 0)	165			ns
t_{CLK2}	Clock high (MM = 1)	240			
t_{CLK0}	Clock low	240			

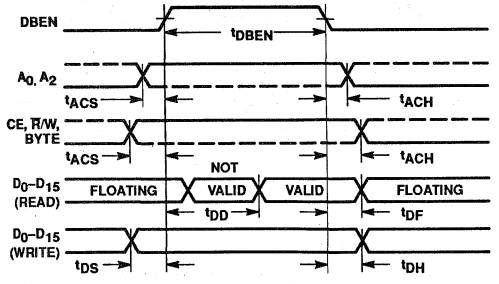
NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified. See ordering code table for applicable temperature range and operating supply range.
2. All voltage measurements are referenced to ground. All time measurements are at 0.8V or 2.0V. Input voltage levels for testing are 0.4V and 2.4V.
3. Output load C_L = 100pF.
4. m = TxC low and applies to writing to $TDSR_H$ only.

TIMING DIAGRAMS

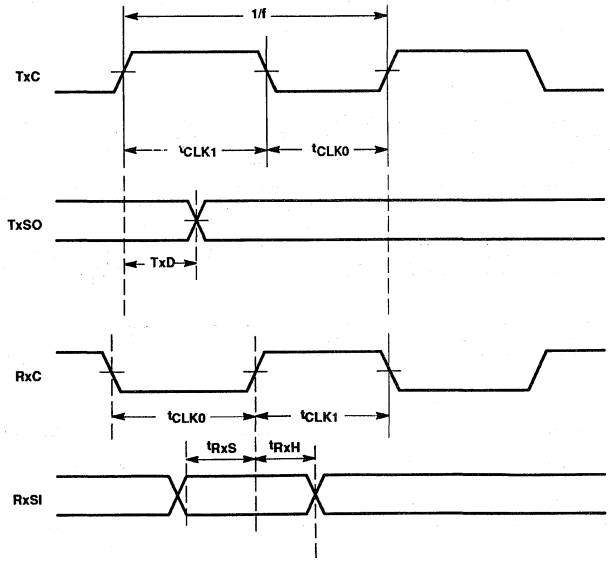
RESET



RESET AND WRITE DATA BUS

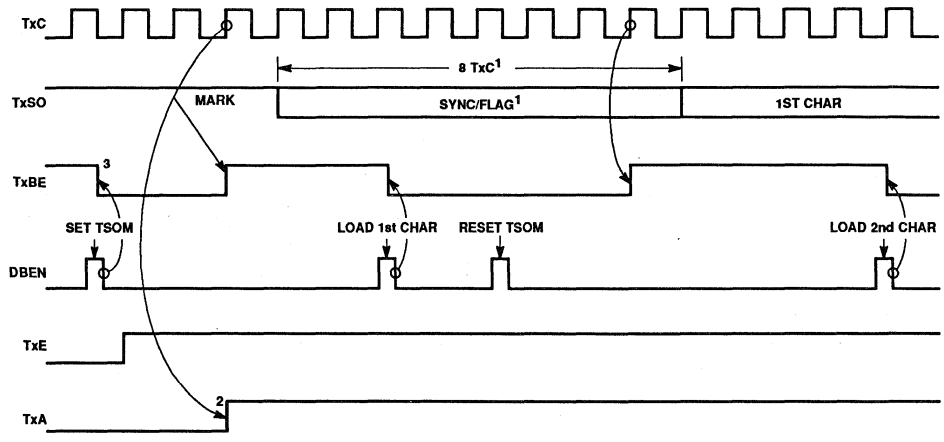


CLOCK



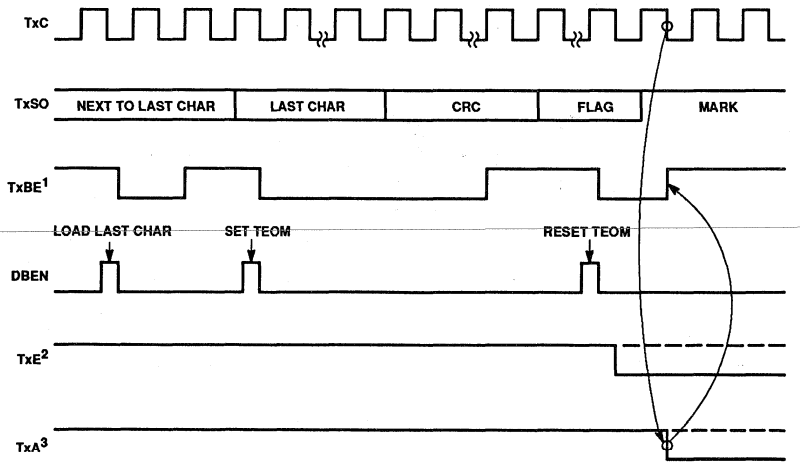
TIMING DIAGRAMS (CONTINUED)

TRANSMIT – START OF MESSAGE



NOTES:
1. SYNC may be 5 to 8 bits and will contain parity bit as specified.
2. TxA goes high relative to TxC rising edge after TSOM has been set and TxE has been raised.
3. TxBE goes low relative to DBEN falling edge on the first write transfer into TDSR. It is reasserted 1 TxC time before the first bit of the transmitted SYNC/FLAG. TxBE then goes low relative to DBEN falling edge when writing into $TDSR_H$ and/or $TDSR_L$. It is reasserted on the rising edge of the TxC that corresponds to the transmission of the last bit of each character, except in BOP mode when the CRC is to be sent as the next character (see Transmit Timing–End of Message).

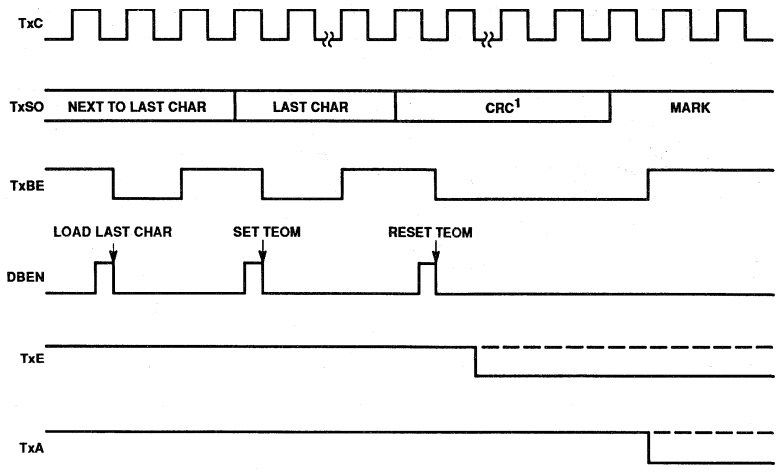
TRANSMIT – END OF BOP MESSAGE



NOTES:
1. TxBE goes low relative to the falling edge of DBEN corresponding to loading $TDSR_{H/L}$. It goes high one TxC before character transmission begins and also when TxA has been dropped.
2. TxE can be dropped before resetting TEOM if TxBE (corresponding to the closing FLAG) is high. Alternatively TxE can remain high and a new message initiated.
3. TxA goes low after TxE has been dropped and 1 1/2 TxC's after the last bit of the closing FLAG has been transmitted.

TIMING DIAGRAMS (CONTINUED)

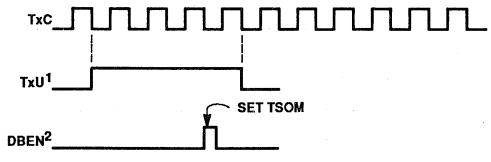
TRANSMIT TIMING – END OF BCP MESSAGE



NOTE:

1. When SCN2652 generated CRC is not required. TEOM should only be set if SYNCs are to follow the message block. In that case, TxE should be dropped in response to TxBE (which corresponds to the start of transmission of the last character). When CRC is required, TxE must be dropped before CRC transmission is complete. Otherwise, the contents of TxDB will be shifted out on TxSO. This facilitates transmission of contiguous messages.

TRANSMIT UNDERRUN

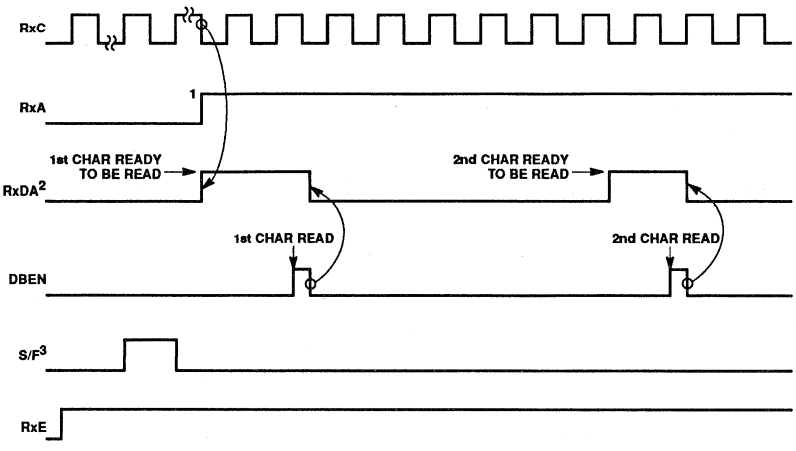


NOTES:

1. TxU goes active relative to TxC falling edge if TxBE has not been serviced after n-1/2 TxC times (where n = transmit character length). TxU is reset on the TxC falling edge following assertion of the TSOM command.
2. An underrun will occur at the next character boundary if TEOM is reset and the transmitter remains enabled, unless the TSOM command is asserted or a character is loaded into the TxDB.

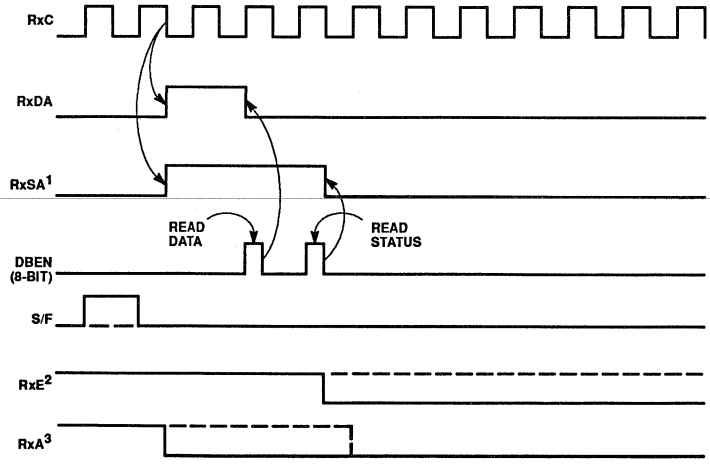
TIMING DIAGRAMS (CONTINUED)

RECEIVE – START OF MESSAGE



NOTES:
1. RxA goes high relative to falling edge of RxC when RxE is high and: a. A data character following two SYNC's is in RxDB (BCP mode). b. Character following FLAG is in RxDB (BOP primary station mode). c. Character following FLAG is in RxDB and character matches the secondary station address or all parties address (BOP secondary station mode).
2. RxDA goes high on RxC falling edge when a character in RxDB is ready to be read. It comes up before RxSA and goes low on the falling edge of DBEN when RxDB is read.
3. S/F goes high relative to rising edge of RxC anytime a SYNC (BCP) or FLAG (BOP) is detected.

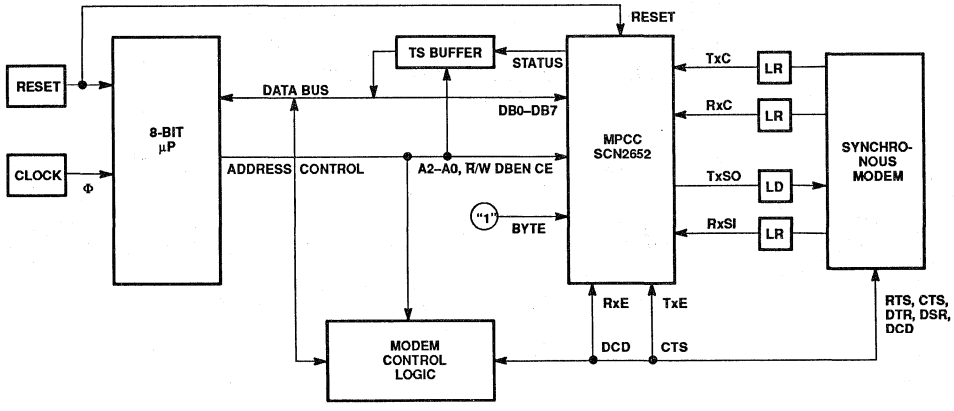
RECEIVE END OF MESSAGE



NOTES:
1. At the end of a BOP message, RxSA goes high when FLAG detection (S/F 1) forces REOm to be set. Processor should read the last data character ($RDSR_L$) and status ($RDSR_H$) which resets RxDA and RxSA respectively. For BCP end of message, RxSA may not be set and S/F = 0. The processor should read the last data character and status.
2. RxE must be dropped for BCP with non-contiguous messages. It may be left on at the end of a BOP message (see BOP Receive Operation).
3. RxA is reset relative to the falling edge of RxC after the closing FLAG of a BOP message (REOM = 1 and RxSA active.) or when RxE is dropped.

TYPICAL APPLICATIONS

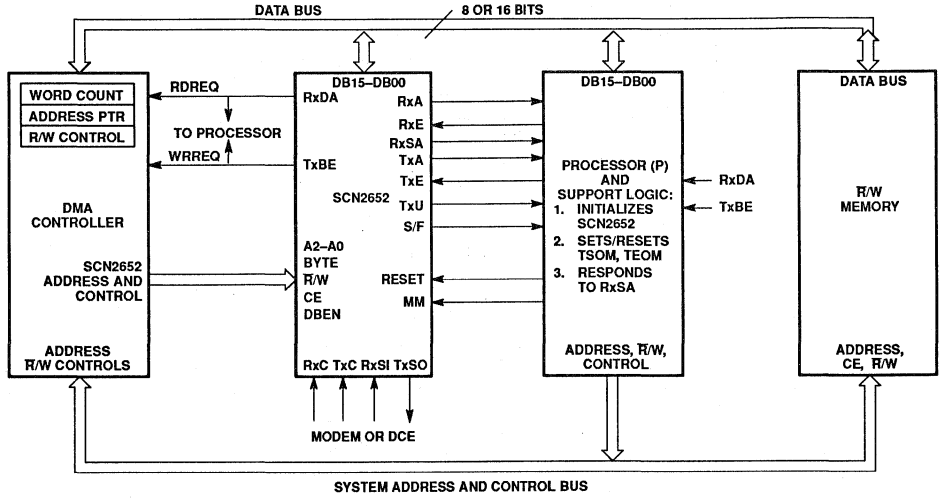
SCN2652 MPCC MICROPROCESSOR INTERFACE



NOTES:

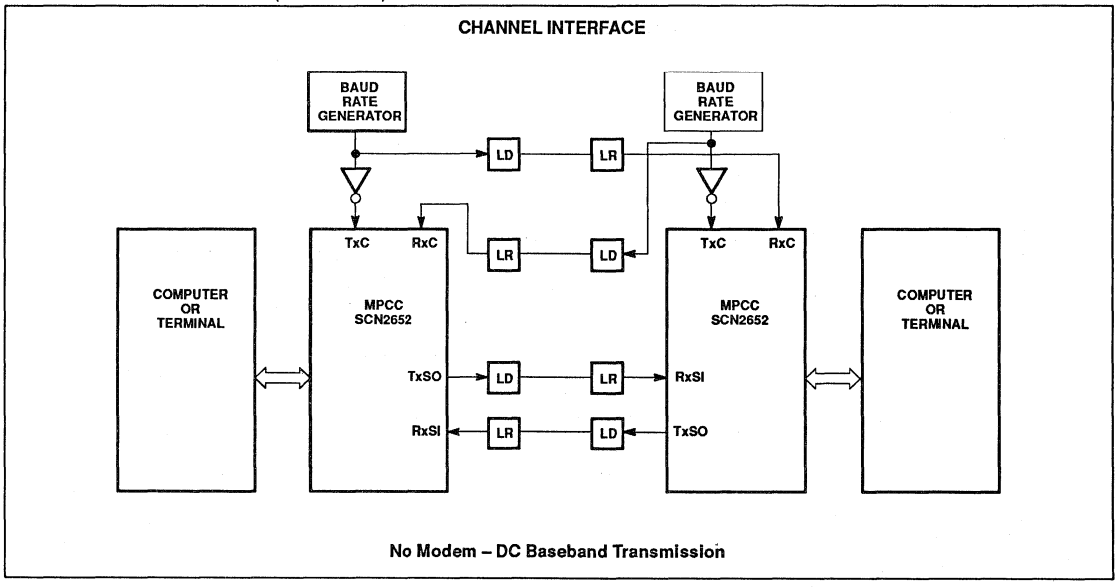
1. Possible µP interrupt requests are: RxDA RxSA TxBE TxU
2. Other SCN2652 status signals and possible uses are S F line idle indicator, frame delimiter. RxA handshake on RxE, line turn around control. TxA handshake on TxE, line turn around control.
3. Line drivers/receivers (LD/LR) convert EIA to TTL voltages and vice-versa.
4. RTS should be dropped after the CRC (BCP) or FLAG (BOP) has been transmitted. This forces CTS low and TxE low.
5. Corresponding high and low order bits of DB must be OR tied.

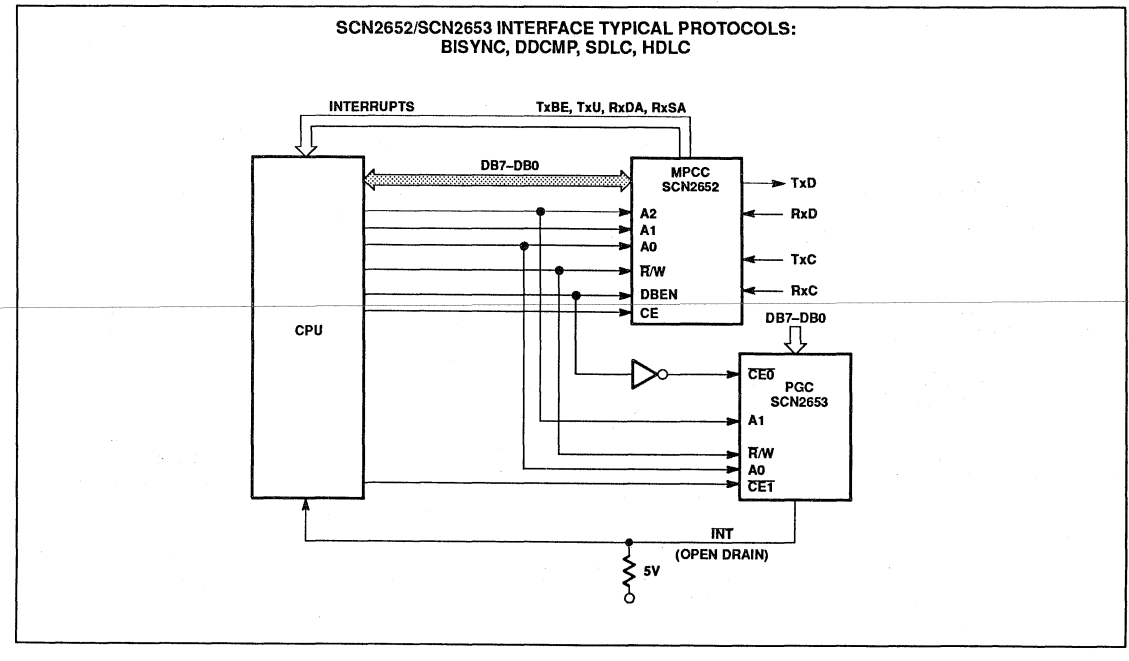
DMA/PROCESSOR INTERFACE



For non-DMA operation TxBE and RxDA are set to the processor which then loads or reads data characters as required.

TYPICAL APPLICATIONS (Continued)





Enhanced programmable communications interface (EPCI)

SCN2661/SCN68661

DESCRIPTION

The Signetics SCN2661 EPCI is a universal synchronous/asynchronous data communications controller chip that is an enhanced version of the SCN2651. It interfaces easily to all 8-bit and 16-bit microprocessors and may be used in a polled or interrupt driven system environment. The SCN2661 accepts programmed instructions from the microprocessor while supporting many serial data communications disciplines —synchronous and asynchronous — in the full- or half-duplex mode. Special support for BISYNC is provided.

The EPCI serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data characters for input to the microcomputer.

The SCN2661 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode. Each version of the EPCI (A, B, C) has a different set of baud rates.

FEATURES

- Synchronous operation
  - 5- to 8-bit characters plus parity
  - Single or double SYN operation
  - Internal or external character synchronization
  - Transparent or non-transparent mode
  - Transparent mode DLE stuffing (Tx) and detection (Rx)
  - Automatic SYN or DLE-SYN insertion SYN, DLE and DLESYN stripping
  - Odd, even, or no parity
  - Local or remote maintenance loopback mode
  - Baud rate: DC to 1Mbps (1X clock)
- Asynchronous operation
  - 5- to 8-bit characters plus parity
  - 1, 1-1/2 or 2 stop bits transmitted
  - Odd, even, or no parity
  - Parity, overrun and framing error detection
  - Line break detection and generation
  - False start bit detection
  - Automatic serial echo mode (echoplex)
  - Local or remote maintenance loopback mode
  - Baud rate: DC to 1Mbps
    (1X clock)
    DC to 62.5kbps (16X clock)
    DC to 15.625kbps
    (64X clock)

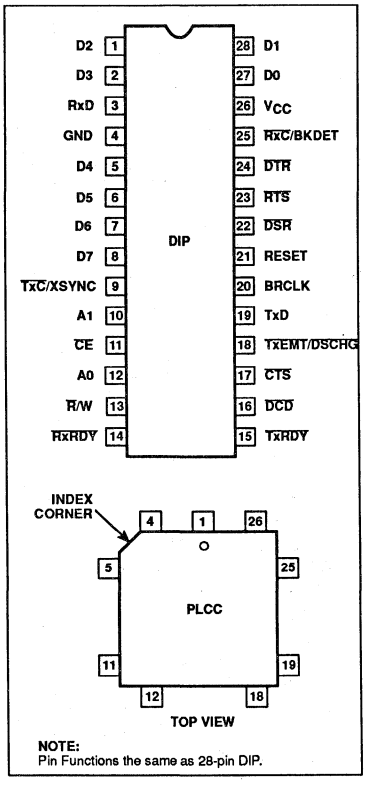
OTHER FEATURES

- Internal or external baud rate clock
- 3 baud rate sets
- 16 internal rates for each set
- Double-buffered transmitter and receiver
- Dynamic character length switching
- Full- or half-duplex operation
- TTL compatible inputs and outputs
- RxC and TxC pins are short-circuit protected
- Single +5V power supply
- No system clock required

APPLICATIONS

- Intelligent terminals
- Network processors
- Front-end processors
- Remote data concentrators
- Computer-to-computer links
- Serial peripherals
- BISYNC adaptors

PIN CONFIGURATIONS

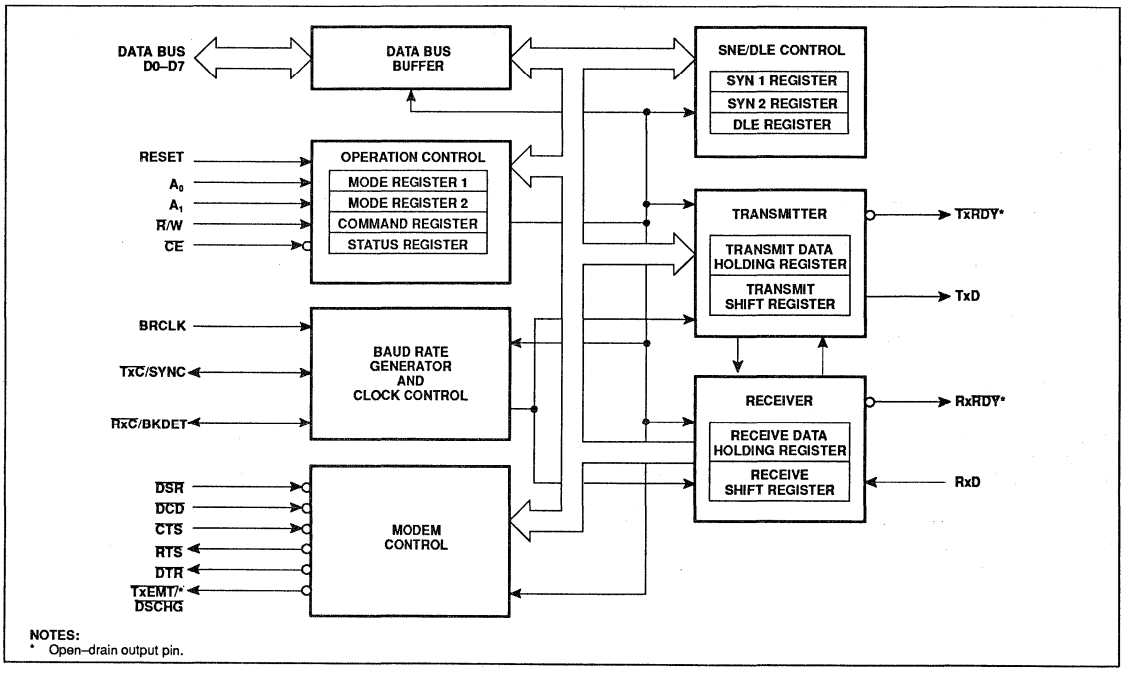


NOTE:
Pin Functions the same as 28-pin DIP.

ORDERING CODE

PACKAGES	V_{CC} = +5V ±5%	
	Commercial	Automotive
	0°C to +70°C	-40°C to +85°C
Ceramic DIP 28-Pin 0.6" Wide	SCN2661BC1F28 SCN2661CC1F28	SCN2661BA1F28 SCN2661CA1F28
Plastic DIP 28-Pin 0.6" Wide	SCN2661AC1N28 SCN2661BC1N28 SCN2661CC1N28	Contact Factory
Plastic LCC	SCN2661AC1A28 SCN2661BC1A28 SCN2661CC1A28	Contact Factory

BLOCK DIAGRAM



NOTES:
* Open–drain output pin.

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	Note 4	°C
Storage temperature	-65 to +150	°C
All voltages with respect to ground[3]	-0.5 to +6.0	V

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum function temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effect of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Over recommended free-air operating temperature range and supply voltage range unless otherwise specified. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
Output voltage						
V_{OL}	Low	I_{OL} = 2.2mA			0.4	V
V_{OH}[4]	High	I_{OH} = -400µA	2.4			V
I_{IL}	Input leakage current	V_{IN} = 0 to 5.5V			10	µA
3-State output leakage current						
I_{LH}	Data bus high	V_O = 4.0V			10	µA
I_{LL}	Data bus low	V_O = 0.45V			10	µA
I_{CC}	Power supply current				150	mA

NOTES:
1. Over recommended free-air operating temperature range and supply voltage range unless otherwise specified. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2. All voltages measurements are referenced to ground. All time measurements are at the 50% level for inputs (except t_{BRH} and t_{BRL}) and at 0.8V and 2.0V for outputs. Input levels swing between 0.4V and 2.4V, with a transition time of ≤ 20ns maximum.
3. Typical values are at +25°C, typical supply voltages and typical processing parameters.
4. $\overline{INTR}$, $\overline{TxRDY}$, $\overline{RxRDY}$ and $\overline{TxEMT/DSCHG}$ outputs are open-drain.

CAPACITANCE T_A = 25°C, V_{CC} = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Capacitance						
C_{IN}	Input				20	pF
C_{OUT}	Output	f_C = 1MHz			20	pF
$C_{I/O}$	Input/Output	Unmeasured pins tied to ground			20	pF

AC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
Pulse width						
t_{RES}	Reset		1000			ns
t_{CE}	Chip enable		250			ns
Setup and hold time						
t_{AS}	Address setup		10			ns
t_{AH}	Address hold		10			ns
t_{CS}	R/W control setup		10			ns
t_{CH}	R/W control hold		10			ns
t_{DS}	Data setup for write		150			ns
t_{DH}	Data hold for write		10			ns
t_{RXS}	RX data setup		300			ns
t_{RXH}	RX data hold		350			ns
t_{DD}	Data delay time for read	C_L = 150pF			200	ns
t_{DF}[7]	Data bus floating time for read	C_L = 150pF			100	ns
t_{CED}	CE to CE delay		600			ns
Input clock frequency						
f_{BRG}	Baud rate generator (2661A, B)		1.0	4.9152	4.9202	MHz
f_{BRG}	Baud rate generator (2661C)		1.0	5.0688	5.0738	MHz
$f_{R/T}$[6]	$\overline{TxC}$ or $\overline{RxC}$		dc		1.0	MHz
Clock width						
t_{BRH}[5]	Baud rate High (2661A, B)		75			ns
t_{BRH}[5]	Baud rate High (2661C)		70			ns
t_{BRL}[5]	Baud rate Low (2661A, B)		75			ns
t_{BRL}[5]	Baud rate Low (2661C)		70			ns
$t_{R/TH}$	$\overline{TxC}$ or $\overline{RxC}$ High		480			ns
$t_{R/TL}$[6]	$\overline{TxC}$ or $\overline{RxC}$ Low		480			ns
t_{TXD}	TxD delay from falling edge of $\overline{TxC}$	C_L = 150pF			650	ns
t_{TCS}	Skew between TxD changing and falling edge of $\overline{TxC}$ output[4]	C_L = 150pF		0		ns

NOTES:
1. Over recommended free-air operating temperature range and supply voltage range unless otherwise specified. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2. All voltages measurements are referenced to ground. All time measurements are at the 50% level for inputs (except t_{BRH} and t_{BRL}) and at 0.8V and 2.0V for outputs. Input levels swing between 0.4V and 2.4V, with a transition time of ≤ 20ns maximum.
3. Typical values are at +25°C, typical supply voltages and typical processing parameters.
4. Parameter applies when internal transmitter clock is used.
5. Under test conditions of 5.0688MHz f_{BRG} (68661) and 4.9152MHz f_{BRG} (68661A, B), t_{BRH} and t_{BRL} measured at V_{IH} and V_{IL}, respectively.
6. In asynchronous local loopback mode, using 1X clock, the following parameters apply: $f_{R/T}$ = 0.83MHz max and $t_{R/TL}$ = 700ns min.
7. See AC load conditions.

BLOCK DIAGRAM

The EPCI consists of six major sections. These are the transmitter, receiver, timing, operation control, modern control and SYN/DLE control. These sections communicate with each other via an internal data bus and an internal control bus. The internal data bus interfaces to the microprocessor data bus via a data bus buffer.

Operation Control

This functional block stores configuration and operation commands from the CPU and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with the microprocessor via the data bus and contains mode registers 1 and 2, the command register, and the status register. Details of register addressing and protocol are presented in the EPCI programming section of this data sheet.

Timing

The EPCI contains a Baud Rate Generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full-duplex operation. See Table 1.

Receiver

The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU.

Transmitter

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

Modem Control

The modem control section provides interfacing for three input signals and three output signals used for "handshaking" and status indication between the CPU and a modem.

SYN/DLE Control

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the CPU. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

Table 1. Baud Rate Generator Characteristics

68661A (BRCLK = 4.9152MHz)

MR23–20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	50	0.8kHz	—	6144
0001	75	1.2	—	4096
0010	110	1.7598	–0.01	2793
0011	134.5	2.152	—	2284
0100	150	2.4	—	2048
0101	200	3.2	—	1536
0110	300	4.8	—	1024
0111	600	9.6	—	512
1000	1050	16.8329	0.196	292
1001	1200	19.2	—	256
1010	1800	28.7438	–0.19	171
1011	2000	31.9168	–0.26	154
1100	2400	38.4	—	128
1101	4800	76.8	—	64
1110	9600	153.6	—	32
1111	19200	307.2	—	16

68661B (BRCLK = 4.9152MHz)

MR23–20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	45.5	0.7279kHz	0.005	6752
0001	50	0.8	—	6144
0010	75	1.2	—	4096
0011	110	1.7598	–0.01	2793
0100	134.5	2.152	—	2284
0101	150	2.4	—	2048
0110	300	4.8	—	1024
0111	600	9.6	—	512
1000	1200	19.2	—	256
1001	1800	28.7438	–0.19	171
1010	2000	31.9168	–0.26	154
1011	2400	38.4	—	128
1100	4800	76.8	—	64
1101	9600	153.6	—	32
1110	19200	307.2	—	16
1111	38400	614.4	—	8

68661C (BRCLK = 5.0688MHz)

MR23–20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	50	0.8kHz	—	6336
0001	75	1.2	—	4224
0010	110	1.76	—	2880
0011	134.5	2.1523	0.016	2355
0100	150	2.4	—	2112
0101	300	4.8	—	1056
0110	600	9.6	—	528
0111	1200	19.2	—	264
1000	1800	28.8	—	176
1001	2000	32.081	0.253	158
1010	2400	38.4	—	132
1011	3600	57.6	—	88
1100	4800	76.8	—	66
1101	7200	115.2	—	44
1110	9600	153.6	—	33
1111	19200	316.8	3.125	16

NOTE:
16X clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1X and BRG can be used only for TxC.

OPERATION

The functional operation of the 68661 is programmed by a set of control words supplied by the CPU. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc. The programming procedure is described in the EPCI programming section of the data sheet.

After programming, the EPCI is ready to perform the desired communications functions. The receiver performs serial to parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the CPU to a serial bit stream. These actions are accomplished within the framework specified by the control words.

Receiver

The 68661 is conditioned to receiver data when the $\overline{DCD}$ input is Low and the RxEN bit in the commands register is true. In the asynchronous mode, the receiver looks for High-to-Low (mark to space) transition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit-time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and one stop bit have been assembled. The data are then transferred to the receive data holding register, the RxRDY bit in the status register is set, and the $\overline{RxRDY}$ output is asserted. If the character length is less than 8 bits, the High order unused bits in the holding register are set to zero. The parity error, framing error, and overrun error status bits are strobed into the status register on the positive going edge of $\overline{RxC}$ corresponding to the received character boundary. If the stop bit is present, the receiver will immediately begin its search for the next start bit. If the stop bit is absent (framing error), the receiver will interpret a space as a start bit if it persists into the next bit timer interval. If a break condition is detected (RxD is Low for the entire character as well as the stop bit), only one character consisting of all zeros (with the FE status bit SR5 set) will be transferred to the holding register. The RxD input must return to a High condition before a search for the next start bit begins.

Pin 25 can be programmed to be a break detect output by appropriate setting of MR27-MR24. If so, a detected break will cause that pin to go High. When RxD returns to mark for one RxC time, pin 25 will go low. Refer to the Break Detection Timing Diagram.

When the EPCI is initialized into the synchronous mode, the receiver first enters the hunt mode on a 0 to 1 transition of RxEN (CR2). In this mode, as data are shifted into the receiver shift register a bit at a time, the contents of the register are compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly mode begins. If single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise, the EPCI returns to the hunt mode. (Note that the sequence SYN1-SYN1-SYN2 will not achieve synchronization.) When synchronization has been achieved, the EPCI continues to assemble characters and transfer then to the holding register, setting the RxRDY status bit and asserting the $\overline{RxRDY}$ output each time a character is transferred. The PE and OE status bits are set as appropriate. Further receipt of the appropriate SYN sequence sets the SYN DETECT status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the holding register. Note that the SYN characters used to establish initial synchronization are not transferred to the holding register in any case.

External jam synchronization can be achieved via pin 9 by appropriate setting of MR27-MR24. When pin 9 is an XSYNC input, the internal SYN1, SYN1–SYN2, and DLE–SYN1 detection is disabled. Each positive going signal on XSYNC will cause the receiver to establish synchronization on the rising edge of the next RxC pulse. Character assembly will start with the RxD input at this edge. XSYNC may be lowered on the next rising edge of RxD. This external synchronization will cause the SYN DETECT status bit to be set until the status register is read. Refer to XSYNC timing diagram.

Table 2. CPU-Related Signals

PIN NAME	PIN NO.	INPUT/ OUTPUT	FUNCTION
RESET	21	I	A High on this input performs a master reset on the 68661. This signal asynchronously terminates any device activity and clears the mode, command and status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.
A0, A1	12,10	I	Address lines used to select internal EPCI registers.
R/W	13	I	Read command when Low, write command when High.
$\overline{CE}$	11	I	Chip enable command. When Low, indicates that control and data lines to the EPCI are valid and that the operation specified by the R/W, A1 and A0 inputs should be performed. When High, places the D0–D7 lines in the 3-State condition.
D0–D7	27,28,1,2,5–8	I/O	8-bit, 3-State data bus used to transfer commands, data and status between EPCI and the CPU. D0 is the least significant bit, D7 the most significant bit.
$\overline{TxRDY}$	15	O	This output is the complement of status register bit SR0. When Low, it indicates that the transmit data holding register (THR) is ready to accept a data character from the CPU. It goes High when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open-drain output which can be used as an interrupt to the CPU.
$\overline{RxRDY}$	14	O	This output is the complement of status register bit SR1. When Low, it indicates that the receive data holding register (RHR) has a character ready for input to the CPU. It goes High when the RHR is read by the CPU, and also when the receiver is disabled. It is an open-drain output which can be used as an interrupt to the CPU.
$\overline{TxEMT}$/ $\overline{DSCHG}$	18	O	This output is the complement of status register bit SR2. When Low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. This output goes High when the status register is ready by the CPU, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the CPU for this line to go high. It is an open-drain output which can be used as an interrupt to the CPU. See Status Register (SR2) for details.

Table 3. Device-Related Signals

PIN NAME	PIN NO.	INPUT/ OUTPUT	FUNCTION
BRCLK	20	I	Clock input to the internal baud rate generator (see Table 1). Not required if external receiver and transmitter clocks are used.
$\overline{RxC}$/BKDET	25	I/O	Receiver clock. If external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. Data are sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin can be a 1X/16X clock or a break detect output pin.
$\overline{TxC}$/XSYNC	9	I/O	Transmitter clock. If external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. The transmitted data changes on the falling edge of the clock. If internal transmitter clock is programmed, this pin can be a 1X/16X clock output or an external jam synchronization input.
RxD	3	I	Serial data input to the receiver. "Mark" is High, "space" is Low.
TxD	19	O	Serial data output from the transmitter. "Mark" is High, "Space" is Low. Held in mark condition when the transmitter is disabled.
$\overline{DSR}$	22	I	General purpose input which can be used for data set ready or ring indicator condition. Its complement appears as status register bit SR7. Causes a Low output on $\overline{TxEMT/DSCHG}$ when its state changes if CR2 or CR0 = 1.
$\overline{DCD}$	16	I	Data carrier detect input. Must be Low in order for the receiver to operate. Its complement appears as status register bit SR6. Causes a Low output on $\overline{TxEMT/DSCHG}$ when its state changes if CR2 or CR0 = 1. If $\overline{DCD}$ goes High while receiving, the RxC is internally inhibited.
$\overline{CTS}$	17	I	Clear to send input. Must be Low in order for the transmitter to operate. If it goes High during transmission, the character in the transmit shift register will be transmitted before termination.
$\overline{DTR}$	24	O	General purpose output which is the complement of command register bit CR1. Normally used to indicate data terminal ready.
$\overline{RTS}$	23	O	General purpose output which is the complement of command register bit CR5. Normally used to indicate request to send. See Command Register (CR5) for details.

Transmitter

The EPCI is conditioned to transmit data when the $\overline{CTS}$ input is Low and the TxEN command register bit is set. The 68661 indicates to the CPU that it can accept a character for transmission by setting the TxRDY status bit and asserting the $\overline{TxRDY}$ output. When the CPU writes a character into the transmit data holding register, these conditions are negated. Data are transferred from the holding register to the transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again. Thus, one full character time of buffering is provided.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the transmit holding register, the TxD output remains in the marking (High) condition and the $\overline{TxEMT/DSCHG}$ output and its corresponding status bit are asserted. Transmission resumes when the CPU loads a new character into the holding register. The transmitter can be forced to output a continuous Low (BREAK) condition by setting the send break command bit (CR3) High.

In the synchronous mode, when the 68661 is initially conditioned to transmit, the TxD output remains High and the TxRDY condition is asserted until the first character to be transmitted (usually a SYN character) is loaded by the CPU. Subsequent to this, a continuous stream of characters is transmitted. No extra bits (other than parity, if commanded) are generated by the EPCI unless the CPU fails to send a new character to the EPCI by the time the transmitter has completed sending the previous character. Since synchronous communication does not allow gaps between characters, the EPCI asserts TxEMT and automatically "fills" the gap by transmitting SYN1s, SYN1–SYN2 doublets, or DLE–SYN1 doubles, depending on the state of MR16 and MR17. Normal transmission of the message resumes when a new character is available in the transmit data holding register. If the send DLE bit in the commands register is true, the DLE character is automatically transmitted prior to transmission of the message character in the THR.

EPCI PROGRAMMING

Prior to initiating data communications, the 68661 operational mode must be programmed by performing write operations to the mode and command registers. In addition, if synchronous operation is programmed, the appropriate SYN/DLE registers must be loaded. The EPCI can be reconfigured at any time during program execution. A flowchart of the initialization process appears in Figure 1.

The internal registers of the EPCI are accessed by applying specific signals to the $\overline{CE}$, $\overline{R}/W$, A1 and A0 inputs. The conditions necessary to address each register are shown in Table 4.

The SYN1, SYN2, and DLE registers are accessed by performing write operations with the conditions A1 = 0, A0 = 1, and $\overline{R}/W$ = 1. The first operation loads the SYN1 register. The next loads the DLE register. Reading or loading the mode registers is done in a similar manner. The first write (or read) operation addresses mode register 1, and a subsequent operation addresses mode register 2. If more than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointers are reset to SYN1 register and mode register 1 by a RESET input or by performing a read command register operation, but are unaffected by any other read or write operation.

The 68661 register formats are summarized in Tables 5, 6, 7 and 8. Mode registers 1 and 2 define the general operational characteristics of the EPCI, while the command register controls the operation within this basic framework. The EPCI indicates its status in the status register. These registers are cleared when a RESET input is applied.

Mode Register 1 (MR1)

Table 5 illustrates mode register 1. Bits MR11 and MR10 select the communication format and baud rate multiplier. 00 specifies synchronous format. However, the multiplier in asynchronous format applies only if the external clock input option is selected by MR24 or MR25.

MR13 and MR12 select a character length of 5, 6, 7 or 8 bits. The character length does not incclude the parity bit, if programmed, and does not include the start and stop bits in asynchronous mode.

MR14 controls parity generation. If enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR15 selects odd or even parity when parity is enabled by MR14. In asynchronous mode, MR17 and MR16 select character framing of 1, 1.5, or 2 stop bits. (If 2X baud rate is programmed, 1.5 stop bits defaults to 1 stop bits on transmit.) In synchronous mode, MR17 controls the number of SYN characters used to establish synchronization and for character fill when the transmitter is idle. SYN1 alone is used if MR17 = 1, and SYN1–SYN2 is used when MR17 = 0. If the transparent mode is specified by MR16, DLE–SYN1 is used for character fill and SYN detect, but the normal synchronization sequence is used to establish character sync. When transmitting, a DLE character in the transmit holding register will cause a second DLE character to be transmitted. This DLE stuffing eliminates the software DLE compare and stuff on each transparent mode data character. If the send DLE command (CR3) is active when a DLE is loaded into THR, only one additional DLE will be transmitted. Also, DLE stripping and DLE detect (with MR14 = 0) are enabled.

The bits in the mode register affecting character assembly and disassembly (MR12–MR16) can be changed dynamically (during active receive/transmit operation). The character mode register affects both the transmitter and receiver; therefore in synchronous mode, changes should be made only in half-duplex mode (RxEN = 1 or TxEN = 1, but not both simultaneously = 1). In asynchronous mode, character changes should be made when RxEN and TxEN = 0 or when TxEN = 1 and the transmitter is marking in half-duplex mode (RxEN = 0).

To effect assembly/disassembly of the next received/transmitted character, MR12 – 15 must be changed within n bit times of the active going state of $\overline{RxRDY/TxRDY}$. Transparent and non-transparent mode changes (MR16) must occur within n-1 bit times of the character to be affected when the receiver or transmitter is active. (n – smaller of the new and old character lengths.)

Table 4. 68661 Register Addressing

$\overline{CE}$	A_1	A_0	R/$\overline{W}$	FUNCTION
1	X	X	X	3-State data bus
0	0	0	0	Read receive holding register
0	0	0	1	Write transmit holding register
0	0	1	0	Read status register
0	0	1	1	Write SYN1/SYN2/DLE registers
0	1	0	0	Read mode register 1/2
0	1	0	1	Write mode register 1/2
0	1	1	0	Read command register
0	1	1	1	Write command register

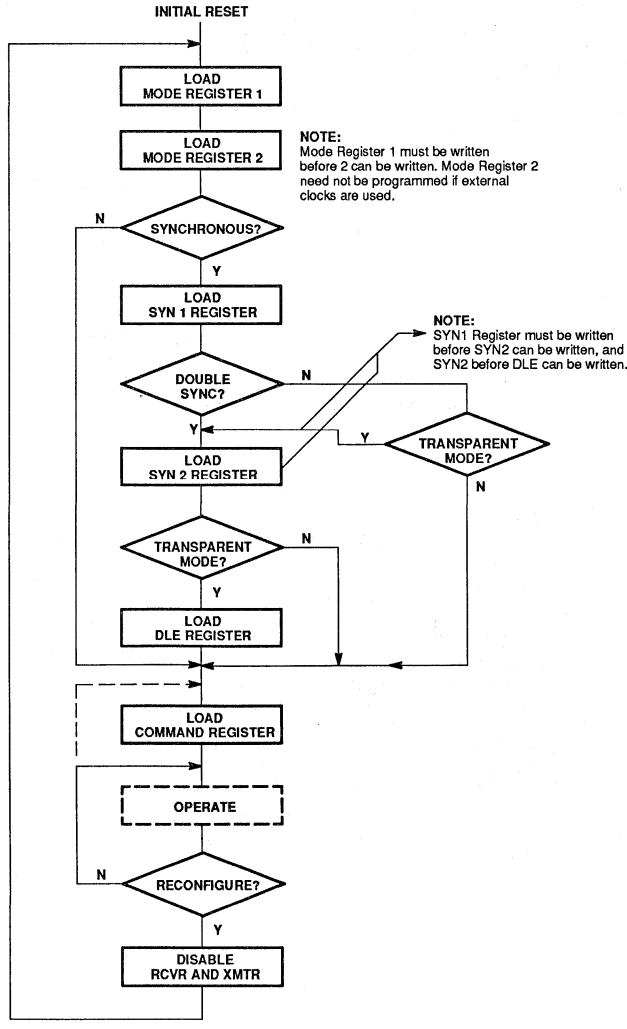


Figure 1. 68661 Initialization Flowchart

Table 5. Mode Register 1 (MR1)

MR17	MR16	MR15	MR14	MR13	MR12	MR11	MR10
Sync/Async		Parity Type	Parity Control	Character Length		Mode and Baud Rate Factor	
Async: Stop bit length 00 = invalid 01 = 1 stop bit 10 = 1 1/2 stop bits 11 = 2 stop bits		0 = Odd 1 = Even	0 = Disabled 1 = Enabled	00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits		00 = Synchronous 1X rate 01 = Asynchronous 1X rate 10 = Asynchronous 16X rate 11 = Asynchronous 64X rate	
Sync: Number of SYN char 0 = Double SYN 1 = Single SYN	**Sync: Transparency control** 0 = Normal 1 = Transparent						

NOTE: Baud rate factor in asynchronous applies only if external clock is selected. Factor is 16X if internal clock is selected. Mode must be selected (MR11, MR10) in any case.

Table 6. Mode Register 2 (MR2)

MR27 – MR24											MR23 – MR20
	TxC	RxC	Pin 9	Pin 25		TxC	RxC	Pin 9	Pin 25	Mode	Baud Rate Selection
0000	E	E	TxC	RxC	1000	E	E	XSYNC*	RXC/TxC	sync	
0001	E	I	TxC	1X	1001	E	I	TxC	BKDET	async	
0010	I	E	1X	RxC	1010	I	E	XSYNC*	RxC	sync	
0011	I	I	1X	1X	1011	I	I	1X	BKDET	async	See baud rates in Table 1.
0100	E	E	TxC	RxC	1100	E	E	XSYNC*	RxC/TxC	sync	
0101	E	I	TxC	16X	1101	E	I	TXC	BKDET	async	
0110	I	E	16X	RxC	1110	I	E	XSYNC*	RxC	sync	
0111	I	I	16X	16X	1111	I	I	16X	BKDET	async	

NOTES:
* When pin 9 is programmed as XSYNC input, SYN1, SYN1–SYN2, and DLE–SYN1 detection is disabled.
E = External clock
I = Internal clock (BRG)
1X and 16X are clock outputs.

Table 7. Command Register (CR)

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
Operating Mode		Request to Send	Reset Error	Sync/Async	Receive Control (RxEN)	Data Terminal Ready	Transmit Control (TxEN)
00 = Normal operation 01 = Async: Automatic Echo mode Sync: SYN and/or DLE stripping mode 10 = Local loopback 11 = Remote loopback		0 = Force $\overline{RTS}$ Output High one clock time after TxSR serialization 1 = Force $\overline{RTS}$ output Low	0 = Normal 1 = Reset error flags in status reg. (FE,OE,PE/ DLE detect.)	**Async:** Force Break 0 = Normal 1 = Force break **Sync** **Send DLE** 0 = Normal 1 = Send DLE	0 = Disable 1 = Enable Not applicable in	0 = Force $\overline{DTR}$ output High 1 = Force $\overline{DTR}$ output Low	0 = Disable 1 = Enable

Table 8. Status Register (SR)

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
Data Set Ready	**Data Carrier Detect**	**FE/SYN Detect**	**Overrun**	**PE/DLE Detect**	**TxEMT DSCHG**	**RxRDY**	**TxRDY**
0 = $\overline{DSR}$ input is High 1 = $\overline{DSR}$ input is Low	0 = $\overline{DCD}$ input is High 1 = $\overline{DCD}$ input is Low	**Async:** 0 = Normal 1 = Framing error **Sync:** 0 = Normal 1 = SYN detected	0 = Normal 1 = Overrun error	**Async:** 0 = Normal 1 = Parity error **Sync:** 0 = Normal 1 = Parity error or DLE received	0 = Normal 1 = Change in $\overline{DSR}$ or $\overline{DCD}$, or transmit shift register is empty	0 = Receive holding register empty 1 = Receive holding register has data	0 = Transmit holding register busy 1 = Transmit holding register empty

Mode Register 2 (MR2)

Table 6 illustrates mode register 2. MR23, MR22, MR21 and MR20 control the frequency of the internal baud rate generator (BRG). Sixteen rates are selectable for each EPCI version (–1,–2,–3). Versions 1 and 2 specify a 4.9152MHz TTL input at BRCLK (pin 20); version 3 specifies a 5.0688MHz input which is identical to the Signetics 2651. MR23 – 20 are don't cares if external clocks are selected (MR25 – MR24 = 0). The individual rates are given in Table 1.

MR24 – MR27 select the receive and transmit clock source (either the BRG or an external input) and the function at pins 9 and 25. Refer to Table 6.

Command Register (CR)

Table 7 illustrates the command register. Bits CR0 (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. A 0– to–1 transition of CR2 forces start bit search (async mode) or hunt mode (sync mode) on the second $\overline{RxC}$ rising edge. Disabling the receiver causes $\overline{RxRDY}$ to go High (inactive). If the transmitter is disabled, it will complete the transmission of the character in the transmit shift register (if any) prior to terminating operation. The TxD output will then remain in the marking state (High) while $\overline{TxRDY}$ and $\overline{TxEMT}$ will go High (inactive). If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be neglected. A 0–to–1 transition of CR2 will initiate start bit search (async) or hunt mode (sync).

Bits CR1 (DTR) and CR5 (RTS) control the $\overline{DTR}$ and $\overline{RTS}$ outputs. Data at the outputs are the logical complement of the register data.

In asynchronous mode, setting CR3 will force and hold the TxD output Low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The TxD line will go High for at least one bit time before beginning transmission of the next character in the transmit data holding register. In synchronous mode, setting CR3 causes the transmission of the DLE register contents prior to sending the character in the transmit data holding register. Since this is a one time command, CR3 does not have to be reset by software. CR3 should be set when entering and exiting transparent mode and for all DLE-non-DLE character sequences.

Setting CR4 causes the error flags in the status register (SR3, SR4, and SR5) to be cleared; this is a one time command. There is no internal latch for this bit.

When CR5 (RTS) is set, the $\overline{RTS}$ pin is forced Low. A 1–to–0 transition of CR5 will cause $\overline{RTS}$ to go High (inactive) one TxC time after the last serial bit has been transmitted. If a 1–to–0 transition of CR5 occurs while data is being transmitted, $\overline{RTS}$ will remain Low (active) until both the THR and the transmit shift register are empty and then go High (inactive) one TxC time later.

The EPCI can operate in one of four submodes within each major mode (synchronous or asynchronous). The operational sub-mode is determined by CR7 and CR6. CR7 – CR6 = 00 is the normal mode, with the transmitter and receive operating independently in accordance with the mode and status register instructions.

In asynchronous mode, CR7 – CR6 = 01 places the EPCI in the automatic echo mode. Clocked, regenerated received data are automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2 = 1), but the transmitter need not be enabled. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled. Only the first character of a break condition is echoed.

The TxD output will go High until the next valid start is detected. The following conditions are true while in automatic echo mode:

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. $\overline{TxRDY}$ **output = 1.**
4. The $\overline{TxEMT/DSCHG}$ pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In synchronous mode, CR7 – CR6 = 01 places the EPCI in the automatic SYN/DLE stripping mode. The exact action taken depends on the setting of bits MR17 and MR16:

1. In the non-transparent, single SYN mode (MR17 – MR16 = 10), characters in the data stream matching SYN1 are not transferred to the Receive Data Holding register (RHR).
2. In the non-transparent, double SYN mode (MR17 – MR16 = 00), character in the data stream matching SYN1, or SYN2 if immediately preceded by SYN1, are not transferred the RHR.
3. In transparent mode (MR16 = 1), character in the data stream matching DLE, or SYN1 if immediately preceded by DLE, are not transferred to the RHR. However, only the first DLE of a DLE–DLE pair is stripped.

Note that automatic stripping mode does not affect the setting of the DLE detect and SYN detect status bits (SR3 and SR5).

Two diagnostic sub-modes can also be configured. In local loopback mode (CR7 – CR6 = 10), the following loops are connected internally:

1. The transmitter output is connected to the receiver input.

2. $\overline{DTR}$ is connected to $\overline{DCD}$ and $\overline{RTS}$ is connected to $\overline{CTS}$.
3. The receiver is clocked by the transmit clock.
4. The $\overline{DTR}$, $\overline{RTS}$ and $\overline{TxD}$ outputs are held High.
5. The $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ and RxD inputs are ignored.

Additional requirements to operate in the local loopback mode are that CR0 (TxEN), CR1 (DTR) and CR5 (RTS) must be set to 1. CR2 (RxEN) is ignored by the EPCI.

The second diagnostic mode is the remote loopback mode (CR7 – CR6 = 11). In this mode:

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receiver clock.
3. No data are sent to the local CPU, but he error status conditions (PE, FE) are set.
4. The $\overline{RxRDY}$, $\overline{TxRDY}$, and $\overline{TxEMT}$/$\overline{DSCHG}$ outputs are held High.
5. CR0 (TxEN) is ignored.
6. All other signals operate normally.

Status Register

The data contained in the status register (as shown in Table 8) indicates receiver and transmitter conditions and modem/data set status.

SR0 is the transmitter ready (TxRDY) status bit. It, and its corresponding output, are valid only when the transmitter is enabled. If equal to 0–, it indicates that the transmit data holding register has been loaded by the CPU and the data has not been transferred to the transmit register. If set equal to 1, it indicates that the holding register is ready to accept data from the CPU. This bit is initially set when the transmitter is enabled by CR0, unless a character has previously been loaded into the holding register. It is not set when the automatic echo or remote loopback modes are programmed. When this bit is set, the $\overline{TxRDY}$ output pin is Low. In the automatic echo and remote loopback modes, the output is held High.

SR1, the receiver ready (RxRDY) status bit, indicates the condition of the receive data holding register. If set, it indicates that a character has been loaded into the holding register from the receive shift register and is ready to be read by the CPU. If equal to zero, there is no new character in the holding register. This bit is cleared when the CPU reads the receive data holding register or when the receiver is disabled by CR2. When set, the $\overline{RxRDY}$ output is Low.

The TxEMT/DSCHG bit, SR2, when set, indicates either a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs (when CR2 or CR0 = 1) or that the transmit shift register has completed transmission of a character and no new character has been loaded into the transmit data holding register. Note that in synchronous mode this bit will be set even though the appropriate "fill" character is transmitted. TxEMT will not go active until at least one character has been transmitted. It is cleared by loading the transmit data holding register. The DSCHG conditions is enabled when TxEN = 1 or RxEN = 1. It is cleared when the status register is read by the CPU. If the status register is read twice and SR2 – 1 while SR6 and SR7 remain unchanged, then a TxEMT condition exists. When SR2 is set, the $\overline{TxEMT/DSCHG}$ output is Low.

SR3, when set, indicates a received parity error when parity is enabled by MR14. In synchronous transparent mode (MR16 = 1), with parity disabled, it indicates that a character matching DLE register was received and the present character is neither SYN2 or DLE. This bit is cleared when the next character following the above sequence is loaded into RHR, when the receiver is disabled, or by a reset error command, CR4.

The overrun error status bit, SR4, indicates that the previous character loaded into the receive holding register was not ready the CPU at the time of new received character was transferred into it. This bit is cleared when the receiver is disabled or by the reset error command, CR4.

In asynchronous mode, bit SR5 signifies that the received character was not framed by a stop bit; i.e., only the first stop bit is checked. If RHR = 0 when SR5 = 1, a break condition is present. In synchronous non-transparent mode (MR16 = 0), it indicates receipt of the SYN1 character in single SYN mode or the SYN1 – SYN2 pair in double SYN mode. In synchronous transparent mode (MR16 = 1), this bit is set upon detection of the initial synchronizing characters (SYN or SYN1 – SYN2) and, after synchronization has been achieved, when a DLE–SYN1 pair is received. The bit is reset when the receiver is disabled, when the reset error command is given in asynchronous mode, or when the status register is read by the CPU in the synchronous mode.

SR6 and SR7 reflect the conditions of the $\overline{DCD}$ and $\overline{DSR}$ inputs, respectively. A Low input sets its corresponding status bit, and a High input clears it.

Table 9. 68661 EPCI vs 2651 PCI

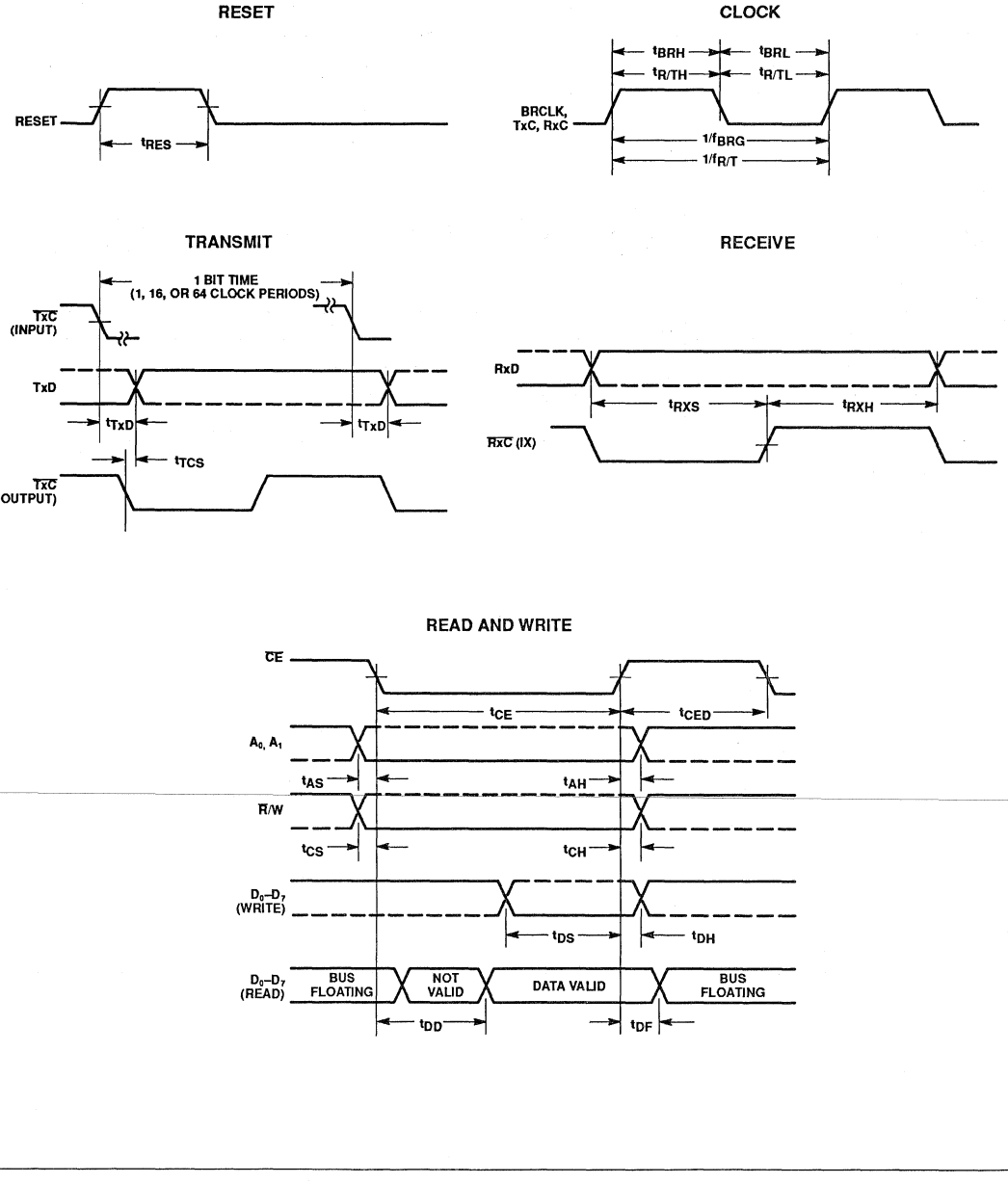
FEATURE	EPCI	PCI
1. MR2 BIT 6, 7	Control pins 9, 25	Not used
2. DLE detect – SR3	SR3 = 0 for DLE–DLE, DLE – SYN1	SR3 = 1 for DLE–DLE, DLE – SYN1
3. Reset of SR3, DLE detect	Second character after DLE, or receiver disable, or CR4 = 1	Receiver disable, or CR4 = 1
4. Send DLE – CR3	One time command	Reset via CR3 on next $\overline{\text{TxRDY}}$
5. DLE stuffing in transparent mode	Automatic DLE stuffing when DLE is loaded except if CR3 = 1	None
6. SYN1 stripping in double sync non-transparent mode	All SYN1	First SYN1 of pair
7. Baud rate versions	Three	One
8. Terminate ASYNC transmission (drop RTS)	Reset CR5 in response to $\overline{\text{TxEMT}}$ changing from 1 to 0	Reset CR0 when $\overline{\text{TxEMT}}$ goes from 1 to 0. Then reset CR5 when $\overline{\text{TxEMT}}$ goes from 1 to 0
9. Break detect	Pin 25*	FE and null character
10. Stop bit searched	One	Two
11. External jam sync	Pin 9**	No
12. Data bus timing	Improved over 2651	—
13. Data bus drivers	Sink 2.2mA Source 400µA	Sink 1.6mA Source 100µA

NOTES:
* Internal BRG used for RxC.
** Internal BRG used for TxC.

AC LOAD CONDITIONS

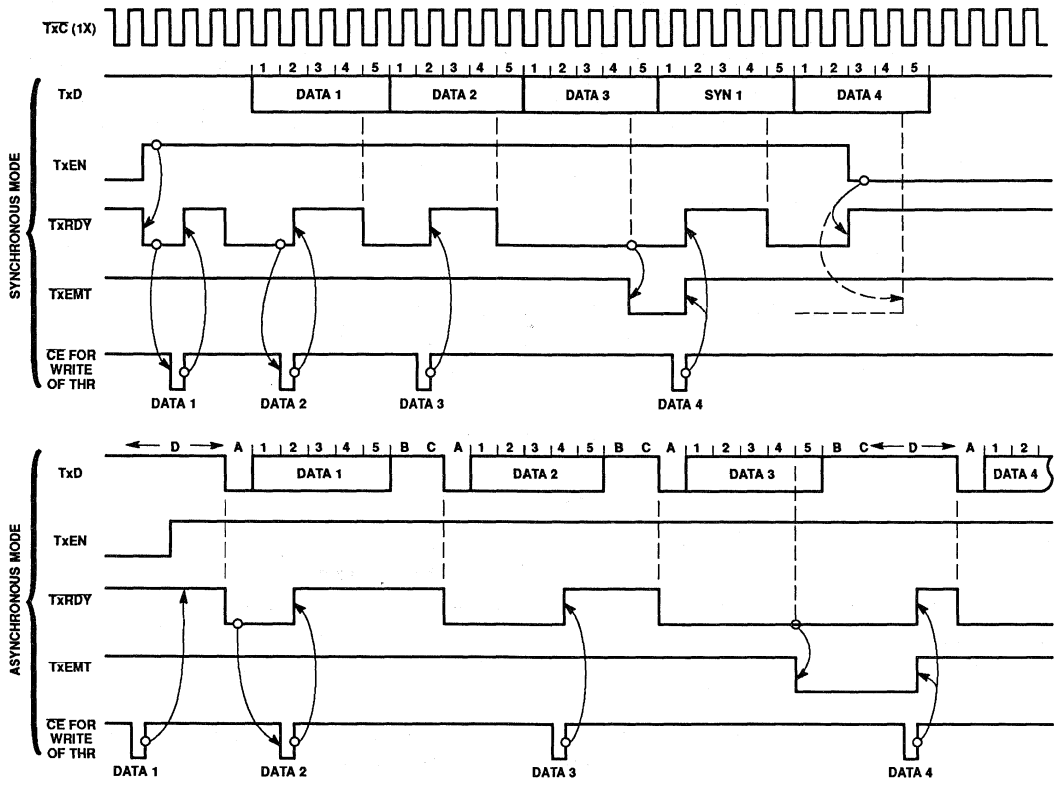
NOTES:
Open-drain outputs.
C_L = Load capacitance includes JIG and probe capacitance.

TIMING DIAGRAMS



TIMING DIAGRAMS (Continued)

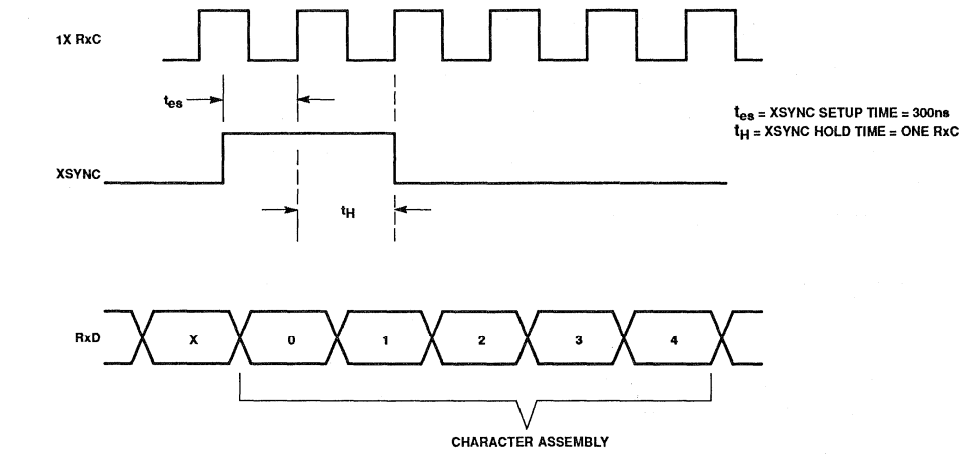
TxRDY, TxEMT (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])



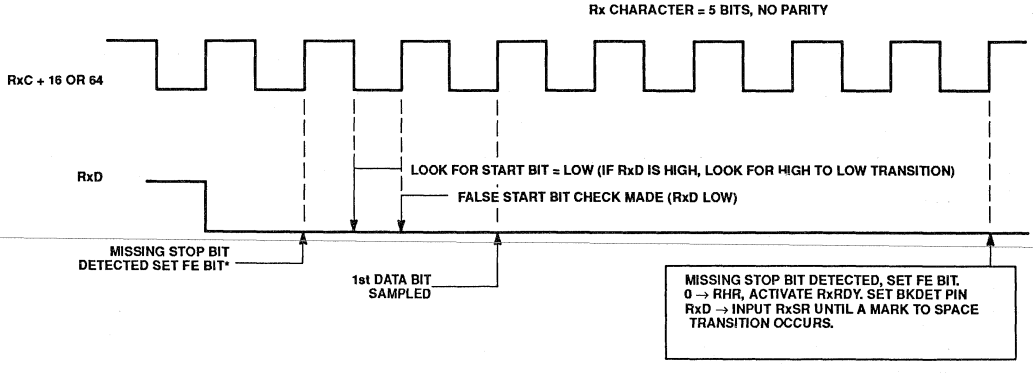
NOTES:
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition
TxEMT goes low at the beginning of the last data bit, or, if parity is enabled, at the beginning of the parity bit.

TIMING DIAGRAMS (Continued)

EXTERNAL SYNCHRONIZATION WITH XSYNC



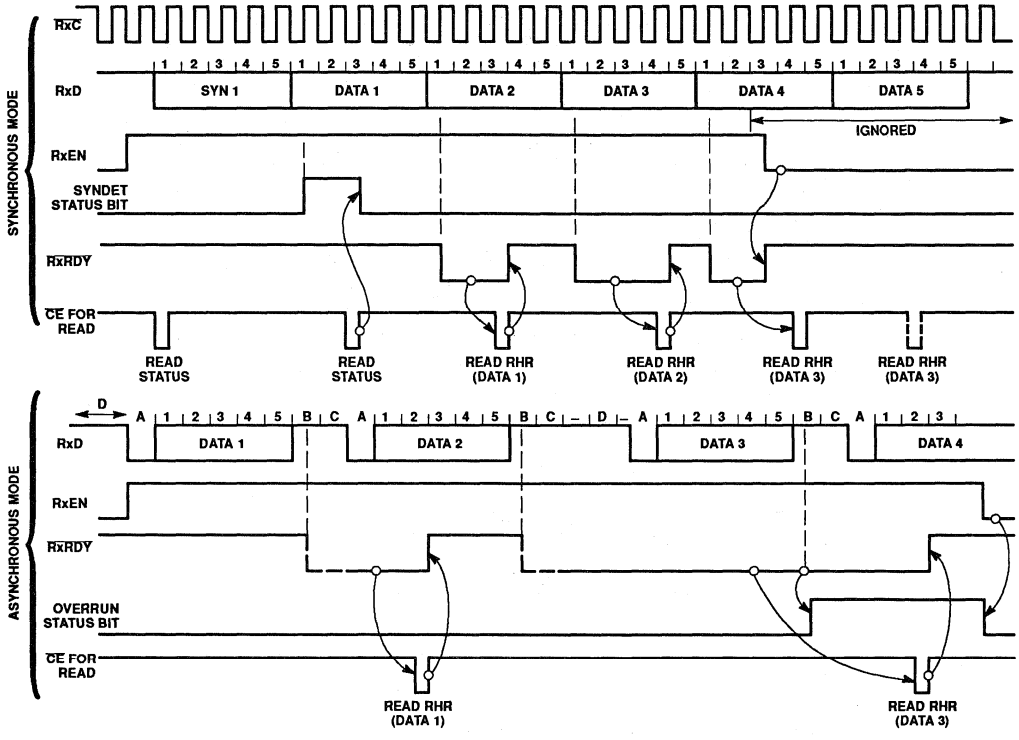
BREAK DETECTION TIMING



NOTE:
* If the stop bit is present, the start bit search will commence immediately.

TIMING DIAGRAMS (Continued)

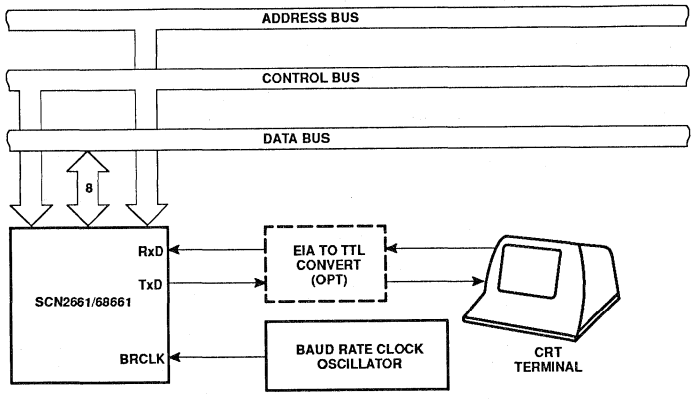
RxRDY (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])



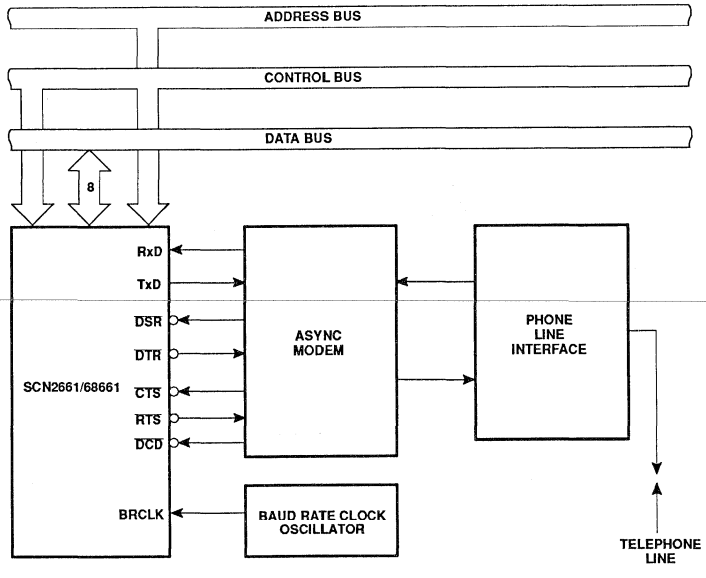
NOTES:
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition
Only one stop bit is detected

TYPICAL APPLICATIONS

ASYNCHRONOUS INTERFACE TO CRT TERMINAL

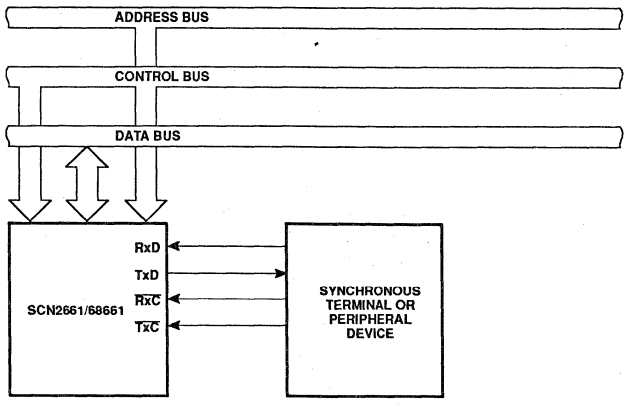


ASYNCHRONOUS INTERFACE TO TELEPHONE LINES

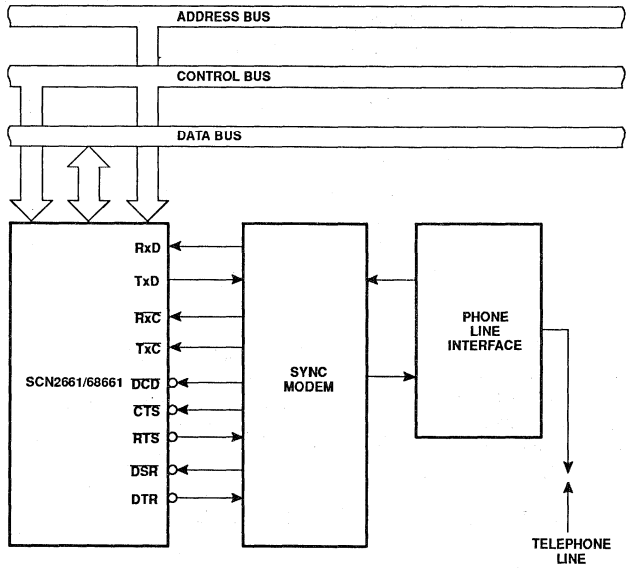


TYPICAL APPLICATIONS (Continued)

SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



SYNCHRONOUS INTERFACE TO TELEPHONE LINES



Dual asynchronous receiver/transmitter (DUART) SCN2681

DESCRIPTION

The Signetics SCN2681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruply buffered to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the buffer of the receiving device is full.

FEATURES

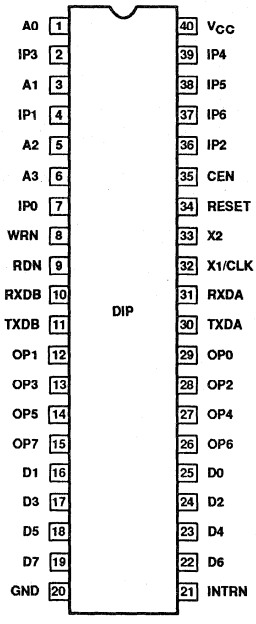
- Dual full-duplex asynchronous receiver/transmitter
- Quadruple buffered receiver data registers
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4k baud
  - Non-standard rates to 115.2Kb
  - One user-defined rate derived from programmable timer/counter
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function programmable 16-bit counter/timer
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer: 1X – 1MB/sec, 16X – 125kB/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Single +5V power supply
- Commercial and industrial temperature ranges available
- DIP and PLCC packages

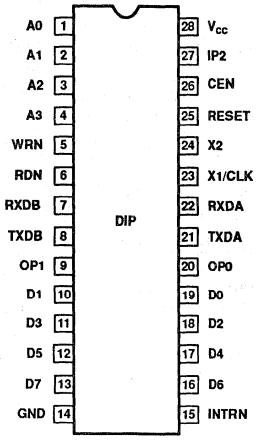
ORDERING INFORMATION

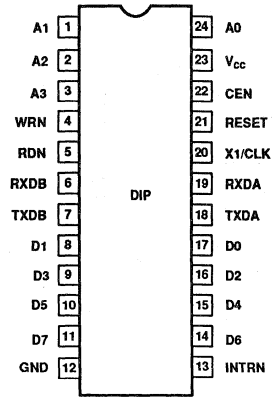
DESCRIPTION	ORDER CODE					
	V_{CC} = +5V ±5%, T_A = 0°C to +70°C				V_{CC} = +5V ±10%, T_A = -40°C to +85°C	
	24-Pin[1]	28-Pin[2]	40-Pin[2]	44-Pin	40-Pin[2]	44-Pin
Ceramic DIP	Not available	SCN2681AC1F28	SCN2681AC1F40	Not available	SCN2681AE1F40	Not available
Plastic DIP	SCN2681AC1N24	SCN2681AC1N28	SCN2681AC1N40	Not available	SCN2681AE1N40	Not available
Plastic LCC	Not available	Not available	Not available	SCN2681AC1A44	Not available	Not available

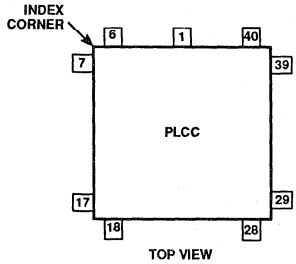
NOTES:
1. 400mil-wide DIP
2. 600mil-wide DIP

PIN CONFIGURATIONS









PIN/FUNCTION		PIN/FUNCTION	
1	NC	23	NC
2	A0	24	INTRN
3	IP3	25	D6
4	A1	26	D4
5	IP1	27	D2
6	A2	28	D0
7	A3	29	OP6
8	IP0	30	OP4
9	WRN	31	OP2
10	RDN	32	OP0
11	RXDB	33	TXDA
12	NC	34	NC
13	TXDB	35	RXDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CEN
18	D1	40	IP2
19	D3	41	IP6
20	D5	42	IP5
21	D7	43	IP4
22	GND	44	VCC

Also provided on the SCN2681 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

The SCN2681 is available in three package versions: 40-pin and 28–pin, both 0.6" wide DIPs; a compact 24-pin 0.4" wide DIP; and a 44-pin PLCC.

PIN DESCRIPTION

SYMBOL	APPLICABLE			TYPE	NAME AND FUNCTION
	40/44	28	24		
D0–D7	X	X	X	I/O	**Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	X	X	X	I	**Chip Enable:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the WRN, RDN and A0-A3 inputs. When High, places the D0-D7 lines in the 3-State condition.
WRN	X	X	X	I	**Write Strobe:** When Low and CEN is also Low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	X	X	X	I	**Read Strobe:** When Low and CEN is also Low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0–A3	X	X	X	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	X	X	X	I	**Reset:** A High level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0–OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Clears Test modes.
INTRN	X	X	X	O	**Interrupt Request:** Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	X	X	X	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5).
X2	X	X		I	**Crystal 2:** Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5).
RxDA	X	X	X	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	X	X	X	I	**Channel B Receive Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	X	X	X	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
TxDB	X	X	X	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
OP0	X	X		O	**Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	X	X		O	**Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	X			O	**Output 2:** General purpose output or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	X			O	**Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	X			O	**Output 4:** General purpose output or Channel A open-drain, active-Low, RxRDYA/FFULLA output.
OP5	X			O	**Output 5:** General purpose output or Channel B open-drain, active-Low, RxRDYB/FFULLB output.
OP6	X			O	**Output 6:** General purpose output or Channel A open-drain, active-Low, TxRDYA output.
OP7	X			O	**Output 7:** General purpose output or Channel B open-drain, active-Low, TxRDYB output.
IP0	X			I	**Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	X			I	**Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	X	X		I	**Input 2:** General purpose input or counter/timer external clock input.
IP3	X			I	**Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.

PIN DESCRIPTION (Continued)

SYMBOL	APPLICABLE			TYPE	NAME AND FUNCTION
	40/44	28	24		
IP4	X			I	**Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	X			I	**Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6	X			I	**Input 6:** General purpose input or Channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
V_{CC}	X	X		I	**Power Supply:** +5V supply input.
GND	X	X		I	**Ground**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	See Note 4	°C
T_{STG}	Storage temperature range	-65 to +150	°C
	All voltages with respect to ground[3]	-0.5 to +6.0	V

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range. See Ordering information table for applicable operating temperature range and V_{CC} supply range.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage (except X1/CLK)[5]		2			V
V_{IH}	Input high voltage (except X1/CLK)[4]		2.5			V
V_{IH}	Input high voltage (X1/CLK)		4			V
V_{OL}	Output low voltage	I_{OL} = 2.4mA			0.4	V
V_{OH}	Output high voltage (except o.d. outputs)[5]	I_{OH} = -400µA	2.4			V
V_{OH}	Output high voltage (except o.d. outputs)[4]	I_{OH} = -400µA	2.9			V
I_{IL}	Input leakage current	V_{IN} = 0 to V_{CC}	-10		10	µA
I_{LL}	Data bus 3-stage leakage current	V_O = 0.4 to V_{CC}	-10		10	µA
I_{X1L}	X1/CLK low input current	V_{IN} = 0, X2 grounded	-4	-2	0	mA
		V_{IN} = 0, X2 floated	-3	-1.5	0	mA
I_{X1H}	X1/CLK high input current	V_{IN} = V_{CC}, X2 grounded	-1	0.2	1	mA
		V_{IN} = V_{CC}, X2 floated	0	3.5	10	mA
I_{X2L}	X2 low input current	V_{IN} = 0, X1/CLK floated	-100	-30	0	µA
I_{X2H}	X2 high input current	V_{IN} = V_{CC}, X1/CLK floated	0	+30	100	µA
I_{OC}	Open-collector output leakage current	V_O = 0.4 to V_{CC}	-10		10	µA
I_{OCC}	Power supply current					
	0°C to +70°C version				150	mA
	-40°C to +85°C version				175	mA

NOTES:
1. Parameters are valid over specified temperature range. See Ordering information table for applicable operating temperature range and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. T_A < 0°C
5. $T_A \geq$ 0°C

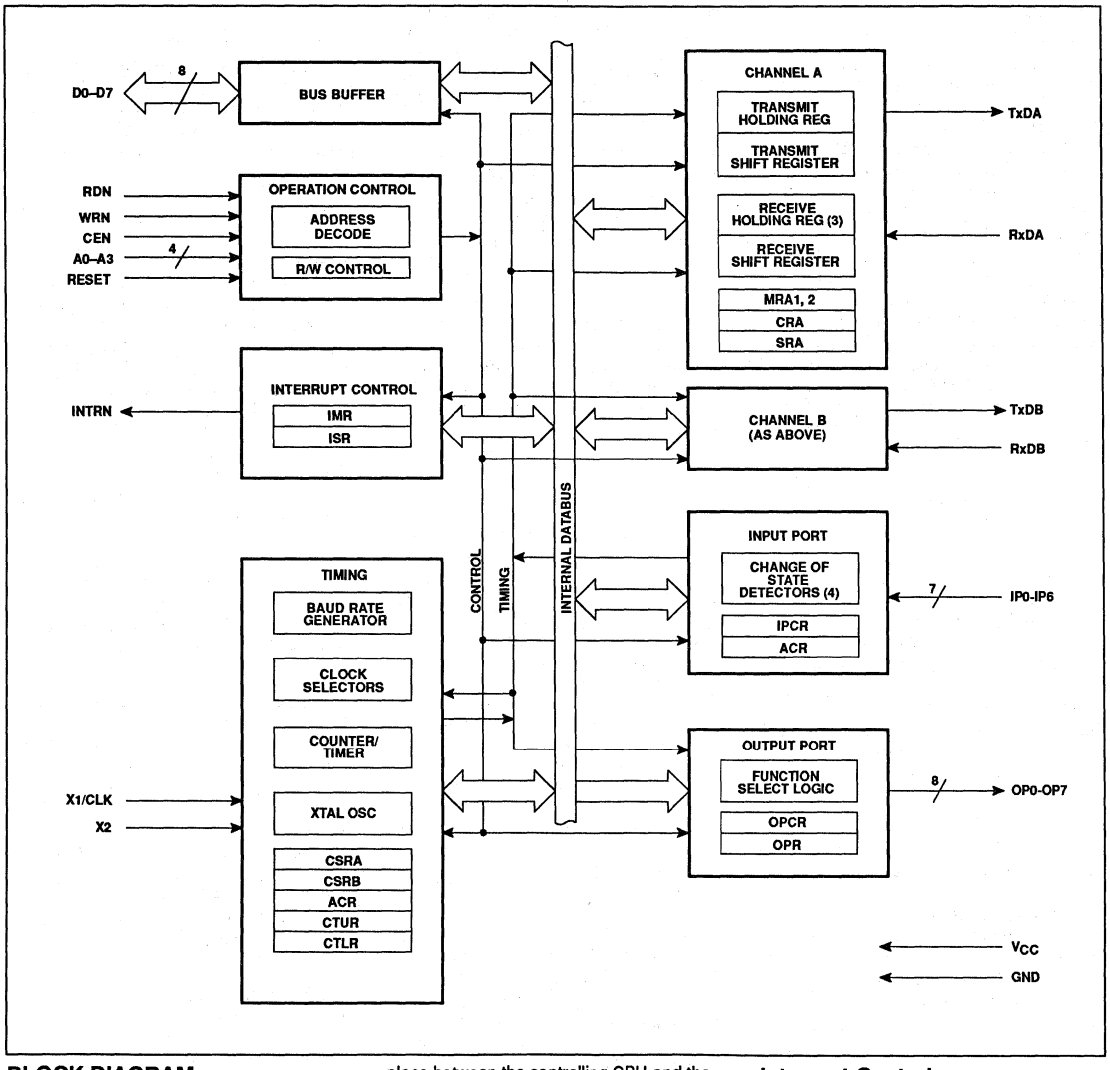
AC CHARACTERISTICS T_A = -55°C to +125°C[1], V_{CC} = +5.0V ± 10%[2, 3, 4, 5]

SYMBOL	PARAMETER	LIMITS Min	Typ	Max	UNIT
Reset Timing (Figure 1)					
t_{RES}	RESET pulse width	200			ns
Bus Timing (Figure 2)[6]					
t_{AS}	A0-A3 setup time to RDN, WRN Low	10			ns
t_{AH}	A0-A3 hold time from RDN, WRN Low	100			ns
t_{CS}	CEN setup time to RDN, WRN Low	0			ns
t_{CH}	CEN hold time from RDN, WRN High	0			ns
t_{RW}	WRN, RDN pulse width	225			ns
t_{DD}	Data valid after RDN Low			175	ns
t_{DF}	Data bus floating after RDN High			100	ns
t_{DS}	Data setup time before WRN High	100			ns
t_{DH}	Data hold time after WRN High	20			ns
t_{RWD}	High time between READs and/or WRITE[7, 8]	200			ns
Port Timing (Figure 3)[6]					
t_{PS}	Port input setup time before RDN Low	0			ns
t_{PH}	Port input hold time after RDN High	0			ns
t_{PD}	Port output valid after WRN High			400	ns
Interrupt Timing (Figure 4)					
t_{IR}	INTRN (or OP3-OP7 when used as interrupts) negated from:				
	Read RHR (RxRDY/FFULL interrupt)			300	ns
	Write THR (TxRDY interrupt)			300	ns
	Reset command (delta break interrupt)			300	ns
	Stop C/T command (counter interrupt)			300	ns
	Read IPCR (input port change interrupt)			300	ns
	Write IMR (clear of interrupt mask bit)			300	ns
Clock Timing (Figure 5)[10]					
t_{CLK}	X1/CLK High or Low time	100			ns
f_{CLK}	X1/CLK frequency	2.0	3.6864	4.0	MHz
t_{CTC}	CTCLK (IP2) High or Low time	100			ns
f_{CTC}	CTCLK (IP2) frequency	0		4.0	MHz
t_{RX}[9]	RxC High or Low time	220			ns
f_{RX}[9]	RxC frequency (16X)	0		2.0	MHz
	(1X)	0		1.0	MHz
t_{TX}[9]	TxC High or Low time	220			ns
f_{TX}[9]	TxC frequency (16X)	0		2.0	MHz
	(1X)	0		1.0	MHz
Transmitter Timing (Figure 6)					
t_{TXD}[9]	TxD output delay from TxC Low			350	ns
t_{TCS}[9]	Output delay from TxC Low to TxD data output	0		150	ns
Receiver Timing (Figure 7)					
t_{RXS}[9]	RxD data setup time to RxC High	240			ns
t_{RXH}[9]	RxD data hold time from RxC High	200			ns

NOTES:

1. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
2. Parameters are valid over specified temperature range.
3. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of ≤ 20ns. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate.
4. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
5. Test condition for outputs: C_L = 150pF, except interrupt outputs. Test condition for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
6. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. In this case, all timing specifications apply referenced to the falling and rising edges of CEN, CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
7. If CEN is used as the 'strobing' input, the parameter defines the minimum High times between one CEN and the next. The RDN signal must be negated for t_{RWD} to guarantee that any status register changes are valid.
8. Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.
9. This parameter is not applicable to the 28-pin device.
10. Operation to 0MHz is assured by design. However, operation at low frequencies is not tested and has not been characterized.

BLOCK DIAGRAM



BLOCK DIAGRAM

The SCN2681 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the block diagram.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer.

Interrupt Control

A single active-Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR). The IMR may be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to

determine all currently active interrupting conditions.

Outputs OP3-OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a 3.6864MHz crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART.

If an external is used instead of a crystal, both X1 and X2 should be driven using a configuration similar to the one in Figure 5.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4k baud. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

The Counter/Timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

Communications Channels A and B

Each communications channel of the SCN2681 comprises a full-duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

The input port pulse detection circuitry uses a 38.4kHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25µs (this assumes that the clock input is 3.6864MHz). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs "coincident with the first sample pulse". The 50µs time refers to the situation in which the change-of-state is "just missed" and the first change-of-state is not detected until 25µs later.

Input Port

The inputs to this unlatched 7-bit port can be read by the CPU by performing a read operation at address D16. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always read as a logic 1. The pins of this port can also serve as auxiliary inputs to certain portions fo the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs lasting longer than 25 – 50µs, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU.

Output Port

The output port pins may be controlled by the OPR, OPCR, MR and CR registers. Via appropriate programming they may be just another parallel port to external circuits, or they may represent many internal conditions of the UART. When this 8-bit port is used as a general purpose output port, the output port pins drive a state which is the complement of the Output Port Register (OPR). OPR(n) = 1 results in OP(n) = Low and vice versa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operation at address E16 with the accompanying data specifying the bits to be set (1 = set, 0 = no change).

Likewise, a bit is reset by a write at address F16 with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Outputs can be also individually assigned specific functions by appropriate programming of the Channel A mode registers (MR1A, MR2A), the Channel B mode registers (MR1B, MR2B), and the Output Port Configuration Register (OPCR).

OPERATION

Transmitter

The SCN2681 is conditioned to transmit data when the transmitter is enabled through the command register. The SCN2681 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When a character is loaded into the Transmit Holding Register (THR), the above conditions are negated. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again which means one full character time of buffering is provided. Characters cannot be loaded into the THR while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains High and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the THR.

If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous Low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS operation is enable, the CTSN input must be Low in order for the character to be transmitted. If it goes High in the middle of a transmission, the character in the shift register is transmitted

and TxDA then remains in the marking state until CTSN goes Low. The transmitter can also control the deactivation of the RTSN output. If programmed, the RTSN output will be reset one bit time after the character in the transmit shift register and transmit holding register (if any) are completely transmitted, if the transmitter has been disabled.

Receiver

The SCN2681 is conditioned to receive data when enabled through the command register. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7 1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive Holding Register (RHR) and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than eight bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, overrun error and received break state (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1. The RxD input must return to a High condition for at least one-half bit time before a search for the next start bit begins.

The RHR consists of a First-In-First-Out (FIFO) stack with a capacity of three characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4] will be set-upon receipt of the start bit of the new (overrunning) character).

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

Table 1. SCN2681 Register Addressing

A3	A2	A1	A0	READ (RDN = 0)	WRITE (WRN = 0)
0	0	0	0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	BRG Test *	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RHRA)	Tx Holding Register A (THRA)
0	1	0	0	Input Port Change Register (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Register (CRUR)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Register (CTLR)
1	0	0	0	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	1X/16X Test	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RHRB)	Tx Holding Register B (THRB)
1	1	0	0	*Reserved*	*Reserved*
1	1	0	1	Input Port	Output Port Conf. Register (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command
1	1	1	1	Stop Counter Command	Reset Output Port Bits Command

* See Table 5 for BRG Test frequencies.

Multidrop Mode

The DUART is equipped with a wake up mode for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wakeup' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the THR.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RHR FIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems.

For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to MR1x by RESET or by issuing a 'reset pointer' command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1x, switches the pointer to MR2x. The pointer then remains at MR2x, so that subsequent accesses are always to MR2x unless the pointer is reset to MR1x as described above.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'0A' should never be read during normal operation since they are reserved for internal diagnostics.

MR1A – Channel A Mode Register 1

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRA. After reading or writing MR1A, the pointer will point to MR2A.

MR1A[7] – Channel A Receiver Request-to-Send Control

This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR1A[7] = 1 causes RTSAN to be negated upon receipt of a valid start bit if the Channel A FIFO is full. However, OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

MR1A[6] – Channel A Receiver Interrupt Select

This bit selects either the Channel A receiver ready status (RxRDY) or the Channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to be output on OP4 if it is programmed as an interrupt output via the OPCR.

MR1A[5] – Channel A Error Mode Select

This bit select the operating mode of the three FIFOed status bits (FE, PE, received break) for Channel A. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block" mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

MR1A[4:3| – Channel A Parity Mode Select

If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data MR1A[4:3] + 11 selects Channel A to operate in the special multidrop mode described in the Operation section.

MR1A[2] – Channel A Parity Type Select

This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

MR1A[1:0] – Channel A Bits Per Character Select

This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

Table 2. Register Bit Formats

	BIT 7	BIT 6	BIT 5	BIT 4 BIT 3	BIT 2	BIT 1 BIT 0
	RxRTS CONTROL	RxINT SELECT	ERROR MODE	PARITY MODE	PARITY TYPE	BITS PER CHARACTER
MR1A MR1B	0 = No 1 = Yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multidrop Mode	0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8

	BIT 7 BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	CHANNEL MODE	TxRTS CONTROL	CTS ENABLE Tx	STOP BIT LENGTH*			
MR2A MR2B	00 = Normal 01 = Auto-Echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

NOTE:
*Add 0.5 to values shown for 0 – 7 if channel is programmed for 5 bits/char.

	BIT 7 BIT 6 BIT 5 BIT 4	BIT 3 BIT 2 BIT 1 BIT 0
	RECEIVER CLOCK SELECT	TRANSMITTER CLOCK SELECT
CSRA CSRB	See Text	See Text

	BIT 7	BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		MISCELLANEOUS COMMANDS	DISABLE Tx	ENABLE Tx	DISABLE Rx	ENABLE Rx
CRA CRB	Not used – must be 0	See Text	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
*Access to the upper four bits of the command register should be separated by three (3) edges of the X1 clock.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RECEIVED BREAK*	FRAMING ERROR*	PARITY ERROR*	OVERRUN ERROR	TxEMT	TxRDY	FFULL	RxRDY
SRA SRB	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
* These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a "reset error status" command. In character mode they are discarded when the corresponding data character is read from the FIFO.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3 BIT 2	BIT 1 BIT 0
	OP7	OP6	OP5	OP4	OP3	OP2
OPCR	0 = OPR[7] 1 = TxRDYB	0 = OPR[6] 1 = TxRDYA	0 = OPR[5] 1 = RxRDY/ FFULLB	0 = OPR[4] 1 = RxRDY/ FFULLA	00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB(1x) 11 = RxCB(1x)	00 = OPR[2] 01 = TxCA(16x) 10 = TxCA(1x) 11 = RxCA(1x)

	BIT 7	BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	BRG SET SELECT	COUNTER/TIMER MODE AND SOURCE	DELTA IP 3 INT	DELTA IP 2 INT	DELTA IP 1 INT	DELTA IP 0 INT
ACR	0 = set 1 1 = set 2	See Table 4	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

Table 2. Register Bit Formats (Continued)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	DELTA IP 3	DELTA IP 2	DELTA IP 1	DELTA IP 0	IP 3	IP 2	IP 1	IP 0
IPCR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	INPUT PORT CHANGE	DELTA BREAK B	RxRDY/ FFULLB	TxRDYB	COUNTER READY	DELTA BREAK A	RxRDY/ FFULLA	TxRDYA
ISR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IN. PORT CHANGE INT	DELTA BREAK B INT	RxRDY/ FFULLB INT	TxRDYB INT	COUNTER READY INT	DELTA BREAK A INT	RxRDY/ FFULLA INT	TxRDYA INT
IMR	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]
CTUR								

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]
CTLR								

MR2A – Channel A Mode Register 2

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

MR2A[7:6] – Channel A Mode Select

Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The Channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked and the stop bits are retransmitted as received.

7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the deselection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop has been retransmitted.

MR2A[5] – Channel A Transmitter Request-to-Send Control
This bit controls the deactivation of the RTSAN output (OPO) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR2A[5] = 1 caused OPR[0] to be reset automatically one bit time after the characters in the Channel A transmit shift register and in the THR, if any, are completely transmitted including the programmed number of stop bits, if the transmitter is not enabled. This feature can be used to automatically terminate the transmission of a message as follows:

1. Program auto-reset mode: MR2A[5] = 1.
2. Enable transmitter.
3. Asset RTSAN: OPR[0] = 1.
4. Send message.
5. Verify the message is sent by waiting until the transmit ready status (TxRDY) is asserted. Disable transmitter after the last character is loaded into the Channel A THR.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

Note: When TxEMT and TxRDY bits are at one just before a write to the Transmit Holding register, a command to disable the transmitter should be delayed until the TxRDY is at one again. TxRDY will set to one at the end of the start bit time.

MR2A[4] – Channel A Clear-to-Send Control
If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IPO) each time it is ready to send a character. If IPO is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes Low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character..

MR2A[3:0] – Channel A Stop Bit Length Select
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of .563 TO 1 AND .563 to 2 bits. In increments of 0.625 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1.0625 to 2 stop bits can be programmed in increments of .0625 bit.

The receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit is enabled) in all cases.

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

MR1B – Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

MR2B – Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode registers 1 and 2 are identical to the bit definitions for MRA and MR2A except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

CSRA – Channel A Clock Select Register

CSRA[7:4] – Channel A Receiver Clock Select
This field selects the baud rate clock for the Channel A receiver as follows:

CSRA[7:4]	ACR[7] = 0	Baud Rate ACR[7] = 1
0000	50	75
0001	110	110
0010	134.5	134.5
0011	200	150
0100	300	300
0101	600	600
0110	1,200	1,200
0111	1,050	2,000
1000	2,400	2,400
1001	4,800	4,800
1010	7,200	1,800
1011	9,600	9,600
1100	38.4k	19.2k
1101	Timer	Timer
1110	IP4–16X	IP4–16X
1111	IP4–1X	IP4–1X

(See also Table 5)

The receiver clock is always a 16X clock except for CSRA[7] = 1111.

CSRA[3:0] – Channel A Transmitter Clock Select
This field selects the baud rate clock for the Channel A transmitter. The field definition is as per CSR[7:4] except as follows:

CSRA[3:0]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP3–16X	IP3–16X
1111	IP3–1X	IP3–1X

The transmitter clock is always a 16X clock except for CSR[3:0] = 1111.

CSRB – Channel B Clock Select Register

CSRB[7:4] – Channel B Receiver Clock Select
This field selects the baud rate clock for the Channel B receiver. The field definition is as per CSRA[7:4] except as follows:

CSRB[7:4]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP6–16X	IP6–16X
1111	IP6–1X	IP6–1X

The receiver clock is always a 16X clock except for CSRB[7:4] = 1111.

CSRB[3:0] – Channel B Transmitter Clock Select
This field selects the baud rate clock for the Channel B transmitter. The field definition is as per CSRA[7:4] except as follows:

CSRB[3:0]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP5–16X	IP5–16X
1111	IP5–1X	IP5–1X

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

CRA – Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

CRA[6:4] – Channel A Miscellaneous Command
The encoded value of this field may be used to specify a single command as follows:

CRA[6:4]	COMMAND
000	No command.
001	Reset MR pointer. Causes the Channel A MR pointer to point to MR1.
010	Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.
011	Reset transmitter. Resets the Channel A transmittor as if a hardware reset had been applied.
100	Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.
101	Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.
110	Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.
111	Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted.

CRA[3] – Disable Channel A Transmitter
This command terminates transmitter operation and reset the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CRA[2] – Enable Channel A Transmitter
Enables operation of the Channel A transmitter. The TxRDY status bit will be asserted.

CRA[1] – Disable Channel A Receiver
This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

CRA[0] – Enable Channel A Receiver
Enables operation of the Channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start-bit state.

CRB – Channel B Command Register

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

SRA – Channel A Status Register

SRA[7] – Channel A Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line to the marking state for at least one-half a bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the Channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

SRA[6] – Channel A Framing Error
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first bit position.

SRA[5] – Channel A Parity Error
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

In the special multidrop mode the parity error bit stores the receive A/D bit.

SRA[4] – Channel A Overrun Error
This bit, when set indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost.

This bit is cleared by a 'reset error status' command.

SRA[3] – Channel A Transmitter Empty (TxEMTA)
This bit will be set when the Channel A transmitter underruns; i.e., both the Transmit Holding Register (THR) and the transmit shift register are empty. It is set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU or when the transmitter is disabled.

SRA[2] – Channel A Transmitter Ready (TxRDYA)
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift

register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, viz., characters loaded into the THR while the transmitter is disabled will not be transmitted.

SRA[1] – Channel A FIFO Full (FFULLA)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

SRA[0] – Channel A Receiver Ready (RxRDYA)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift to the FIFO and reset when the CPU reads the RHR, if after this read there are not more characters still in the FIFO.

SRB – Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

OPCR – Output Port Configuration Register

OPCR[7] – OP7 Output Select
This bit programs the OP7 output to provide one of the following:
- The complement of OPR[7].
- The Channel B transmitter interrupt output which is the complement of TxRDYB. When in this mode OP7 acts as an Open-Collector output. Note that this output is not masked by the contents of the IMR.

OPCR[6] – OP6 Output Select
This bit programs the OP6 output to provide one of the following:
- The complement of OPR[6].
- The Channel A transmitter interrupt output which is the complement of TxRDYA. When in this mode OP6 acts as an Open-Collector output. Note that this output is not masked by the contents of the IMR.

OPCR[5] – OP5 Output Select
This bit programs the OP5 output to provide one of the following:
- The complement of OPR[5].
- The Channel B transmitter interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an Open-Collector output. Note that this output is not masked by the contents of the IMR.

OPCR[4] – OP4 Output Select
This field programs the OP4 output to provide one of the following:
- The complement of OPR[4].
- The Channel B transmitter interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an Open-Collector output. Note that this output is not masked by the contents of the IMR.

OPCR[3:2] – OP3 Output Select
This bit programs the OP3 output to provide one of the following:
- The complement of OPR[3].
- The counter/timer output, in which case OP3 acts as an Open-Collector output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
- The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

OPCR[1:0] – OP2 Output Select
This field programs the OP2 output to provide one of the following:
- The complement of OPR[2].
- The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
- The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects one of two sets of baud rates to be generated by the BRG:

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.
Set 2: 75, 110, 134.5, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, and 19.2k baud.

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table 3.

ACR[6:4] – Counter/Timer Mode And Clock Source Select
This field selects the operating mode of the counter/timer and its clock source as shown in Table 4.

ACR[3:0] – IP3, IP2, IP1, IP0 Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7:4] – IP3, IP2, IP1, IP0 Change-of-State
These bits are set when a change-of-state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – IP3, IP2, IP1, IP0 Current State
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR – the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to 00_{16} when the DUART is reset.

ISR[7] – Input Port Change Status
This bit is a '1' when a change-of-state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

ISR[6] – Channel B Change In Break
This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel B 'reset break change interrupt' command.

ISR[5] – Channel B Receiver Ready or FIFO Full
The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that a character has been received in Channel B and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel B FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

ISR[4] – Channel B Transmitter Ready
This bit is a duplicate of TxRDYB (SRB[2]).

ISR[3] – Counter Ready.
In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

ISR[2] – Channel A Change In Break
This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

ISR[1] – Channel A Receiver Ready Or FIFO Full
The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that a character has been received in Channel A and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU read the RHR. IF after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel A FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the ISR[0] and IMR waiting character is loaded into the FIFO.

ISR[0] – Channel A Transmitter Ready
This bit is a duplicate of TxRDYA (SRA[2]).

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3–OP7 or the reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is 0002_{16}. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the CT generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR.

If the value in CTUR and CTLR is changed, the current half-period will not be affected, but subsequent half periods will be. In this mode the C/T runs continuously. Receipt of a start counter command (read with A3-A0 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR. The waveform so generated is often used for a data clock. The formula for calculating the divisor n to load to the CTUR and CTLR for a particular 1X data clock is shown below:

$$n = \frac{C/T\ Clock\ Frequency}{2 \cdot 16 \cdot Baud\ rate\ desired}$$

Often this division will result in a non-integer number; 26.03, for example. One can only program integer numbers in a digital divider. Therefore, 26 would be chosen. This gives a baud rate error of 0.03/26.3 which is .114%; well within the ability asynchronous mode of operation.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3-A0 = 1111). The command however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

On power up and after reset, the timer/counter runs in timer mode and can only be restarted. Because it cannot be shut off or stopped, and runs continuously in timer mode, it is recommended that at initialization, the output port (OP3) should be masked off through the OPCR[3:2] = 00 until the T/C is programmed to the desired operational state.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a counter command. Upon reaching terminal count (0000_{16}), the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command. If new values have not been loaded, the previous count values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU.

It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

Table 3. Bit Rate Generator Characteristics Crystal or Clock = 3.6864MHz

NORMAL RATE (BAUD)	ACTUAL 16x CLOCK (kHz)	ERROR (%)
50	0.8	0
75	1.2	0
110	1.759	-0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	-0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2k	307.2	0
38.4k	614.4	0

NOTE: Duty cycle of 16x clock is 50% ± 1%.

Table 4. ACR 6:4 Field Definition

ACR 6:4	MODE	CLOCK SOURCE
000	Counter	External (IP2)
001	Counter	TxCA – 1x clock of Channel A transmitter
010	Counter	TxCB – 1x clock of Channel B transmitter
011	Counter	Crystal or external clock (x1/CLK) divided by 16
100	Timer	External (IP2)
101	Timer	External (IP2) divided by 16
110	Timer	Crystal or external clock (x1/CLK)
111	Timer	Crystal or external clock (x1/CLK) divided by 16

TIMING DIAGRAMS

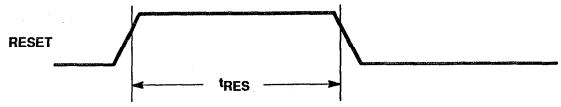


Figure 1. Reset Timing

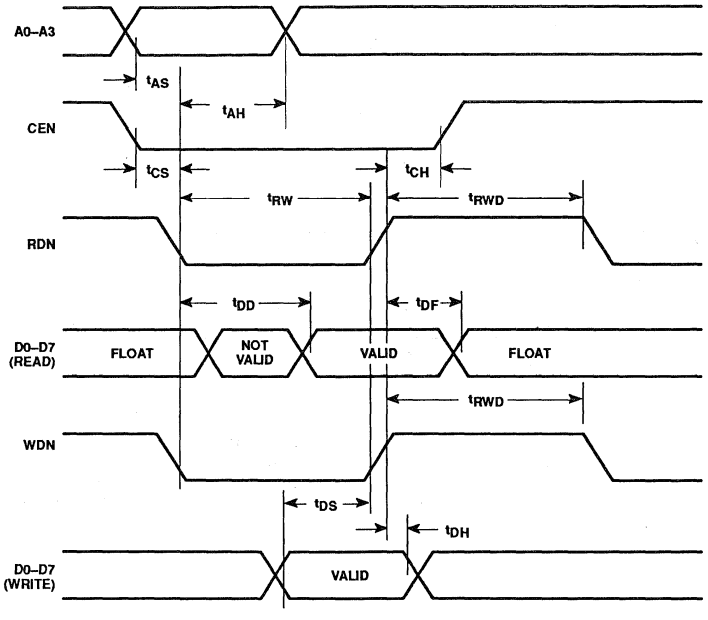


Figure 2. Bus Timing

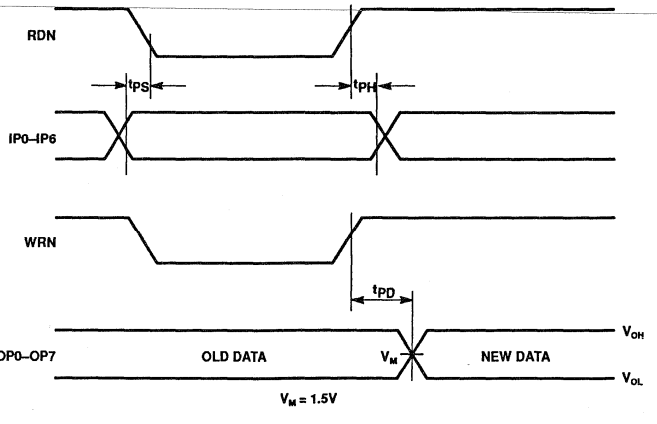
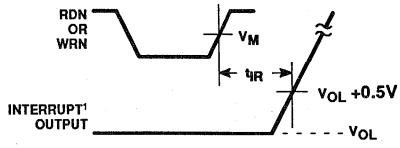


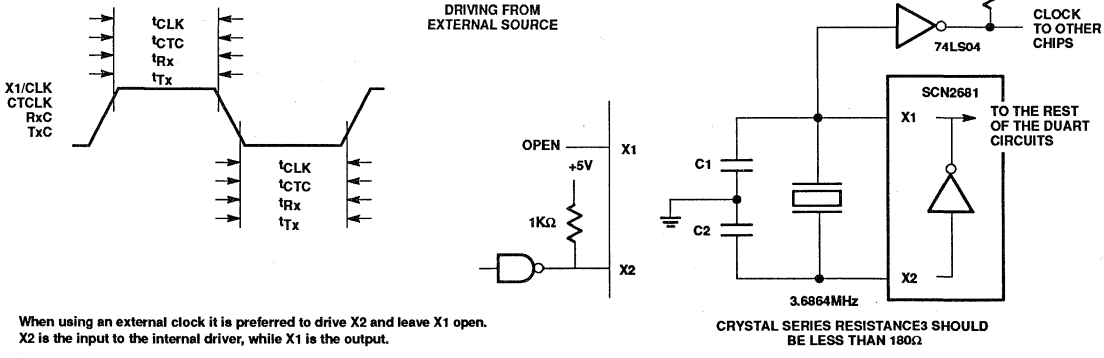
Figure 3. Port Timing



NOTES:

1. INTRN or OP3 – OP7 when used as interrupt outputs.
2. The test for open-drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from themidpoint of the switching signal, V_M, to a point 0.5V above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 4. Interrupt Timing



When using an external clock it is preferred to drive X2 and leave X1 open. X2 is the input to the internal driver, while X1 is the output.

CRYSTAL SERIES RESISTANCE3 SHOULD BE LESS THAN 180Ω

Figure 5. Clock Timing

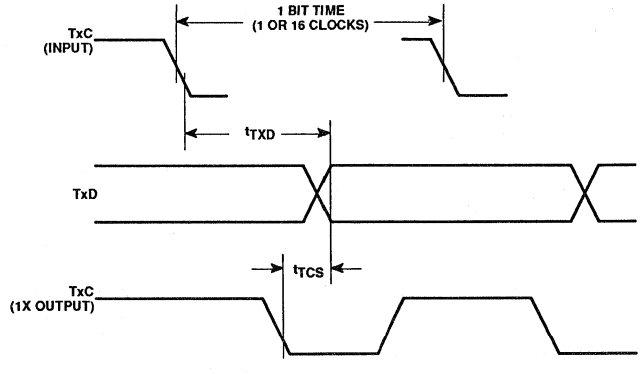


Figure 6. Transmit

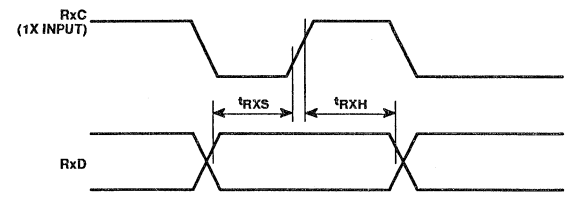
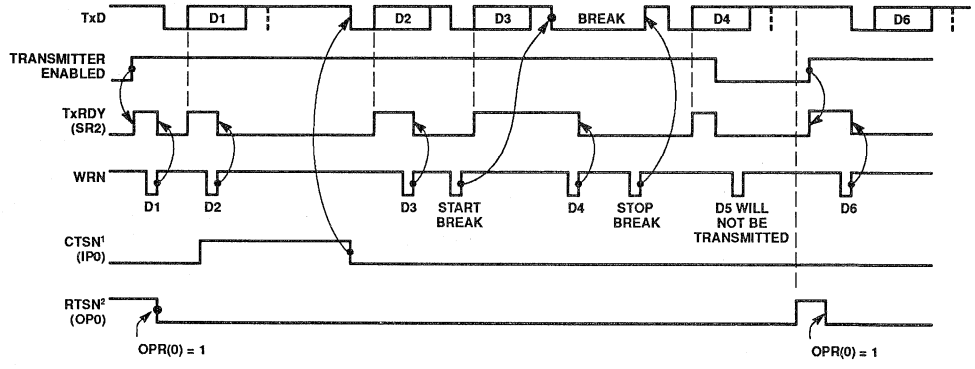
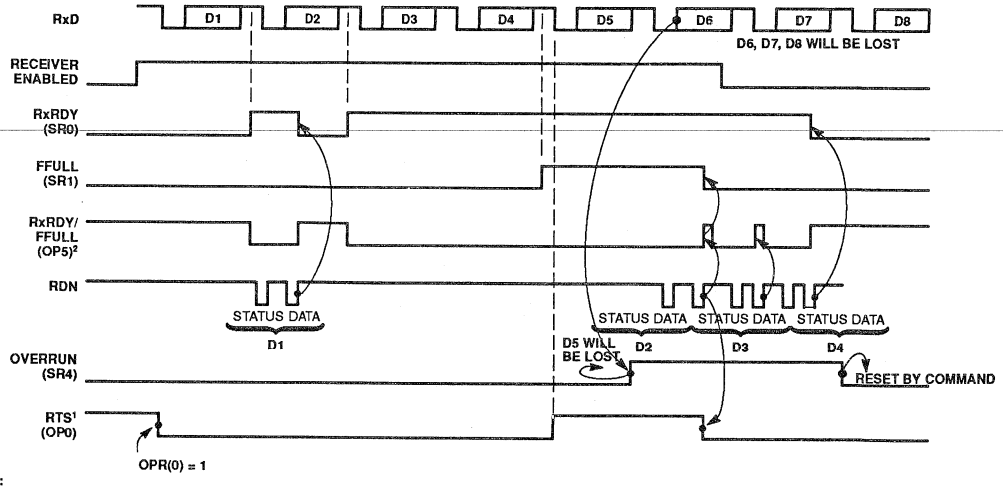


Figure 7. Receive



NOTES:
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

Figure 8. Transmitter Timing



NOTES:
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) = 1 and MR(6) = 0.

Figure 9. Receiver Timing

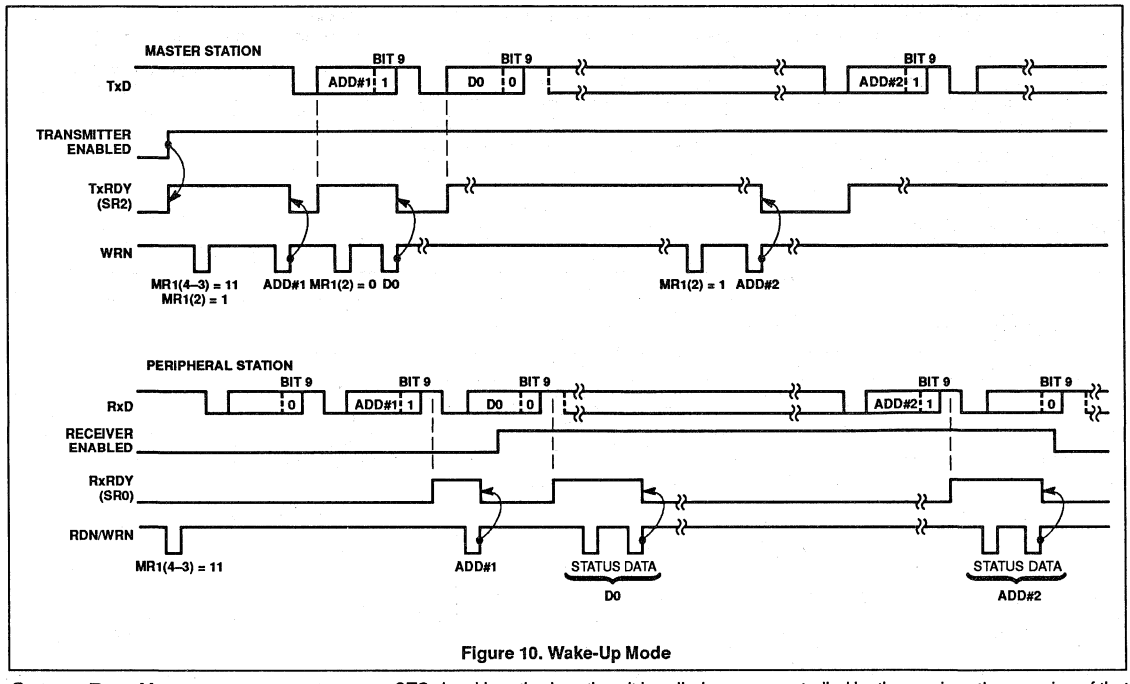


Figure 10. Wake-Up Mode

Output Port Notes

The output ports are controlled from three places: the OPCR register, the OPR register, and the MR registers. The OPCR register controls the source of the data for the output ports OP2 through OP7. The data source for output ports OP0 and OP1 is controlled by the MR and CR registers. When the OPR is the source of the data for the output ports, the data at the ports is inverted from that in the OPR register. The content of the OPR register is controlled by the "Set Output Port Bits Command" and the "Reset Output Bits Command". These commands are at E and F, respectively. When these commands are used, action takes place only at the bit locations where ones exist. For example, a one in bit location 5 of the data word used with the "Set Output Port Bits" command will result in OPR5 being set to one. The OP5 would then be set to zero (V_{SS}). Similarly, a one in bit position 5 of the data word associated with the "Reset Output Ports Bits" command would set OPR5 to zero and, hence, the pin OP5 to a one (V_{DD}).

The CTS, RTS, CTS Enable Tx signals

CTS (Clear To Send) is usually meant to be a signal to the transmitter meaning that it may transmit data to the receiver. The CTS input is on pin IP0 for TxA and on IP1 for TxB. The CTS signal is active low; thus, it is called CTSAN for TxA and CTSBN for TxB.

RTS is usually meant to be a signal from the receiver indicating that the receiver is ready to receive data. It is also active low and is, thus, called RTSAN for RxA and RTSBN for RxB. RTSAN is on pin op0 and RTSBN is on OP1. A receiver's RTS output will usually be connected to the CTS input of the associated transmitter. Therefore, one could say that RTS and CTS are different ends of the same wire!

MR2(4) is the bit that allows the transmitter to be controlled by the CTS pin (IP0 or IP1). When this bit is set to one AND the CTS input is driven high, the transmitter will stop sending data at the end of the present character being serialized. It is usually the RTS output of the receiver that will be connected to the transmitter's CTS input. The receiver will set RTS high when the receiver FIFO is full AND the start bit of the fourth character is sensed. Transmission then stops with four valid characters in the receiver. When MR2(4) is set to one, CTSN must be at zero for the transmitter to operate. If MR2(4) is set to zero, the IP pin will have no effect on the operation of the transmitter.

MR1(7) is the bit that allows the receiver to control OP0. When OP0 (or OP1) is controlled by the receiver, the meaning of that pin will be RTS. However, a point of confusion arises in that OP0 (or OP1) may also be controlled by the transmitter. When the transmitter is controlling this pin, its meaning is not RTS at all. It is, rather, that the transmitter has finished sending its last data byte. Programming the OP0 or OP1 pin to be controlled by the receiver and the transmitter at the same time is allowed, but would usually be incompatible.

RTS is expressed at the OP0 or OP1 pin which is still an output port. Therefore, the state of OP0 or OP1 should be set low for the receiver to generate the proper RTS signal. The logic at the output is basically a NAND of the OPR register and the RTS signal as generated by the receiver. When the RTS flow control is selected via the MR(7) bit state of the OPR register is not changed. Terminating the use of "Flow Control" (via the MR registers) will return the OP0 or OP1 pins to the control of the OPR register.

Transmitter Disable Note

The sequence of instructions enable transmitter — load transmit holding register — disable transmitter will result in nothing being sent if the time between the end of loading the transmit holding register and the disable command is less that 3/16 bit time in

the 16x mode or one bit time in the 1x mode. Also, if the transmitter, while in the enabled state and underrun condition, is immediately disabled after a single character is loaded to the transmit holding register, that character will not be sent.

In general, when it is desired to disable the transmitter before the last character is sent AND the TxEMT bit is set in the status register (TxEMT is always set if the transmitter has underrun or has just been enabled), be sure the TxRDY bit is active immediately before issuing the transmitter disable instruction. TxRDY sets at the end of the "start bit" time. It is during the start bit that the data in the transmit holding register is transferred to the transmit shift register.

Non-standard baud rates are available as shown in Table [5] below, via the BRG Test function.

Table 5. Baud Rate

	Normal BRG		BRG Test	
CSR[7:4]	**ACR[7] = 0**	**ACR[7] = 1**	**ACR[7] = 0**	**ACR[7] = 1**
0000	50	75	4,800	7,200
0001	110	110	880	880
0010	134.5	38.4K	1,076	38.4K
0011	200	150	19.2K	14.4K
0100	300	300	28.8K	28.8K
0101	600	600	57.6K	57.6K
0110	1,200	1,200	115.2K	115.2K
0111	1,050	2,000	1,050	2,000
1000	2,400	2,400	57.6K	57.6K
1001	4,800	4,800	4,800	4,800
1010	7,200	1,800	57.6K	14.4K
1011	9,600	9,600	9,600	9,600
1100	38.4K	19.2K	38.4K	19.2K
1101	Timer	Timer	Timer	Timer
1110	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X
1111	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X

NOTE:
Each read on address H'2' will toggle the baud rate test mode. When in the BRG test mode, the baud rates change as shown to the left. This change affects all receivers and transmitters on the DUART. Also, the RTSN outputs (OP[0] and OP[1]) become the transmitter 1x clock.

The test mode at address H'A' changes all transmitters and receivers to the 1x mode and connects the output ports to some internal nodes.

Dual asynchronous receiver/transmitter (DUART) SCN2681T

DESCRIPTION

The Signetics SCN2681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. The SCN2681T features a faster bus cycle time than the standard SCN2681. The quick bus cycle eliminates or reduces the need for wait states with fast CPUs and permits high throughput in I/O intensive systems. Higher external clock rates may be used with the transmitter, receiver and counter timer which in turn provide greater versatility in baud rate generation. The SCN2681T interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruple buffered to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the receiver buffer is full.

Also provided on the SCN2681T are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

For a complete functional description and programming information for the SCN2681T, refer to the SCN2681 product specification.

FEATURES

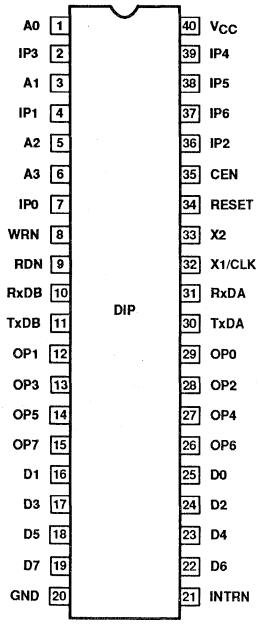
- Fast bus cycle times reduce or eliminate CPU wait states
- Dual full-duplex asynchronous receiver/transmitters
- Quadruple buffered receiver data registers
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4k baud
  - Non-standard rates to 115.2
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function programmable 16-bit counter/timer
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer rates:
  1X – 1MB/sec transmitter and receiver;
  16X – 500kB/sec receiver and 250kB/sec transmitter
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Single +5V power supply
- Commercial and industrial temperature ranges available

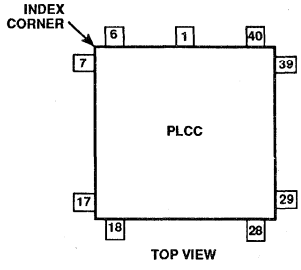
ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±10%, T_A = 0°C to +70°C
40-Pin Plastic DIP (600mil-wide DIP)	SCN2681TC1N40A
44-Pin Plastic LCC	SCN2681TC1A44A

NOTE: For a full register description and programming information see the SCN2681.

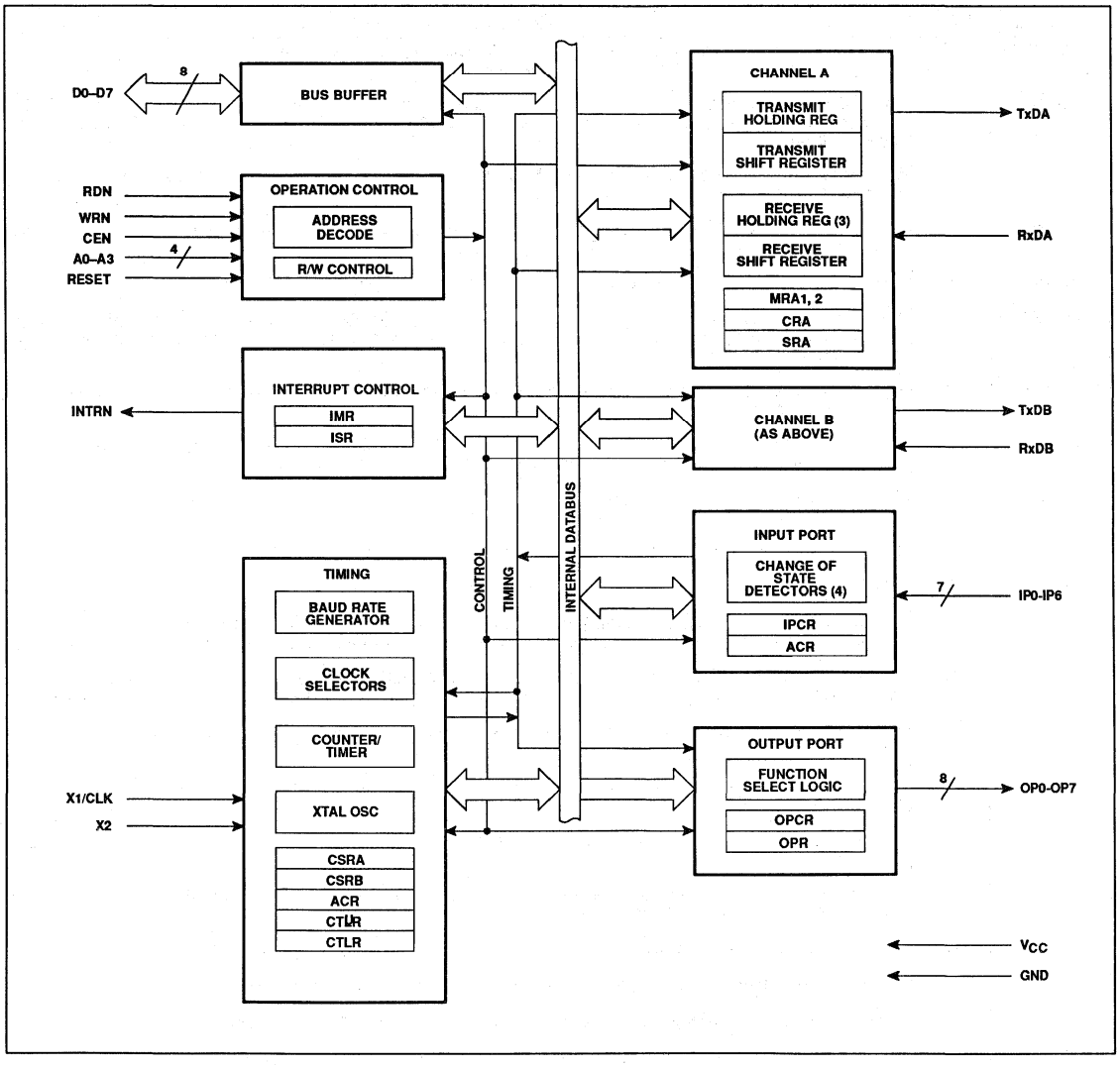
PIN CONFIGURATIONS





PIN/FUNCTION		PIN/FUNCTION	
1	NC	23	NC
2	A0	24	INTRN
3	IP3	25	D6
4	A1	26	D4
5	IP1	27	D2
6	A2	28	D0
7	A3	29	OP6
8	IP0	30	OP4
9	WRN	31	OP2
10	RDN	32	OP0
11	RxDB	33	TxDA
12	NC	34	NC
13	TxDB	35	RxDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CEN
18	D1	40	IP2
19	D3	41	IP6
20	D5	42	IP5
21	D7	43	IP4
22	GND	44	V_{CC}

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	TYPE	NAME AND FUNCTION
D0–D7	I/O	**Data Bus:** Bidirectional three-state data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	I	**Chip Enable:** Active low input signal. When low, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the WRN, RDN, and A0–A3 inputs. When CEN is high, the DUART places the D0–D7 lines in the three-state condition.
WRN	I	**Write Strobe:** When low and CEN is also low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	I	**Read Strobe:** When low and CEN is also low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0–A3	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	I	**Reset:** A high level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0–OP7 in the high state, stops the counter/timer, and puts channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (high) state. Clears Test modes.
INTRN	O	**Interrupt Request:** Active-low, open-drain output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5).
X2	I	**Crystal 2:** Connection for other side of crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5). If X1/CLK is driven from an external source, this pin should be grounded.
RxDA	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. 'Mark' is high, 'space' is low.
RxDB	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. 'Mark' is high, 'space' is low.
TxDA	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is high, 'space' is low.
TxDB	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is high, 'space' is low.
OP0	O	**Output 0:** General purpose output, or channel A request to send (RTSAN, active-low). Can be deactivated automatically on receive or transmit.
OP1	O	**Output 1:** General purpose output, or channel B request to send (RTSBN, active-low). Can be deactivated automatically on receive or transmit.
OP2	O	**Output 2:** General purpose output, or channel A transmitter 1X or 16X clock output, or channel A receiver 1X clock output.
OP3	O	**Output 3:** General purpose output, or open-drain, active-low counter/timer output, or channel B transmitter 1X clock output, or channel B receiver 1X clock output.
OP4	O	**Output 4:** General purpose output, or channel A open-drain, active-low, RxRDYA/FFULLA output.
OP5	O	**Output 5:** General purpose output, or channel B open-drain, active-low, RxRDYB/FFULLB output.
OP6	O	**Output 6:** General purpose output, or channel A open-drain, active-low, TxRDYA output.
OP7	O	**Output 7:** General purpose output, or channel B open-drain, active-low TxRDYB output.
IP0	I	**Input 0:** General purpose input, or channel A clear to send active-low input (CTSAN).
IP1	I	**Input 1:** General purpose input, or channel B clear to send active-low input (CTSBN).
IP2	I	**Input 2:** General purpose input, or counter/timer external clock input.
IP3	I	**Input 3:** General purpose input, or channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	I	**Input 4:** General purpose input, or channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.

PIN DESCRIPTION (Continued)

MNEMONIC	TYPE	NAME AND FUNCTION
IP5	I	**Input 5:** General purpose input, or channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6	I	**Input 6:** General purpose input, or channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
V_{CC}	I	**Power Supply:** +5V supply input.
GND	I	**Ground**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
	All voltages with respect to GND[3]	-0.5 to +6.0	V

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage (except X1/CLK)		2.0			V
V_{IH}	Input high voltage (X1/CLK)		3.5			V
V_{OL}	Output low voltage	I_{OL} = 2.4mA			0.4	V
V_{OH}	Output high voltage (except o.c. outputs)[4]	I_{OH} = -400µA	2.4			V
I_{IL}	Input leakage current	V_{IN} = 0 to V_{CC}	-10		10	µA
I_{LL}	Data bus 3-state leakage current	V_O = 0.4 to V_{CC}	-10		10	µA
I_{X1L}	X1/CLK low input current	V_{IN} = 0, X2 grounded	-4	-2	0	mA
		V_{IN} = 0, X2 floated	-3	-1.5	0	mA
I_{X1H}	X1/CLK high input current	V_{IN} = V_{CC}, X2 = grounded	-1	0.2	1	mA
		V_{IN} = V_{CC}, X2 floated	0	3.5	10	mA
I_{X2L}	X2 low input current	V_{IN} = 0, X1/CLK floated	-100	-30	0	µA
I_{X2H}	X2 high input current	V_{IN} = V_{CC}, X1/CLK floated	0	+30	100	µA
I_{OC}	Open-collector output leakage current	V_O = 0.4 to V_{CC}	-10		10	µA
I_{CC}	Power supply current[5] 0°C to +70°C version				150	mA

NOTES:
1. Parameters are valid over specified temperature range. See Ordering information table for applicable operating temperature range and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.0V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
5. For bus operations, CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.

AC ELECTRICAL CHARACTERISTICS[1, 2, 3, 4]

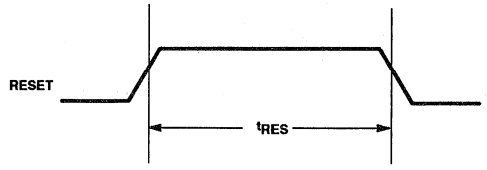


Figure 1. Reset Timing

NOTES:
1. Parameters are valid over specified temperature range. See Ordering information table for applicable operating temperature range and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.0V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{RES}	Reset pulse width	1.0		µs

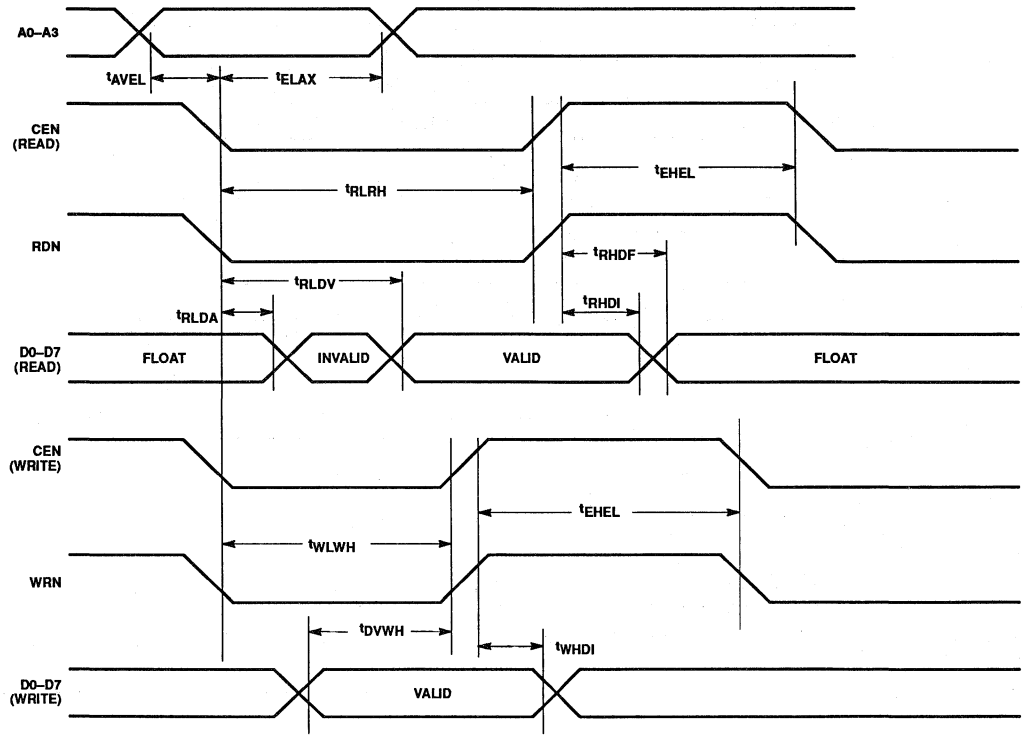


Figure 2. Bus Timing

SYMBOL	PARAMETER[1]	LIMITS		UNIT
		Min	Max	
t_{AVEL}	A0–A3 setup to RDN and CEN, or WRN and CEN low	0		ns
t_{ELAX}	RDN and CEN, or WRN and CEN low to A0–A3 invalid	100		ns
t_{RLRH}	RDN and CEN low to RDN or CEN high	120		ns
t_{EHEL}	CEN high to CEN low[2, 3]	110		ns
t_{RLDA}	CEN and RDN low to data outputs active	15		ns
t_{RLDV}	CEN and RDN low to data valid		100	ns
t_{RHDI}	CEN or RDN high to data invalid	10		ns
t_{RHDF}	CEN or RDN high to data outputs floating		65	ns
t_{WLWH}	WRN and CEN low to WRN or CEN high	75		ns
t_{DVWH}	Data input valid to WRN or CEN high	35		ns
t_{WHDI}	WRN or CEN high to data invalid	15		ns

NOTES:

1. For bus operations, CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
2. If CEN is used as the 'strobing' input, the parameter defines the minimum high times between one CEN and the next. The RDN signal must be negated for t_{EHEL} to guarantee that any status register changes are valid. As a consequence, this minimum time must be met for the RDN input even if the CEN is used as the strobing signal for bus operations.
3. Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.

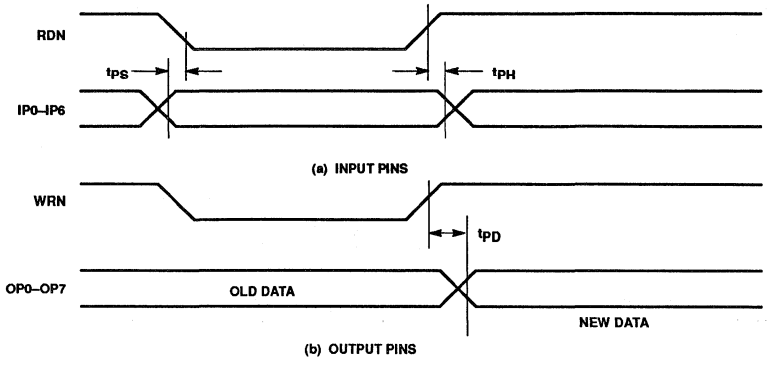
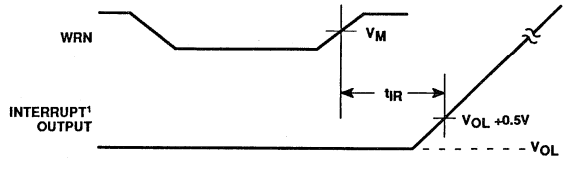


Figure 3. Port Timing

SYMBOL	PARAMETER[1]	LIMITS Min	LIMITS Max	UNIT
t_{PS}	Port input setup time before RDN low	0		ns
t_{PH}	Port input hold time after RDN high	0		ns
t_{PD}	Port output valid after WRN high		200	ns

NOTE:
1. For bus operations, CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.



NOTES:
1. INTRN or OP3-OP7 when used as interrupt outputs.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from the midpoint of the switching signal, V_M, to a point 0.5V above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 4. Interrupt Timing

SYMBOL	PARAMETER	LIMITS Min	LIMITS Max	UNIT
t_{IR}	INTRN (or OP3–OP7 when used as interrupts) negated from:			
	Read RHR (RxRDY/FFULL interrupt)		200	ns
	Write THR (TxRDY i nterrupt)		200	ns
	Reset command (delta break interrupt)		200	ns
	Stop C/T command (counter interrupt)		200	ns
	Read IPCR (input port change interrupt)		200	ns
	Write IMR (clear of interrupt mask bit)		200	ns

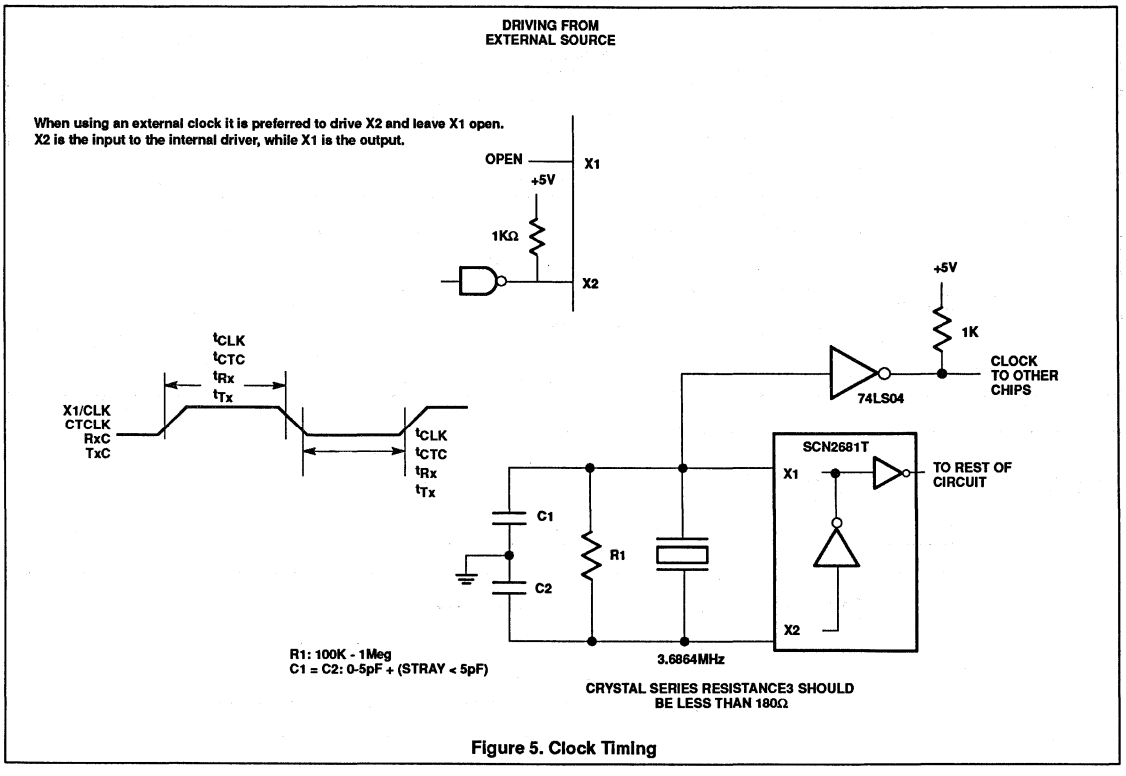


Figure 5. Clock Timing

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
t_{CLK}	X1/CLK high or low time	90			ns
f_{CLK}	X1/CLK frequency	2	3.686	4	MHz
t_{CTC}	CTCLK (IP2) high or low time	55	4		ns
f_{CTC}	CTCLK (IP2) frequency[1]	0		8	MHz
t_{RX}	RxC high or low time	55			ns
f_{RX}	RxC frequency (16X)[1]	0		8	MHz
t_{TX}	(1X)[1]	0		1	MHz
f_{TX}	TxC high or low time	110			ns
	TxC frequency (16X)[1]	0		4	MHz
	(1X)[1]	0		1	MHz

NOTE:
1. Minimum frequencies are not tested but are guaranteed by design.

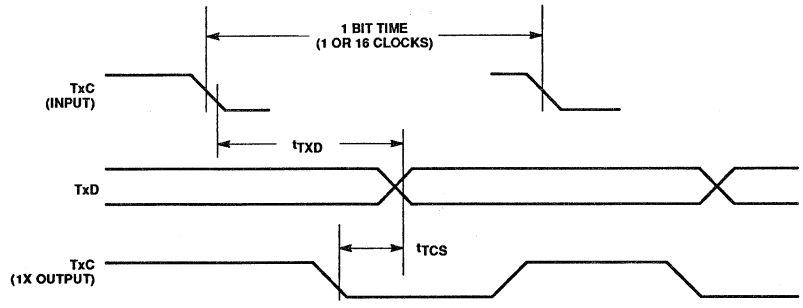


Figure 6. Transmit

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{TXD}	TxD output delay from TxC low		300	ns
t_{TCS}	Output delay from TxC low to TxD data output	0	100	ns

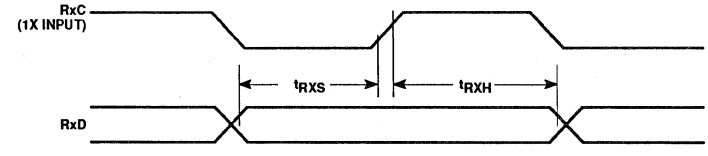
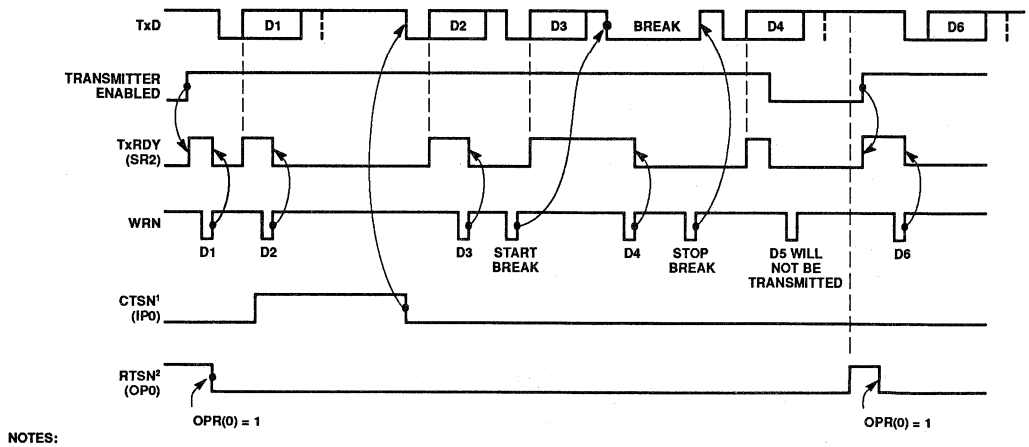


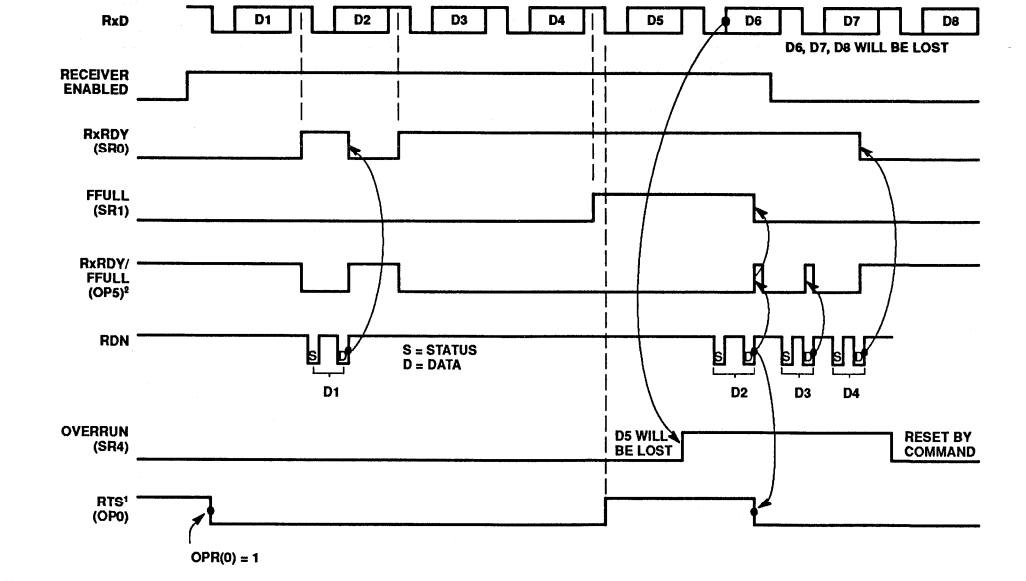
Figure 7. Receive

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{RXS}	RxD data setup time to RxC high	200		ns
t_{RXH}	RxD data hold time from RxC high	25		ns



NOTES:
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

Figure 8. Transmitter Timing



NOTES:
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) = 1 and MR1(6) = 0.

Figure 9. Receiver Timing

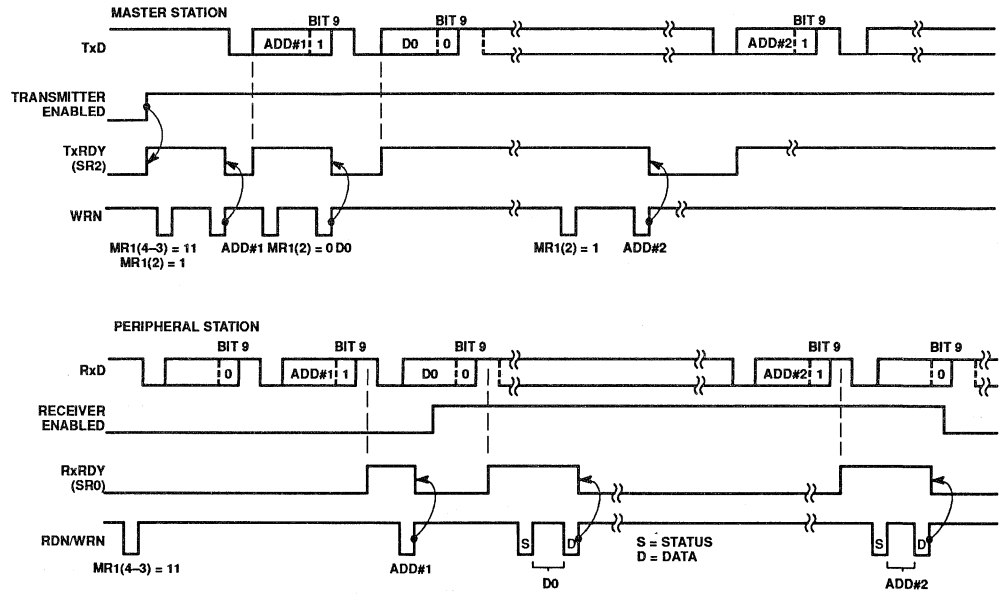


Figure 10. Wake-Up Mode

Dual asynchronous receiver/transmitter (DUART) SCN68681

DESCRIPTION

The Signetics SCN68681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. It is compatible with other S68000 family devices, and can also interface easily with other microprocessors. The DUART can be used in polled or interrupt driven systems.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

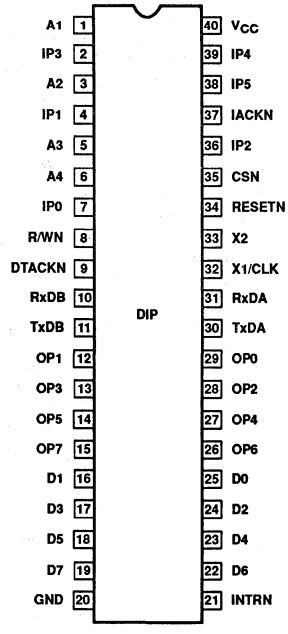
FEATURES

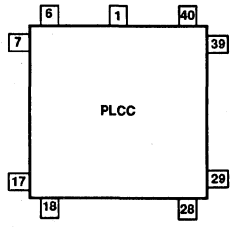
- S68000 bus compatible
- Dual full-duplex asynchronous receiver/transmitter
- Quadruple buffered receiver data registers
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4k baud
  - Non-standard rates to 115.2kb
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function programmable 16-bit counter/timer
- Multi-function 6-bit input port
  - Can serve as clock or control inputs
  - Change-of-state detection on four inputs
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Interrupt vector output on interrupt acknowledge
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer rates: 1X - 1MB/sec, 16X - 125kB/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Single +5V power supply
- Commercial and industrial temperature ranges available
- DIP and PLCC packages

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	
	V_{CC} = +5V +5%, T_A = 0°C to +70°C	V_{CC} = +5V +10%, T_A = 40°C to +85°C
40-Pin Ceramic DIP	Not available	SCN68681E1F40
40-Pin Plastic DIP	SCN68681C1N40	SCN68681E1N40
44-Pin Plastic LCC	SCN68681CIA44	SCN68681E1A44

PIN CONFIGURATIONS

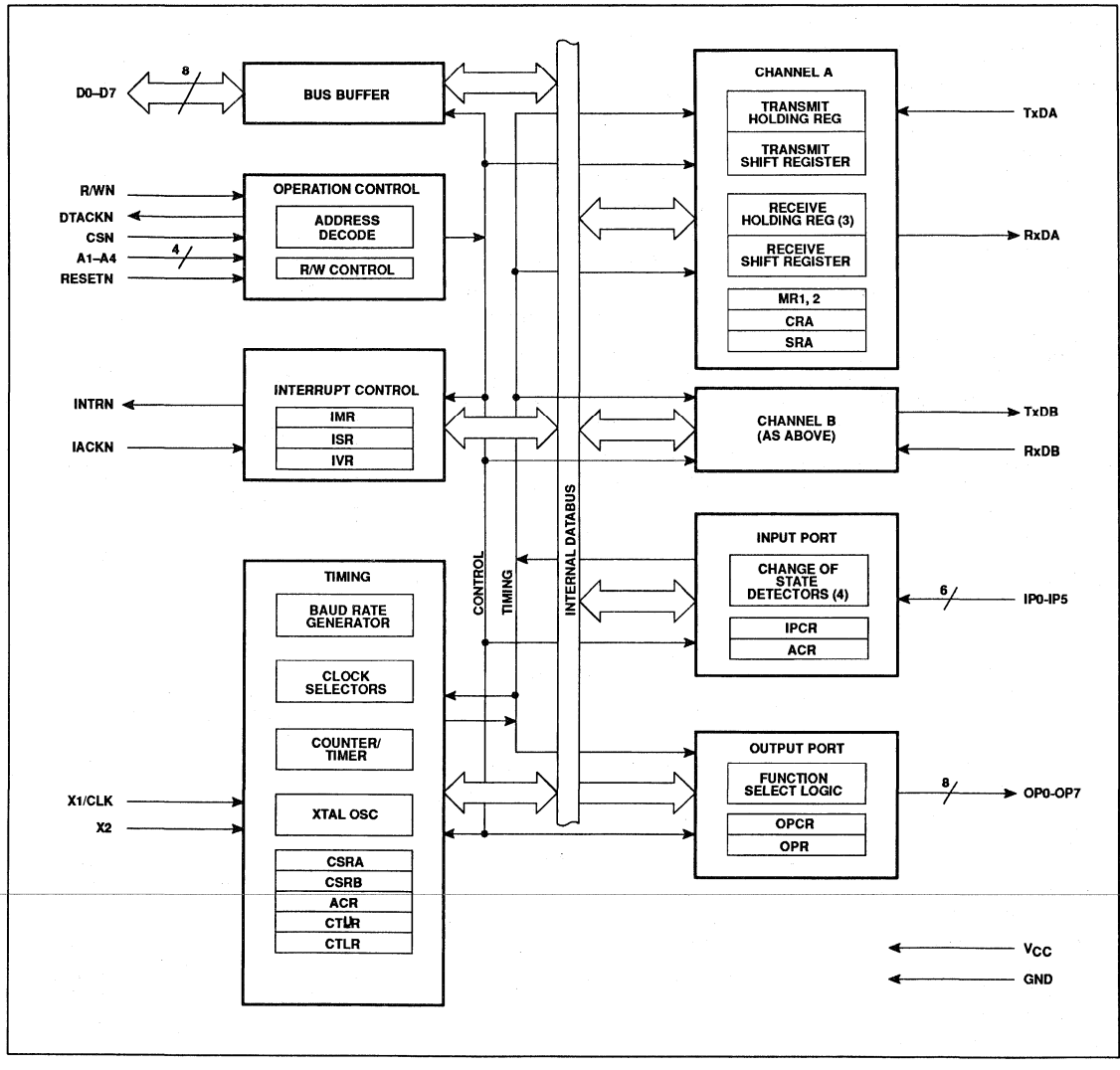




PIN/FUNCTION

1	NC	16	OP5	31	OP2
2	A1	17	OP7	32	OP0
3	IP3	18	D1	33	TxDA
4	A2	19	D3	34	NC
5	IP1	20	D5	35	RxDA
6	A3	21	D7	36	X1/CLK
7	A4	22	GND	37	X2
8	IP0	23	NC	38	RESETN
9	R/WN	24	INTRN	39	CSN
10	DTACKN	25	D6	40	IP2
11	RxDB	26	D4	41	IACKN
12	NC	27	D2	42	IP5
13	TxDB	28	D0	43	IP4
14	OP1	29	OP6	44	VCC
15	OP3	30	OP4		

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	TYPE	NAME AND FUNCTION
D0-D7	I/O	**Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CSN	I	**Chip Select:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the R/WN, RDN and A1-A4 inputs. When High, places the D0-D7 lines in the 3-State condition.
R/WN	I	**Read/Write:** A High input indicates a read cycle and a Low input indicates a write cycle, when a cycle is initiated by assertion of the CSN input.
A1-A4	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESETN	I	**Reset:** A Low level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), initializes the IVR to hex 0F, puts OP0-OP7 in the High state, stops the coutner/timer, and puts Channel A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Clears Test modes.
DTACKN	O	**Data Transfer Acknowledge:** Three-state active Low output asserted in write, read, or interrupt cycles to indicate proper transfer of data between the CPU and the DUART.
INTRN	O	**Interrupt Request:** Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
IACKN	I	**Interrupt Acknowledge:** Active-Low input indicating an interrupt acknowledge cycle. In response, the DUART will place the interrupt vector on the data bus and will assert DTACKN if it has an interrupt pending.
X1/CLK	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. If a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7).
X2	I	**Crystal 2:** Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7). If an external clock is used, this pin should be grounded.
RxDA	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
TxDB	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is High, 'space' is Low.
OP0	O	**Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	O	**Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	O	**Output 2:** General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	O	**Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	O	**Output 4:** General purpose output or Channel A open-drain, active-Low, RxRDYA/FFULLA output.
OP5	O	**Output 5:** General purpose output or Channel B open-drain, active-Low, RxRDYB/FFULLB output.
OP6	O	**Output 6:** General purpose output or Channel A open-drain, active-Low, TxRDYA output.
OP7	O	**Output 7:** General purpose output, or Channel B open-drain, active-Low, TxRDYB output.
IP0	I	**Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	I	**Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	I	**Input 2:** General purpose input, or Channel B receiver external clock input (RxCB), or counter/timer external clock input. When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP3	I	**Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	I	**Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	I	**Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
V_{CC}	I	**Power Supply:** +5V supply input.
GND	I	**Ground:**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	See Note 4	°C
T_{STG}	Storage temperature range	-65 to +150	°C
	All voltages with respect to ground[3]	-0.5 to +6.0	V

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range. See Ordering information table for applicable operating temperature range and V_{CC} supply range.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage (except X1/CLK)[5]		2			V
V_{IH}	Input high voltage (except X1/CLK)[4]		2.5			V
V_{IH}	Input high voltage (X1/CLK)		4			V
V_{OL}	Output low voltage	I_{OL} = 2.4mA			0.4	V
V_{OH}	Output high voltage (except o.d. outputs)[5]	I_{OH} = -400µA	2.4			V
V_{OH}	Output high voltage (except o.d. outputs)[4]	I_{OH} = -400µA	2.9			V
I_{IL}	Input leakage current	V_{IN} = 0 to V_{CC}	–10		10	µA
I_{LL}	Data bus 3-State leakage current	V_O = 0.4 to V_{CC}	–10		10	µA
I_{X1L}	X1/CLK low input current	V_{IN} = 0, X2 grounded	-4	-2	0	mA
		V_{IN} = 0, X2 floated	-3	-1.5	0	mA
I_{X1H}	X1/CLK high input current	V_{IN} = V_{CC}, X2 grounded	-1	0.2	1	mA
		V_{IN} = V_{CC}, X2 floated	0	3.5	10	mA
I_{X2L}	X2 low input current	V_{IN} = 0, X1/CLK floated	-100	-30	0	µA
I_{X2H}	X2 high input current	V_{IN} = V_{CC}, X1/CLK floated	0	+30	100	µA
I_{OC}	Open-collector output leakage current	V_O = 0.4 to V_{CC}	–10		10	µA
I_{CC}	Power supply current					
	0°C to +70°C version				150	mA
	-40°C to +85°C version				175	mA

NOTES:
1. Parameters are valid over specified temperature range. See Ordering information table for applicable operating temperature range and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. T_A < 0°C
5. $T_A \geq$ 0°C

AC CHARACTERISTICS T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10% [1, 2, 3, 4]

SYMBOL	PARAMETER	LIMITS Min	Typ[3]	Max	UNIT
Reset Timing (See Figure 1)					
t_{RES}	RESETN pulse width	200			ns
Bus Timing (See Figures 2, 3 4)					
t_{AS}	A1-A4 setup time to CSN Low	10			ns
t_{AH}	A1-A4 hold time from CSN Low	100			ns
t_{RWS}	RWN setup time to CSN High	0			ns
t_{RWH}	RWN holdup time to CSN High	0			ns
t_{CSW}	CSN High pulse width	90			ns
t_{CSD}[5]	CSN or IACKN High from DTACKN Low	20			ns
t_{DD}	Data valid from CSN or IACKN Low			175	ns
t_{DF}	Data bus floating from CSN or IACKN High[7]			100	ns
t_{DS}	Data setup time to CLK High	100			ns
t_{DH}	Data hold time from CSN High	20			ns
t_{DAL}	DTACKN Low from read data valid	0			ns
t_{DCR}	DTACKN Low (read cycle) from CLK High			125	ns
t_{DCW}	DTACKN Low (write cycle) from CLK High			125	ns
t_{DAH}	DTACKN High from CSN or IACKN High			100	ns
t_{DAT}	DTACKN High imepdance from CSN or IACKN High			125	ns
t_{CSC}[6]	CSN or IACKN setup time to clock High	90			ns
Port Timing (See Figure 5)					
t_{PS}	Port input setup time to CSN Low	0			ns
t_{PH}	Port input hold time from CSN High	0			ns
t_{PD}	Port output valid from CSN High			400	ns
Interrupt Reset Timing (See Figure 6)					
t_{IR}	INTRN or OP3-OP7 when used as interrupts negated from:				
	Read RHR (RxRDY/FFULL interrupt)			300	ns
	Write THR (TxRDY interrupt)			300	ns
	Reset command (delta break interrupt)			300	ns
	Stop C/T command (counter interrupt)			300	ns
	Read IPCR (input port change interrupt)			300	ns
	Write IMR (clear of interrupt mask bit)			300	ns
Clock Timing (See Figure 7)					
t_{CLK}	X1/CLK High or Low time	100			ns
f_{CLK}	X1/CLK frequency	0[8]	3.6864	4.0	MHz
t_{CTC}	CTCLK High or Low time	100			ns
f_{CTC}	CTCLK frequency	0		4.0	MHz
t_{RX}	RxC High or Low time	220			ns
f_{RX}	RxC frequency (16X)	0		2.0	MHz
	(1X)	0		1.0	MHz
t_{TX}	TxC High or Low time	220			ns
f_{TX}	TxC frequency (16X)	0		2.0	MHz
	(1X)	0		1.0	MHz
Transmitter Timing (See Figure 8)					
t_{TXD}	TxD output delay from TxC Low			350	ns
t_{TCS}	Output delay from TxC Low to TxD data output			150	ns
Receiver Timing (See Figure 9)					
t_{RXS}	RxD data setup time to RxC High	240			ns
t_{RXH}	RxD data hold time from RxC High	200			ns

NOTES:

1. Parameters are valid over specified temp. range. See Ordering information table for applicable operating temp. range and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test condition for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
5. This specification will impose maximum 68000 CPU CLK to 6MHz. Higher CPU CLK can be used if repeating bus reads are not performed. Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.
6. This specification imposes a lower bound on CSN and IACKN Low, guaranteeing that it will be Low for at least 1 CLK period. This requirement is made on CSN only to insure assertion of DTACKN and not to guarantee operation of the part.
7. This spec is made only to insure that DTACKN is asserted with respect to the rising edge of the X1/CLK pin as shown in the timing diagram, not to guarantee operation of the part. If setup time is violated, DTACKN may be asserted as shown, or may be asserted 1 clock cycle later.
8. Operation to 0MHz is assured by design. Minimum test frequency is 2.0MHz.

Each receiver is quadruply buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the buffer of the receiving device is full.

Also provided on the SCN68681 are a multipurpose 6-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

BLOCK DIAGRAM

The SCN68681 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the Block Diagram.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The DTACKN output is asserted during write and read cycles to indicate to the CPU that data has been latched on a write cycle, or that valid data is present on the bus on a read cycle.

Interrupt Control

A single active-Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR), the Auditary Control Register(ACR) and the Interrupt Vector Register (IVR). The IMR may be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. When IACKN is asserted, and the DUART has an interrupt pending, the DUART responds by placing the contents of the IVR regsiter on the data bus and asserting DTACKN.

Outputs OP3-OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART. If an external is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 7.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4k baud. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

The Counter/Timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

Communications Channels A and B

Each communications channel of the SCN68681 comprises a full-duplex asynchronous receiver/transmitter (DUART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

The input port pulse detection circuitry uses a 38.4kHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25µs (assuming that the clock input is 3.6864MHz). The detection circuitry, in order to guarantee a true change in level has occurred, requires that two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs coincident with the first sample pulse. The 50µs time refers to the situation in which the change of state is just missed and the first change of state is not detected until 25µs later.

Input Port

The inputs to this unlatched 6-bit port can be read by the CPU by performing a read operation at address H'D'. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always read as a logic 1 and D6 will reflect the level of IACKN. The pins of this port can also serve as auxiliary inputs to certain portions fo the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs, lasting longer than 25 - 50µs, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU.

Output Port

The 8-bit multipurpose output port can be used as a general purpose output port, in which case the outputs are the complements of the Output Port Register (OPR). OPR[n] = 1 results in OP[n] = Low and vice versa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operation at address H'E' with the accompanying data specifying the bits to be reset (1 = set, 0 = no change). Likewise, a bit is reset by a write at address H'F' with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Outputs can be also individually assigned specific functions by appropriate programming of the Channel A mode registers (MR1A, MR2A), the Channel B mode registers (MR1B, MR2B), and the Output Port Configuration Register (OPCR).

OPERATION

Transmitter

The SCN68681 is conditioned to transmit data when the transmitter is enabled through the command register. The SCN68681

indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When a character is loaded into the Transmit Holding Register (THR), the above conditions are negated. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again which means one full character time of buffering is provided. Characters cannot be loaded into the THR while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains High and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the THR. If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous Low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS operation is enable, the CTSN input must be Low in order for the character to be transmitted. If it goes High in the middle of a transmission, the character in the shift register is transmitted and TxDA then remains in the marking state until CTSN goes Low. The transmitter can also control the deactivation of the RTSN output. If programmed, the RTSN output will be reset one bit time after the character in the transmit shift register and transmit holding register (if any) are completely transmitted, if the transmitter has been disabled.

Receiver

The SCN68681 is conditioned to receive data when enabled through the command register. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive Holding Register (RHR) and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than 8 bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1. The RxD input must return to a High condition for at least one-half bit time before a search for the next start bit begins.

The RHR consists of a First-In-First-Out (FIFO) stack with a capacity of three characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4]) will be set-upon receipt of the start bit of the new (overrunning) character).

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

Multidrop Mode

The DUART is equipped with a wake up mode for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wakeup' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed

number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the THR.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RHR FIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems.

For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to MR1x by RESET or by issuing a 'reset pointer' command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1x, switches the pointer to MR2x. The pointer then remains at MR2x, so that subsequent accesses are always to MR2x unless the pointer is reset to MR1x as described above.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'OA' should never be read during normal operation since they are reserved for internal diagnostics.

Table 1. SCN68681 Register Addressing

A4	A3	A2	A1	READ (R/WN = 1)	WRITE (R/WN = 0)
0	0	0	0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	BRG Test	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RHRA)	Tx Holding Register A (THRA)
0	1	0	0	Input Port Change Register (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Register (CRUR)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Register (CTLR)
1	0	0	0	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	1X/16X Test	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RHRB)	Tx Holding Register B (THRB)
1	1	0	0	Interrupt Vector Register (IVR)	Interrupt Vector Register (IVR)
1	1	0	1	Input Port	Output Port Conf. Register (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command
1	1	1	1	Stop Counter Command	Reset Output Port Bits Command

MR1A – Channel A Mode Register 1

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRA. After reading or writing MR1A, the pointer will point to MR2A.

MR1A[7] – Channel A Receiver Request-to-Send Control

This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR1A[7] = 1 causes RTSAN to be negated upon receipt of a valid start bit if the Channel A FIFO is full. However, OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

MR1A[6] – Channel A Receiver Interrupt Select

This bit selects either the Channel A receiver ready status (RxRDY) or the Channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to be output on OP4 if it is programmed as an interrupt output via the OPCR.

MR1A[5] – Channel A Error Mode Select

This bit select the operating mode of the three FIFOed status bits (FE, PE, received break) for Channel A. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block" mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

MR1A[4:3| – Channel A Parity Mode Select

If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data MR1A[4:3] = 11 selects Channel A to operate in the special multidrop mode described in the Operation section.

MR1A[2] – Channel A Parity Type Select

This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity'

mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

MR1A[1:0] – Channel A Bits Per Character Select
This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2A – Channel A Mode Register 2

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

MR2A[7:6] – Channel A Mode Select
Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The Channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop has been re-transmitted.

MR2A[5] – Channel A Transmitter Request-to-Send Control
This bit controls the deactivation of the RTSAN output (OP0) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR2A[5] = 1 caused OPR[0] to be reset automatically one bit time after the characters in the Channel A transmit shift register and in the THR, if any, are completely transmitted including the programmed number of stop bits, if the transmitter is not enabled. This feature can be used to automatically terminate the transmission of a message as follows:

1. Program auto-reset mode: MR2A[5] = 1.
2. Enable transmitter.
3. Asset RTSAN: OPR[0] = 1.
4. Send message.
5. Verify the message is sent by waiting until the transmit ready status (TxRDY) is asserted. Disable transmitter after the last character is loaded into the Channel A THR.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

NOTE: When TxEMT and TxRDY bits are at one just before a write to the Transmit Holding register, a command to disable the transmitter should be delayed until the TxRDY is at one again. TxRDY will set to one and the end of the start bit time.

MR2A[4] – Channel A Clear-to-Send Control
If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IP0) each time it is ready to send a character. If IP0 is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character.

MR2A[3:0] – Channel A Stop Bit Length Select
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1-9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1-1/16 to 2 stop bits can be programmed in increments of 1/16 bit. The receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit is enabled), in all cases.

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

MR1B – Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to MR1A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

MR2B – Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode register are identical to the bit definitions for MR2A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

Table 2. Register Bit Formats

	BIT 7	BIT 6	BIT 5	BIT 4 BIT 3	BIT 2	BIT 1 BIT 0
	RxRTS CONTROL	RxINT SELECT	ERROR MODE	PARITY MODE	PARITY TYPE	BITS PER CHARACTER
MR1A MR1B	0 = No 1 = Yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multidrop Mode	0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8

	BIT 7 BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	CHANNEL MODE	TxRTS CONTROL	CTS ENABLE Tx	STOP BIT LENGTH*			
MR2A MR2B	00 = Normal 01 = Auto-Echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

NOTE:
*Add 0.5 to values shown for 0 - 7 if channel is programmed for 5 bits/char.

	BIT 7 BIT 6 BIT 5 BIT 4	BIT 3 BIT 2 BIT 1 BIT 0
	RECEIVER CLOCK SELECT	TRANSMITTER CLOCK SELECT
CSRA CSRB	See Text	See Text

	BIT 7 BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MISCELLANEOUS COMMANDS	DISABLE Tx	ENABLE Tx	DISABLE Rx	ENABLE Rx
CRA CRB	See Text	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
Access to the uper four bits of the command register should be separated by three (3) edges of the X1 clock.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RECEIVED BREAK*	FRAMING ERROR*	PARITY ERROR*	OVERRUN ERROR	TxEMT	TxRDY	FFULL	RxRDY
SRA SRB	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
* These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a "reset error status" command. In character mode they are discarded when the corresponding data character is read from the FIFO.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3 BIT 2	BIT 1 BIT 0
	OP7	OP6	OP5	OP4	OP3	OP2
OPCR	0 = OPR[7] 1 = TxRDYB	0 = OPR[6] 1 = TxRDYA	0 = OPR[5] 1 = RxRDY/ FFULLB	0 = OPR[4] 1 = RxRDY/ FFULLA	00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB(1x) 11 = RxCB(1x)	00 = OPR[2] 01 = TxCA(16x) 10 = TxCA(1x) 11 = RxCA(1x)

	BIT 7	BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	BRG SET SELECT	COUNTER/TIMER MODE AND SOURCE	DELTA IP3 INT	DELTA IP2 INT	DELTA IP1 INT	DELTA IP0 INT
ACR	0 = set 1 1 = set 2	See Table 4	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

Table 2. Register Bit Formats (Continued)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	DELTA IP3	DELTA IP2	DELTA IP1	DELTA IP0	IP3	IP2	IP1	IP0
IPCR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	INPUT PORT CHANGE	DELTA BREAK B	RxRDY/ FFULLB	TxRDYB	COUNTER READY	DELTA BREAK A	RxRDY/ FFULLA	TxRDYA
ISR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IN. PORT CHANGE INT	DELTA BREAK B INT	RxRDY/ FFULLB INT	TxRDYB INT	COUNTER READY INT	DELTA BREAK A INT	RxRDY/ FFULLA INT	TxRDYA INT
IMR	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]
CTUR								

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]
CTLR								

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IVR[7]	IVR[6]	IVR[5]	IVR[4]	IVR[3]	IVR[2]	IVR[1]	IVR[0]
IVR								

CSRA – Channel A Clock Select Register

CSRA[7:4] – Channel A Receiver Clock Select
This field selects the baud rate clock for the Channel A receiver. The field definition is shown in Table 3.

CSRA[3:0] – Channel A Transmitter Clock Select
This field selects the baud rate clock for the Channel A transmitter. The field definition is as shown in Table 3, except as follows:

CSRA[3:0]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP3-16X	IP3-16X
1111	IP3-1X	IP3-1X

The transmitter clock is always a 16X clock except for CSR[3:0] = 1111.

Table 3. Baud Rate Clock = 3.6864 MHz

CSRA[7:4]	ACR[7] = 0	Baud Rate ACR[7] = 1
0000	50	75
0001	110	110
0010	134.5	134.5
0011	200	150
0100	300	300
0101	600	600
0110	1,200	1,200
0111	1,050	2,000
1000	2,400	2,400
1001	4,800	4,800
1010	7,200	1,800
1011	9,600	9,600
1100	38.4k	19.2k
1101	Timer	Timer
1110	IP4-16X	IP4-16X
1111	IP4-1X	IP4-1X

NOTE: The receiver clock is always a 16X clock except for CSRA[7:4] = 1111.

CSRB – Channel B Clock Select Register

CSRB[7:4] – Channel B Receiver Clock Select
This field selects the baud rate clock for the Channel B receiver. The field definition is as shown in Table 3, except as follows:

CSRB[7:4]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP2-16X	IP2-16X
1111	IP2-1X	IP2-1X

The receiver clock is always a 16X clock except for CSRB[7:4] = 1111.

CSRB[3:0] – Channel B Transmitter Clock Select
This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 3, except as follows:

CSRB[3:0]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP5-16X	IP5-16X
1111	IP5-1X	IP5-1X

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

CRA – Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

CRA[6:4] – Miscellaneous Commands
The encoded value of this field may be used to specify a single command as follows:

CRA[6:4] COMMAND
NOTE: Access to the uper four bits of the command register should be separated by three (3) edges of the X1 clock.

000 No command.
001 Reset MR pointer. Causes the Channel A MR pointer to point to MR1.
010 Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.
011 Reset transmitter. Resets the Channel A transmitter as if a hardware reset had been applied.
100 Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.
101 Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.
110 Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.
111 Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted.

CRA[3] – Disable Channel A Transmitter
This command terminates transmitter operation and reset the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CRA[2] – Enable Channel A Transmitter
Enables operation of the Channel A transmitter. The TxRDY status bit will be asserted.

CRA[1] – Disable Channel A Receiver
This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

CRA[0] – Enable Channel A Receiver
Enables operation of the Channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start-bit state.

CRB – Channel B Command Register

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.,

SRA – Channel A Status Register

SRA[7] – Channel A Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received further entries to the FIFO are inhibited until the RxDA line to the marking state for at least one-half a bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the Channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

SRA[6] – Channel A Framing Error
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SRA[5] – Channel A Parity Error
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

In the special multidrop mode the parity error bit stores the receive A/D bit.

SRA[4] – Channel A Overrun Error
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost.

This bit is cleared by a 'reset error status' command.

SRA[3] – Channel A Transmitter Empty (TxEMTA)
This bit will be set when the Channel A transmitter underruns; i.e., both the Transmit Holding Register (THR) and the transmit shift register are empty. It is set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU or when the transmitter is disabled.

SRA[2] – Channel A Transmitter Ready (TxRDYA)
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, viz., characters loaded into the THR while the transmitter is disabled will not be transmitted.

SRA[1] – Channel A FIFO Full (FFULLA)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

SRA[0] – Channel A Receiver Ready (RxRDYA)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift to the FIFO and reset when the CPU reads the RHR, if after this read there are not more characters still in the FIFO.

SRB – Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

OPCR – Output Port Configuration Register

OPCR[7] – OP7 Output Select
This bit programs the OP7 output to provide one of the following:
0: The complement of OPR[7].
1: The Channel B transmitter interrupt output which is the complement of TxRDYB. When in this mode OP7 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[6] – OP6 Output Select
This bit programs the OP6 output to provide one of the following:
0: The complement of OPR[6].
1: The Channel A transmitter interrupt output which is the complement of TxRDYA. When in this mode OP6 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[5] – OP5 Output Select
This bit programs the OP5 output to provide one of the following:
0: The complement of OPR[5].
1: The Channel B transmitter interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[4] – OP4 Output Select
This field programs the OP4 output to provide one of the following:
0: The complement of OPR[4].
1: The Channel A receiver interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[3:2] – OP3 Output Select
This bit programs the OP3 output to provide one of the following:
00: The complement of OPR[3].
01: The counter/timer output, in which case OP3 acts as an open-drain output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
10: The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
11: The 1X clock for the Channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

OPCR[1:0] – OP2 Output Select
This field programs the OP2 output to provide one of the following:
00: The complement of OPR[2].
01: The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
10: The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
11: The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects one of two sets of baud rates to be generated by the BRG:

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.

Set 2: 75, 110, 134.5, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, and 19.2k baud.

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table 4.

Table 4. Bit Rate Generator Characteristics Crystal or Clock = 3.6864MHz

NORMAL RATE (BAUD)	ACTUAL 16x CLOCK (kHz)	ERROR (%)
50	0.8	0
75	1.2	0
110	1.759	-0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	-0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2k	307.2	0
38.4k	614.4	0

NOTE:
Duty cycle of 16x clock is 50% ± 1%.

ACR[6:4] – Counter/Timer Mode And Clock Source Select
This field selects the operating mode of the counter/timer and its clock source as shown in Table 5.

Table 5. ACR 6:4 Field Definition

ACR [6:4]	MODE	CLOCK SOURCE
000	Counter	External (IP2)*
001	Counter	TxCA – 1x clock of Channel A transmitter
010	Counter	TxCB – 1x clock of Channel B transmitter
011	Counter	Crystal or external clock (x1/CLK) divided by 16
100	Timer	External (IP2)*
101	Timer	External (IP2) divided by 16*
110	Timer	Crystal or external clock (X1/CLK)
111	Timer	Crystal or external clock (X1/CLK) divided by 16

NOTE:
* In these modes, the Channel B receiver clock should normally be generated from the baud rate generator.

ACR[3:0] – IP3, IP2, IP1, IP0
Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7] – IP3, IP2, IP1, IP0
Change-of-State
These bits are set when a change-of-state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – IP3, IP2, IP1, IP0
Current State
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR – the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to 00_{16} when the DUART is reset.

ISR[7] – Input Port Change Status
This bit is a '1' when a change-of-state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

ISR[6] – Channel B Change In Break
This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel B 'reset break change interrupt' command.

ISR[5] – Channel B Receiver Ready or FIFO Full
The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that a character has been received in Channel B and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel B FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

ISR[4] – Channel B Transmitter Ready
This bit is a duplicate of TxRDYB (SRB[2]).

ISR[3] – Counter Ready.
In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

ISR[2] – Channel A Change In Break
This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

ISR[1] – Channel A Receiver Ready Or FIFO Full
The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that a character has been received in Channel A and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU read the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel A FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the ISR[0] and IMR waiting character is loaded into the FIFO.

ISR[0] – Channel A Transmitter Ready
This bit is a duplicate of TxRDYA (SRA[2]).

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3-OP7 or the reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is 0002_{16}. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR and CTLR is changed, the current half-period will not be affected, but subsequent half periods will be. In this mode the C/T runs continuously. Receipt of a start counter command (read with A4-A1) = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR. The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A4-A1 = 1111). The command, however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

On power-up and after reset, the counter/timer runs in timer mode and can only be restarted. Because it cannot be shut off or stopped, and runs continuously in timer

mode, it is recommended that at initialization, the output port, OP3, should be masked off through the OPCR[3:2} = 00 until the C/T is programmed to the desired operational state.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching terminal count 0000_{16}, the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter commands. If new values have not been loaded, the previous count values are preserved and used for the next count cycle

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

IVR – Interrupt Vector Register

This register contains the interrupt vector. The register is initialized to H'0F' by RESET. The contents of the register are placed on the data bus when the DUART responds to a valid interrupt acknowledge cycle.

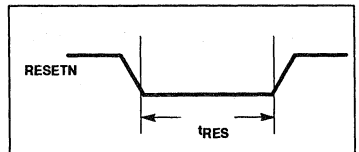


Figure 1. Reset Timing

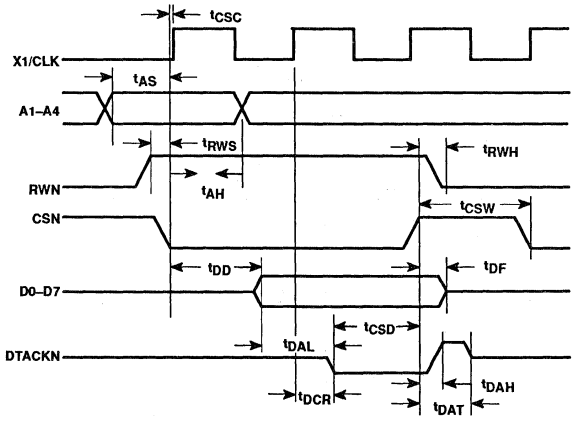


Figure 2. Bus Timing (Read Cycle)

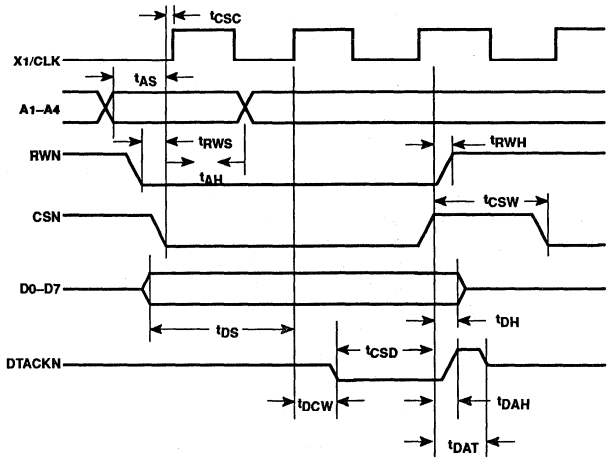


Figure 3. Bus Timing (Write Cycle)

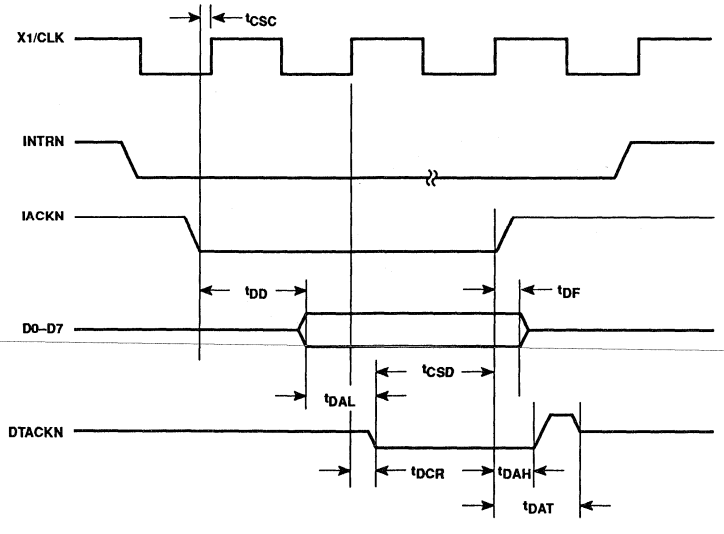


Figure 4. Interrupt Cycle Timing

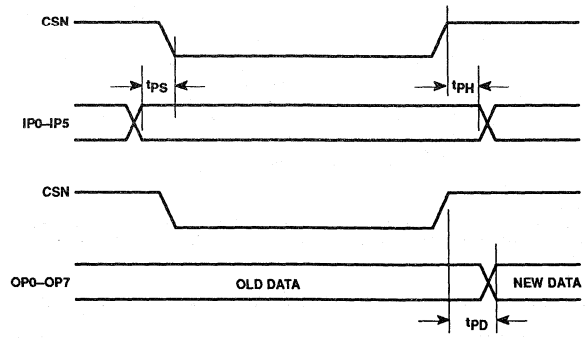


Figure 5. Port Timing

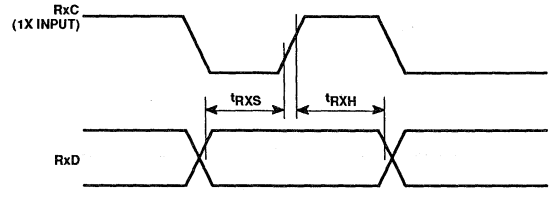


Figure 6. Receive Timing

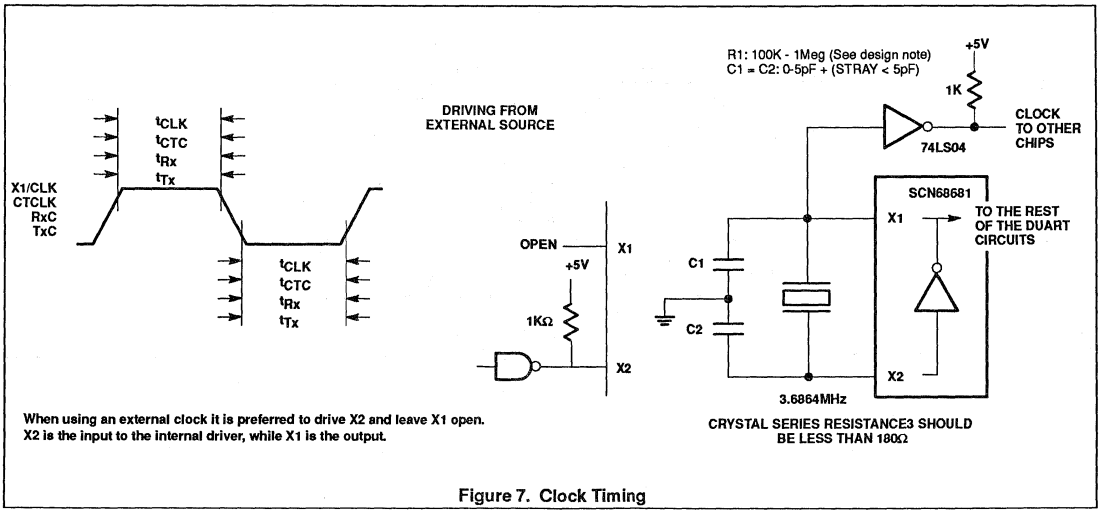
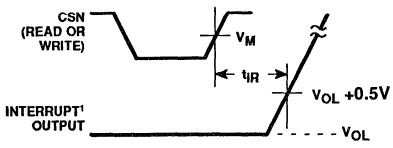


Figure 7. Clock Timing



NOTES:

1. INTRN or OP3 – OP7 when used as interrupt outputs.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from themidpoint of the switching signal, V_M, to a point 0.5 volts above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 8. Interrupt Timing

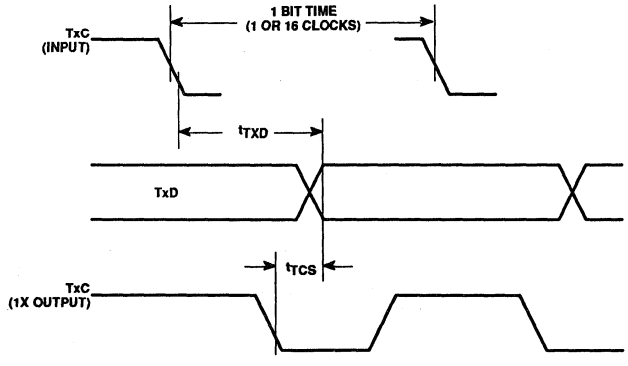


Figure 9. Transmit Timing

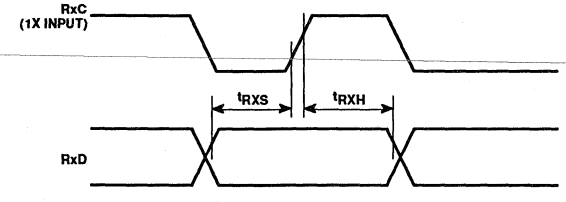
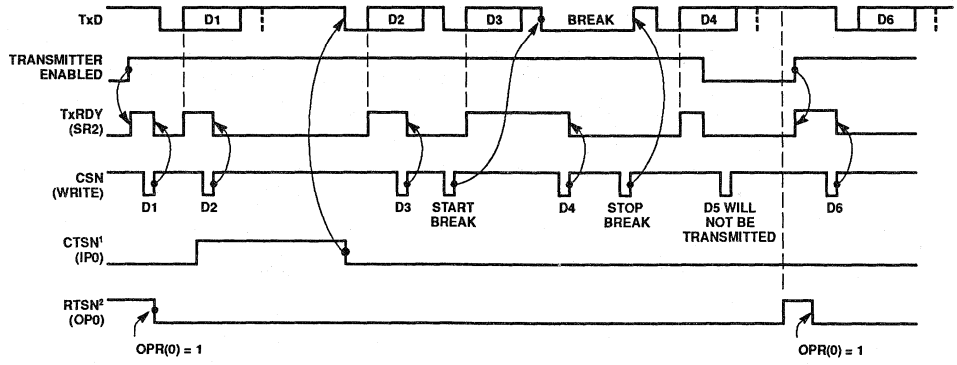
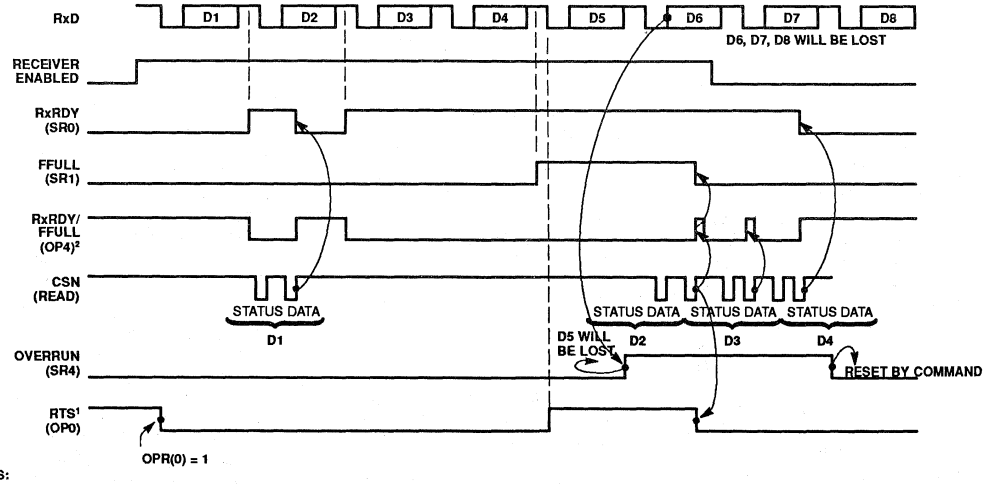


Figure 10. Receive Timing



NOTES:
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

Figure 11. Transmitter Timing



NOTES:
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) and MR1(6) = 0.

Figure 12. Receiver Timing

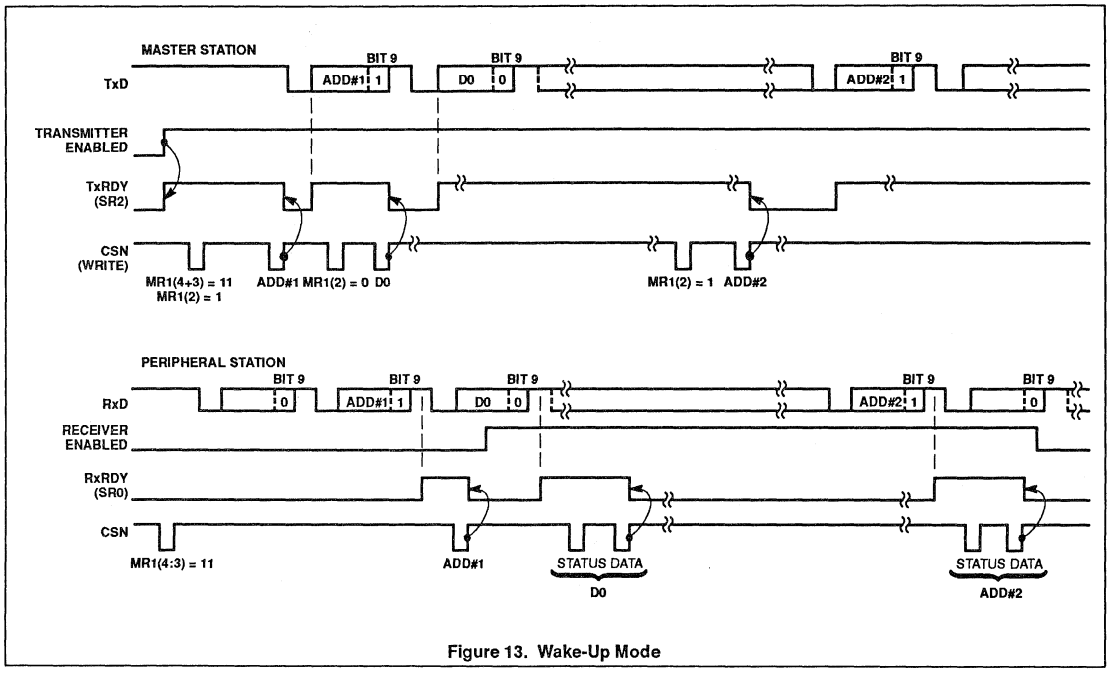


Figure 13. Wake-Up Mode

Output Port Notes

The output ports are controlled from three places: the OPCR register, the OPR register, and the MR registers. The OPCR register controls the source of the data for the output ports OP2 through OP7. The data source for output ports OP0 and OP1 is controlled by the MR and CR registers. When the OPR is the source of the data for the output ports, the data at the ports is inverted from that in the OPR register. The content of the OPR register is controlled by the "Set Output Port Bits Command". These commands are at E and F, respectively. When these commands are used, action takes place only at the bit locations where ones exist. For example, a one in bit location 5 of the data word used with the "Set Output Port Bits" command will result in OPR5 being set to one. The OP5 would then be set to zero (V_{SS}). Similarly, a one in bit position 5 of the data word associated with the "Reset Output Ports Bits" command would set OPR5 to zero, and hence, the pin OP5 to a one (V_{DD}).

The CTS, RTS, CTS Enable Tx signals

CTS (Clear To Send) is usually meant to be a signal to the transmitter meaning that it may transmit data to the receiver. The CTS input is on pin MPI. The CTS signal is active low; thus, it is called CTS.

RTS is usually meant to be a signal from the receiver indicating that the receiver is ready to receive data. It is also active low and is, thus, called RTSN. RTSN is on pin MP0. A receiver's RTS output will usually be connected to the CTS input of the associated transmitter. Therefore, one could say that RTS and CTS are different ends of the same wire!

MR2(4) is the bit that allows the transmitter to be controlled by the CTS pin (MPI). When this bit is set to one AND the CTS input is driven high, the transmitter will stop sending data at the end of the present character being serialized. It is usually the RTS output of the receiver that will be connected to the transmitter's CTS input. The receiver will set RTS high when the receiver FIFO is full AND the start bit of the fourth character is sensed. Transmission then stops with four valid characters in the receiver. When MR2(4) is set to one, CTSN must be at zero for the transmitter to operate. If MR2(4) is set to zero, the MP pin will have no effect on the operation of the transmitter.

MR1(7) is the bit that allows the receiver to control MP0. When MP0 is controlled by the receiver, the meaning of that pin will be RTS. However, a point of confusion arises in that MP0 may also be controlled by the transmitter. When the transmitter is controlling this pin, its meaning is not RTS at all. It is, rather, that the transmitter has finished sending its last data byte. Programming the MP0 pin to be controlled by the receiver and the transmitter at the same time is allowed, but would usually be incompatible.

RTS is expressed at the MP0 pin which is still an output port. Therefore, the state of MP0 should be set low for the receiver to generate the proper RTS signal. The logic at the output is basically a NAND of the MP0 bit register and the RTS signal as generated by the receiver. When the RTS flow control is selected via the MR(7) bit the state of the MP0 register is not changed. Terminating the use of "Flow Control" (via the MR registers) will return the MP0 pin to the control of the MP0 register.

Transmitter Disable Note

The sequence of instructions enable transmitter — load transmit holding register — disable transmitter will result in nothing being sent if the time between the end of loading the transmit holding register and the disable command is less that 3/16 bit time in the 16x mode or one bit time in the 1x mode. Also, if the transmitter, while in the enabled state and underrun condition, is immediately disabled after a single character is loaded to

the transmit holding register, that character will not be sent.

In general, when it is desired to disable the transmitter before the last character is sent AND the TxEMT bit is set in the status register (TxEMT is always set if the transmitter has underrun or has just been enabled), be sure the TxRDY bit is active immediately before issuing the transmitter disable instruction. TxRDY sets at the end of the "start bit" time. It is during the start bit that the data in the transmit holding register is transferred to the transmit shift register.

Non-standard baud rates are available as shown in Table 6 below, via the BRG Test function.

Table 6. Baud Rate

	Normal BRG		BRG Test	
CSR[7:4]	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0000	50	75	4,800	7,200
0001	110	110	880	880
0010	134.5	38.4K	1,076	38.4K
0011	200	150	19.2K	14.4K
0100	300	300	28.8K	28.8K
0101	600	600	57.6K	57.6K
0110	1,200	1,200	115.2K	115.2K
0111	1,050	2,000	1,050	2,000
1000	2,400	2,400	57.6K	57.6K
1001	4,800	4,800	4,800	4,800
1010	7,200	1,800	57.6K	14.4K
1011	9,600	9,600	9,600	9,600
1100	38.4K	19.2K	38.4K	19.2K
1101	Timer	Timer	Timer	Timer
1110	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X
1111	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X

NOTE:
Each read on address H'2' will toggle the baud rate test mode. When in the BRG test mode, the baud rates change as shown to the left. This change affects all receivers and transmitters on the DUART. Also, the RTSN outputs (OP[0] and OP[1]) become the transmitter 1x clock.

The test mode at address H'A' changes all transmitters and receivers to the 1x mode and connects the output ports to some internal nodes.

Universal asynchronous receiver/transmitter (UART) SCC2691

DESCRIPTION

The Signetics SCC2691 Universal Asynchronous Receiver/Transmitter (UART) is a single-chip CMOS-LSI communications device that provides a full-duplex asynchronous receiver/transmitter. It is fabricated with Signetics CMOS technology which combines the benefits of high density and low power consumption.

The operating speed of the receiver and transmitter can be selected independently as one of 18 fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the UART particularly attractive for dual-speed channel applications such as clustered terminal systems.

The receiver is quadruple buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a handshaking capability is provided to disable a remote UART transmitter when the receiver buffer is full.

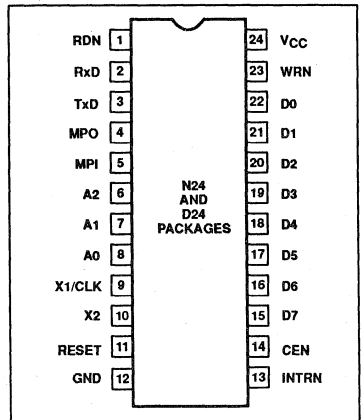
The UART provides a power-down mode in which the oscillator is frozen but the register contents are stored. This results in reduced power consumption on the order of several magnitudes.

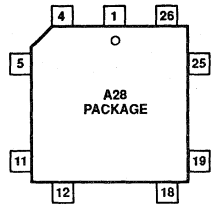
The UART is fully TTL compatible and operates from a single +5V power supply.

FEATURES

- Full-duplex asynchronous receiver/transmitter
- Quadruple buffered receiver data register
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Baud rate for the receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4K baud
  - Non-standard rates to 115.2kb
  - One user-defined rate derived from programmable timer/ counter
  - External 1X or 16X clock
- Parity, framing, and overrun detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote Loopback
- Multi-function programmable 16-bit counter/timer
- Single interrupt output with seven maskable interrupting conditions
- On-chip crystal oscillator
- Low power mode
- TTL compatible
- Single +5V power supply
- Commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature versions available
- SOL, PLCC and 300 mil wide DIP packages available

PIN CONFIGURATIONS



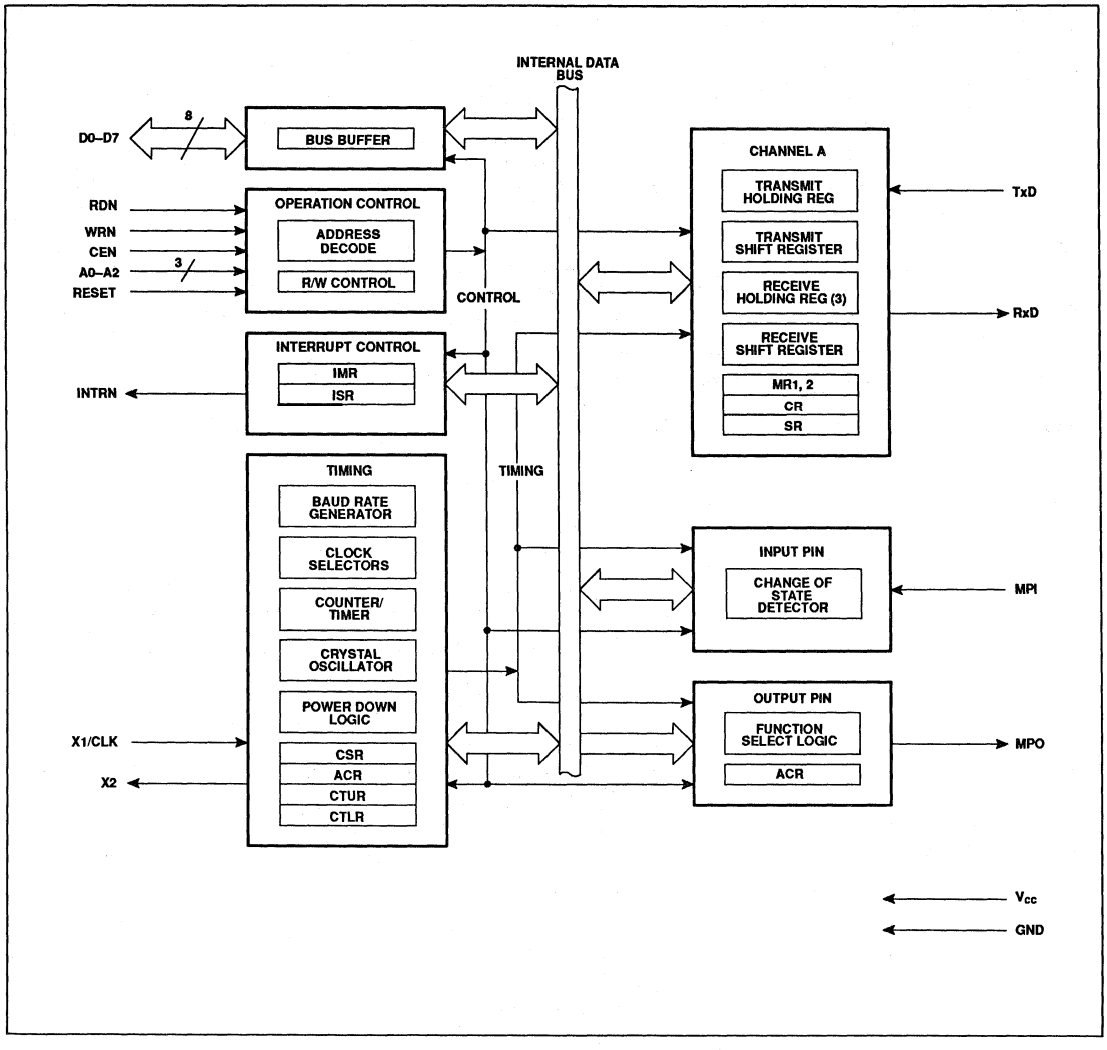


Pin	Symbol	Pin	Symbol
1	V_{CC}	15	GND
2	RDN	16	INTRN
3	RxD	17	CEN
4	TxD	18	D7
5	MPO	19	D6
6	MPI	20	D5
7	NC	21	D4
8	NC	22	D3
9	A2	23	NC
10	A1	24	D2
11	A0	25	D1
12	X1/CLK	26	NC
13	X2	27	D0
14	RESET	28	WRN

ORDERING INFORMATION

PACKAGES	V_{CC} = +5V ±10%, T_A = 0°C to +70°C	V_{CC} = +5V ±10%, T_A = –40°C to +85°C
Plastic DIP	SCC2691AC1N24	SCC2691AE1N24
Plastic LCC	SCC2691AC1A28	SCC2691AE1A28
Plastic SOL	SCC2691AC1D24	

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
D0–D7	22–15	27, 25, 24, 22–18	I	**Data Bus:** Active-high 8-bit bidirectional 3-State data bus. Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the UART take place over this bus. The direction of the transfer is controlled by the WRN and RDN inputs when the CEN input is low. When the CEN input is high, the data bus is in the 3-State condition.
CEN	14	17	I	**Chip Enable:** Active-low input. When low, data transfers between the CPU and the UART are enabled on D0–D7 as controlled by the WRN, RDN and A0–A2 inputs. When CEN is high, the UART is effectively isolated from the data bus and D0–D7 are placed in the 3-State condition.
WRN	23	28	I	**Write Strobe:** Active-low input. A low on this pin while CEN is low causes the contents of the data bus to be transferred to the register selected by A0–A2. The transfer occurs on the trailing (rising) edge of the signal.
RDN	1	2	I	**Read Strobe:** Active-low input. A low on this pin while CEN is low causes the contents of the register selected by A0–A2 to be placed on the data bus. The read cycle begins on the leading (falling) edge of RDN.
A0–A2	8–6	11–9	I	**Address Inputs:** Active-high address inputs to select the UART registers for read/write operations.
RESET	11	14	I	**Reset:** Master reset. A high on this pin clears the status register (SR), the interrupt mask register (IMR), and the interrupt status register (ISR), sets the mode register pointer to MR1, and places the receiver and transmitter in the inactive state causing the TxD output to go to the marking (high) state. Clears Test modes.
INTRN	13	16	O	**Interrupt Request:** This active-low output is asserted upon occurrence of one or more of seven maskable interrupting conditions. The CPU can read the interrupt status register to determine the interrupting condition(s). This open-drain output requires a pull-up resistor.
X1/CLK	9	12	I	**Crystal 1:** Crystal or external clock input. When using the crystal oscillator, this pin serves as the connection for one side of the crystal. If a crystal is not used, an external clock is supplied at this input. An external clock (or crystal) is required even if the internal baud rate generator is not utilized. This clock is used to drive the internal baud rate generator, as an optional input to the timer/counter, and to provide other clocking signals required by the chip.
X2	10	13	I	**Crystal 2:** Connection for other side of crystal. If an external source is used instead of a crystal, this connection should be open.
RxD	2	3	I	**Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified, this input is sampled on the rising edge of the clock.
TxD	3	4	O	**Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the marking (high) condition when the transmitter is idle or disabled and when the UART is operating in local loopback mode. If external transmitter is specified, the data is shifted on the falling edge of the transmitter clock.
MPO	4	5	O	**Multi-Purpose Output:** One of the following functions can be selected for this output pin by programming the auxiliary control register: **RTSN** – Request to send active-low output. This output is asserted and negated via the command register. By appropriate programming of the mode registers, RTSN can be programmed to be automatically reset after the character in the transmitter is completely shifted or when the receiver FIFO and shift register are full. **C/TO** – The counter/timer output. **TxC1X** – The 1X clock for the transmitter. **TxC16X** – The 16X clock for the transmitter. **RxC1X** – The 1X clock for the receiver. **RxC16X** – The 16X clock for the receiver. **TxRDY** – The transmitter holding register empty signal. Active-low output. **RxRDY/FFULL** – The receiver FIFO not empty/full signal. Active-low output.
MPI	5	6	I	**Multi-Purpose Input:** This pin can serve as an input for one of the following functions: **GPI** – General purpose input. The current state of the pin can be determined by reading the ISR. **CTSN** – Clear-to-send active-low input. **CTCLK** – Counter/timer external clock input. **RTCLK** – Receiver and/or transmitter external clock input. This may be a 1X or 16X clock as programmed by CSR[3:0] or CSR[7:4].
V_{CC}	24	1	I	**Power Supply:** +5V supply input.
GND	12	15	I	**Ground**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	Note 4	°C
T_{STG}	Storage temperature range	–65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	–0.5 to + 7.0	V
V_S	Voltage from any pin to ground[3]	–0.5 to V_{CC} ±10%	V
P_D	Power Dissipation	300	mW

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperature, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range. See Ordering Information table for applicable operating temperature and V_{CC} supply range.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage					
	All except X1/CLK		2			V
	X1/CLK		$0.8V_{CC}$		V_{CC}	V
V_{OL}	Output low voltage	I_{OL} = 2.4mA			0.4	V
V_{OH}[4]	Output high voltage (except open drain outputs)	I_{OH} = –400µA	2.4			V
I_{IL}	Input leakage current	V_{IN} = 0 to V_{CC}	–10		10	µA
I_{LL}	Data bus 3-State leakage current	V_O = 0.4 to V_{CC}	–10		10	µA
I_{OD}	Open-drain output leakage curent	V_O = 0.4 to V_{CC}	–10		10	µA
I_{XIL}	X1/CLK low input current	V_{IN} = 0, X2 floated	–100	–30	0	µA
I_{XIH}	X1/CLK high input current	V_{IN} = V_{CC}, X2 floated	0	30	100	µA
I_{X2L}	X2 low output current	V_{OUT} = 0, X1/CLK = V_{CC}	–100			µA
I_{X2H}	X2 high output current	V_{OUT} = V_{CC}, X1/CLK = 0V			100	µA
I_{CCA}	Power supply current, active					
	0°C to +70°C			0.8	2.0	mA
	–40°C to +85°C			1.0	2.5	mA
I_{CCD}	Power down current[5]				500	µA

NOTES:
1. Parameters are valid over specified temperature range. See Ordering Information table for applicable operating temperature and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all input signals swing between 0V and 2.8V with a transition time of 20ns max. For X1/CLK, this swing is between 0.4V and 4.0V. All time measurements are referenced at input voltages of 0.8V and 2V and output voltages of 0.8V and 2V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test condition for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
5. For power down current levels in the 1µA region see the UART application note.

AC ELECTRICAL CHARACTERISTICS[1, 2, 3, 4]

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Reset timing (Figure 1)					
t_{RES}	Reset pulse width	100			ns
Bus timing (Figure 2)[5]					
t_{AS}	A0–A2 setup time to RDN, WRN low	10			ns
t_{AH}	A0–A2 hold time from RDN, WRN low	100			ns
t_{CS}	CEN setup time to RDN, WRN low	0			ns
t_{CH}	CEN hold time from RDN, WRN high	0			ns
t_{RW}	WRN, RDN pulse width	150			ns
t_{DD}	Data valid after RDN low			125	ns
t_{DF}	Data bus floating after RDN high			110	ns
t_{DS}	Data setup time before WRN high	50			ns
t_{DH}	Data hold time after WRN high	30			ns
t_{RWD}	Time between reads and/or writes[6, 7]	150			ns
MPI and MPO timing (Figure 3)[5]					
t_{PS}	MPI input setup time before RDN low	30			ns
t_{PH}	MI input hold time after RDN low	30			ns
t_{PD}	MPO output valid after WRN high			370	ns
Interrupt timing (Figure 4)					
t_{IR}	INTRN negated				
	Read RHR (RxRDY/FFULL interrupt)			370	ns
	Write THR (TxRDY, TxEMT interrupt)			370	ns
	Reset command (break change interrupt)			370	ns
	Reset command (MPI change interrupt)			370	ns
	Stop C/T command (counter interrupt)			370	ns
	Write IMR (clear of interrupt mask bit)			270	ns
Clock timing (Figure 5)					
t_{CLK}	X1/CLK high or low time	100			ns
f_{CLK}	X1/CLK frequency[9]	0	3.6864	4.0	MHz
t_{CTC}	Counter/timer clock high or low time	100			ns
f_{CTC}	Counter/timer clock frequency	0[8]		4.0M	Hz
t_{RX}	RxC high or low time	220			ns
f_{RX}	RxC frequency (16X)	0[8]		2.0M	Hz
	RxC frequency (1X)	0[8]		1.0M	Hz
t_{TX}	TxC high or low time	220			ns
f_{TX}	TxC frequency (16X)	0[8]		2.0M	Hz
	TxC frequency (1X)	0[8]		1.0M	Hz
Transmitter timing (Figure 6)					
t_{TXD}	TxD output delay from TxC low			350	ns
t_{TCS}	TxC output delay from TxD output data	0		150	ns
Receiver timing (Figure 7)					
t_{RXS}	RxD data setup time to RxC high	100			ns
t_{RXH}	RxD data hold time from RxC high	100			ns

NOTES:

1. Parameters are valid over specified temp. range. See Ordering Information table for applicable operating temp. and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all input signals swing between 0V and 2.8V with a transition time of 20ns max. For X1/CLK, this swing is between 0.4V and 4.0V. All time measurements are referenced at input voltages of 0.8V and 2V and output voltages of 0.8V and 2V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test condition for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
5. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. In this case, all timing specifications apply referenced to the falling and rising edges of CEN. CEN and RDN (also CEN and WRN) are ORed internally. As a consequence, this signal asserted last initiates the cycle and the signal negated first terminates the cycle.
6. If CEN is used as the 'strobing' input, this parameter defines the minimum high time between one CEN and the next. The RDN signal must be negated for t_{RWD} guarantee that any status register changes are valid.
7. Consecutive write operations to the command register require at least three rising edges of the X1 clock between writes.
8. These parameters are guaranteed by design, but are not 100% tested in production.
9. Operation to 0MHz is assured by design. Minimum test frequency is 2MHz.

BLOCK DIAGRAM

As shown in the block diagram, the UART consists of: data bus buffer, interrupt control, operation control, timing, receiver and transmitter.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data busses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and UART.

Interrupt Control

A single interrupt output (INTRN) is provided which may be asserted upon occurrence of any of the following internal events:

- Transmit holding register ready
- Transmit shift register empty
- Receive holding register ready or FIFO full
- Change in break received status
- Counter reached terminal count
- Change in MPI input
- Assertion of MPI input

Associated with the interrupt system are the interrupt mask register (IMR) and the interrupt status register (ISR). The IMR can be programmed to select only certain of the above conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. However, the bits of the ISR are not masked by the IMR.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The functions performed by the CPU read and write operations are shown in Table 1.

Mode registers 1 and 2 are accessed via an auxiliary pointer. The pointer is set to MR1 by RESET or by issuing a reset pointer command via the command register. Any read or write of the mode register while the pointer is at MR1 switches the pointer to MR2. the pointer then remains at MR2 so that subsequent accesses are to MR2, unless the pointer is reset to MR1 as described above.

Table 1. Register Addressing

A2	A1	A0	READ (RDN = 0)	WRITE (WRN = 0)
0	0	0	MR1, MR2	MR1, MR2
0	0	1	SR	CSR
0	1	0	BRG Test	CR
0	1	1	RHR	THR
1	0	0	1X/16X Test	ACR
1	0	1	ISR	IMR
1	1	0	CTU	CTUR
1	1	1	CTL	CTLR

NOTE;
*Reserved registers should never be read during operation since they are reserved for internal diagnostics.
ACR = Auxiliary control register
CR = Command register
CSR = Clock select register
CTL = Counter/timer lower
CTLR = Counter/timer lower register
CTU = Counter/timer upper
CTUR = Counter/timer upper register
MR = Mode register A
SR = Status register
THR = Tx holding register

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and two clock selectors.

The crystal oscillator operates directly from a 3.6864MHz crystal connected across the X1/CLK and X2 inputs with a minimum of external components. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. If an external clock is used instead of a crystal, X1/CLK is driven using a configuration similar to the one in Figure 5. In this case, the input high-voltage must be capable of attaining the voltage specified in the DC Electrical Characteristics. The clock serves as the basic timing reference for the baud rate generator (BRG), the counter/timer, and other internal circuits. A clock frequency, within the limits specified in the electrical specifications, must be supplied if the internal BRG is not used.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. Thirteen of these are available simultaneously for use by the receiver and transmitter. Eight are fixed, and one of two sets of five can be selected by programming ACR[7]. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The clock selectors allow the independent selection by the receiver and er of any of these baud rates or an external timing signal.

The C/T operation is programmed by ACR[6:4]. One of eight timing sources can be used as the input to the C/T. The output of the C/T is available to the clock selectors and can be programmed by ACR[2:0} to be output on the MPO pin.

In the timer mode, the C/T generates a square wave whose period is twice the number of clock periods loaded into the C/T upper and lower registers. The counter ready bit in the ISR is set once each cycle of the square wave. If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half-periods will be affected. In this mode the C/T runs continuously and does not recognize the stop counter command (the command only resets the counter ready bit in the ISR). Receipt of a start C/T command causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR. Counting begins upon receipt of a start C/T command. Upon reaching terminal count, the counter ready bit in the ISR is set. The counter continues counting past the terminal count until stopped by the CPU. If MPO is programmed to be the output of the C/T, the output remains high until terminal count is reached, at which time it goes low. The output returns to the high state and the counter ready bit is cleared when the counter is stopped by a stop counter command. the CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command following a stop counter command. If new values have not been loaded, the previous count values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower eight bits of the counter may be read by the CPU. It is recommended that

the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower eight bits to the upper eight bits occurs between the times that both halves of the counter are read. However, a subsequent start counter command causes the counter to begin a new count cycle using the values in CTUR and CTLR.

Receiver and Transmitter

The UART is a full-duplex asynchronous receiver/transmitter. The operating frequency for the receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input. Registers associated with the communications channel are: the mode registers (MR1 and MR2), the clock select register (CSR), the command register (CR), the status register (SR), the transmit holding register (THR), and the receive holding register (RHR).

Transmitter

The transmitter accepts parallel data from the CPU and converts it to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains high and the TxEMT bit in the SR will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character in the THR. In the 16X clock mode, this also resynchronizes the internal 1X transmitter clock so that transmission of the new character begins with minimum delay.

The transmitter can be forced to send a break (continuous low condition) by issuing a start break command via the CR. The break is terminated by a stop break command.

If the transmitter is disabled, it continues operating until the character currently being transmitted and the character in the THR, if any, are completely sent out. Characters cannot be loaded in the THR while the transmitter is disabled.

Receiver

The receiver accepts serial data on the RxD pin, converts the serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition, and presents the assembled character to the CPU. The receiver looks for a high-to-low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled again each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled high, the start bit is invalid and the search for a valid start bit begins again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and the parity bit (if any) have been assembled, and one sop bit has been detected. The data is then transferred to the RHR and the RxRDY bit in the SR is set to a 1. If the character length is less than eight bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (i.e. framing error) and RxD remains low for one-half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point(one-half bit time after the stop bit was sampled). The parity error, framing error and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set.

If a break condition is detected (RxD is low for the entire character including the stop bit), only one character consisting of all zeros will be loaded in the FIFO and the received break bit in the SR is set to 1. The RxD input must return to a high condition for two successive clock edges of the 1X clock (internal or external) before a search for the next start bit begins.

RECEIVER FIFO

The RHR consists of a first-in-first-out (FIFO) queue with a capacity of three characters. Data is loaded from the receive shift register into the top-most empty position of the FIFO. The RxRDY bit in the status register (SR) is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three queue positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are appended to each data character in the FIFO. Status can be provided in two ways, as programmed by the error mode control bit in mode register 1. In the character mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the block mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last reset error command was issued. In either mode, reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore, the SR should be read prior to reading the corresponding data character.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exists, the contents of the FIFO are not affected: the character previously in the shift register is lost and the overrun error status bit (SR[4]) will be set upon receipt of the start bit of the new (overrunning) character.

WAKE-UP MODE

In addition to the normal transmitter and receiver operation described above, the UART incorporates a special mode which provides automatic wake-up of the receiver through address frame recognition for multi-processor communications. This mode is selected by programming bits MR1[4:3] to '11'.

In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, whose receivers are normally disabled, examine the received data stream and 'wake-up' the CPU [by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, an address/data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1[2]. MR1[2] = 0 transmits a zero in the A/D bit position which identifies the corresponding data bits as data, while MR1[2] = 1 transmits a one in the A/D bit position which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits in the THR.

While in this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character in

the RHR FIFO if the received A/D bit is a one, but discards the received character if the received A/D bit is a zero. If enabled, all received characters are then transferred to the CPU via the RHR. In either case, the data bits are loaded in the data FIFO while the A/D bit is loaded in the status FIFO position normally used for parity error (SR[5]). Framing error, overrun error, and break detect operate normally whether or not the receiver is enabled.

MULTI-PURPOSE INPUT PIN

The MPI pin can be programmed as an input to one of several UART circuits. The function of the pin is selected by programming the appropriate control register (MR2[4]), ACR[6:4], CSR [7:4, 3:0]}. Only one of the functions may be selected at any given time. If CTS or GPI is selected, a change of state detector provided with the pin is activated. A high-to-low or low-to-high transition of the inputs lasting longer than 25–50µs sets the MPI change-of-state bit in the interrupt status register. The bit is cleared via a command. The change-of-state can be programmed to generate an interrupt to the CPU by setting the corresponding bit in the interrupt mask register.

The input port pulse detection circuitry uses a 38.4kHz sampling clock derived from one of the baud rate generator taps. This produces a sampling period of slightly more than 25µs (assuming a 3.6864MHz oscillator input). The detec- tion circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs coincident with the first sample pulse. The 50µs time refers to the condition where the change of state is just missed and the first change of state is not detected until after an additional 25µs.

MULT-PURPOSE OUTPUT PIN

This pin can be programmed to serve as a request-to-send output, the counter/timer output, the output for the 1X or 16X transmitter or receiver clocks, the TxRDY output or the RxRDY/FFULL output (see ACR[2:0] – MPO Output Select).

REGISTERS

The operation of the UART is programmed by writing control words in the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. Addressing of the registers is as described in Table 1.

The contents of certain control registers are initialized to zero on reset (see RESET pin description). Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems. For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. The contents of the MR, the CSR, and the ACR should only be changed while the receiver and transmitter are disabled, and certain changes to the ACR should only be made while the C/T is stopped. The bit formats of the UART are shown in Table 2.

MR1 – Mode Register 1

MR1 is accessed when the MR pointer points to MR1. The pointer is set to MR1 by RESET or by a set pointer command applied via the CR. After reading or writing MR1, the pointers are set at MR2.

MR1[7] – Receiver Request-to-Send Control

The bit controls the deactivation of the RTSN output (MPO) by the receiver. This output is normally asserted and negated by commands applied via the command register. MR1[7] = 1 causes RTSN to be automatically negated upon receipt of a valid start bit if the receiver FIFO is full. RTSN is reasserted when an empty FIFO position is available. This feature can be used to prevent overrun in the receiver by using the RTSN output signal to control the CTS input of the transmitting device.

MR1[6] – Receiver Interrupt Select

This bit selects either the receiver ready status (RxRDY) or the FIFO full status (FFULL) to be used for CPU interrupts.

MR1[5] – Error Mode Select

This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break). In the character mode, status is provided on a character-by-character basis. The status applies only to the character at the top of the FIFO. In the block mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last reset error command was issued.

MR1[4:3] – Parity Mode Select

If with parity or force parity is selected, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR![4:3] = 11 selects the channel to operate in the special wake-up mode.

MR1[2] – Parity Type Select

This bit selects the parity type (odd or even) if the with parity mode is programmed by MR1[4:3], and the polarity of the forced parity bit if the force parity mode is programmed. It has no effect if the no parity mode is programmed. In the special wake-up mode, it selects the polarity of the transmitted A/D bit.

MR1[1:0] – Bits Per Character Select

This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2 – Mode Register 2

MR2 is accessed when the channel MR pointer points to MR2, which occurs after any access to MR1. Accesses to MR2 do not change the pointer.

MR2[7:6] – Mode Select

The UART can operate in one of four modes. MR2[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxD output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e., transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU-to-receiver communication continues normally, but the CPU-to-transmitter link is disabled.

Two diagnostic modes can also be selected. MR2[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxD output is held high.
4. The RxD input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TxD output.

2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., the transmitted parity bit is as received.
5. The receiver must be enabled, but the transmitter need not be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

When switching in and out of the various modes, the selected mode is activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected, the device will switch out of the mode immediately. An exception to this is switching out of auto-echo or remote loopback modes; if the deselection occurs just after the receiver has sampled the stop bit (indicated in auto-echo by assertion o fRxRDY), and the transmitter is enabled, the transmitter is enabled, the transmitter will remain in auto-echo mode until one full stop bit has been retransmitted.

MR2[5] – Transmitter Request-to–Send Control

This bit controls the deactivation of the RTSN output (MPO) by the transmitter. This output is normally asserted and negated by appropriate commands issued via the command register. MR2[5] = 1 causes RTSN to be reset automatically one bit time after the characters in the transmit shift register and in the THR (if any) are completely transmitted (including the programmed number of stop bits) if the transmitter is not enabled. This feature can be used to automatically terminate the transmission as follows:

1. Program auto-reset mode: MR2[5] = 1.
2. Enable transmitter.
3. Assert RTSN via command.
4. Send message.
5. Disable transmitter after the last character of the message is loaded in the THR.
6. The last character will be transmitted and RTSN will be reset one bit time after the last stop bit.

Note: When TxEMT and TxRDY bits are at one just before a swrite to the Transmit Holding register, a command to disable the transmitter should be delayed until the TxRDY is at one again. TxRDY will set to one at the end of the start bit time.

Table 2. Register Bit Formats

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MR1 (Mode Register 1)							
RxRTS Control	**RxINT Select**	**Error Mode**	**Parity Mode**		**Parity Type**	**Bits per Character**	
0 = no 1 = yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With parity 01 = Force parity 10 = No parity 11 = Special mode		0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8	
MR2 (Mode Register 2)							
Channel Mode	**TxRTS Control**	**CTS Enable Tx**	**Stop Bit Length***				
00 = Normal 01 = Auto echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 =1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000	
NOTE: *Add 0.5 to values shown for 0–7 if channel is programmed for 5 bits/character.							
CSR (Clock Select Register)							
Receiver Clock Select				**Transmitter Clock Select**			
See Text				See Text			
CR (Command Register)							
Miscellaneous Commands				**Disable Tx**	**Enable Tx**	**Disable Rx**	**Enable Rx**
See Text				0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes
SR (Channel Status Register)							
Received Break	**Framing Error**	**Parity Error**	**Overrun Error**	**TxEMT**	**TxRDY**	**FFULL**	**RxRDY**
0 = No 1 = Yes *	0 = No 1 = Yes *	0 = No 1 = Yes *	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes
NOTE: *These status bits are appended to the corresponding data character in the receive FIFO. A read of the status register provides these bits [7:5] from the top of the FIFO together with bits [4;0]. These bits are cleared by a reset error status command. In character mode they are reset when the corresponding data character is read from the FIFO.							

ACR (Auxiliary Control Register)							
BRG Set Select	Counter/Timer Mode and Source			Power-Down Mode	MPO Pin Function Select		
0 = Set 1 1 = Set 2	See Text			0 = On PWRDN Active 1 = Off Normal	000 = RTSN 001 = C/TO 010 = TxC (1X) 011 = TxC (16X)		100 = RxC (1X) 101 = RxC (16X) 110 = TxRDY 111 = RxRDY/FFULL
ISR (Interrupt Status Register)							
MPI Pin Change	MPI Pin Current State	Not used	Counter Ready	Delta Break	RxRDY/ FFULL	TxEMT	TxRDY
0 = No 1 = Yes	0 = Low 1 = High		0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

Table 3. Register Bit Formats (Continued)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IMR (Interrupt Mask Resister)							
MPI Change Interrupt	MPI Level Interrupt	Not used	Counter Ready Int	Delta Break Interrupt	RxRDY/FFULL Interrupt	TxEMT Interrupt	TxRDY Interrupt
0 = Off 1 = On	0 = Off 1 = On		0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On
CTUR (Counter/Timer Upper Register)							
C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]
CTLR (Counter/Timer Lower Register)							
C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]

MR2[4] – Clear-to-Send Control
The sate of this bit determines if the CTSN input (MPI) controls the operation of the transmitter. If this bit is 0, CTSN has no effect on the transmitter. If this bit is a 1, the transmitter checks the sate of CTSN each time it is ready to send a character. If it is asserted (low), the character is transmitted. If it is negated (high), the TxD output remains in the marking state and the transmission is delayed until CTSN goes low. Changes in CTSN while a character is being transmitted do not affect the transmission of that character. This feature can be used to prevent overrun of a remote receiver.

MR2[3:0] – Stop Bit Length Select
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1–9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character length of 5 bits, 1–1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a mark condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit if parity is enabled). If an external 1X clock is used for the transmitter, MR2[3] = 0 selects one stop bit and MR2[3] = 1 selects two stop bits to be transmittted.

Table 4. Baud Rate Selection

CSR[3:0]/ [7:4]	ACR[7] = 0	ACR[7] = 1
0 0 0 0	50	75
0 0 0 1	110	110
0 0 1 0	134.5	134.5
0 0 1 1	200	150
0 1 0 0	300	300
0 1 0 1	600	600
0 1 1 0	1,200	1,200
0 1 1 1	1,050	2,000
1 0 0 0	2,400	2,400
1 0 0 1	4,800	4,800
1 0 1 0	7,200	1,800
1 0 1 1	9,600	9,600
1 1 0 0	38.4k	19.2k
1 1 0 1	Timer	Timer
1 1 1 0	MPI – 16X	MPI – 16X
1 1 1 1	MPI–1X	MPI–1X

The receiver clock is always a 16X clock, except for CSR[7:4] = 1111.

CSR – Clock Select Register

CSR[7:4] – Receiver Clock Select
This field selects the baud rate clock for the receiver as shown in Table 3. The baud rates listed are for a 3.6864MHz crystal or external clock.

CSR[3:0] – Transmitter Clock Select
This field selects the baud rate clock for the transmitter. The field definition is as shown in Table 3.

CR – Command Register

CR is used to write commands to the UART. Multiple commands can be specified in a single write to CR as long as the commands are non-conflicting, e.g., the enable transmitter and reset transmitter commands cannot be specified in a single command word.

CR[7:4] – Miscellaneous Commands

The encoded value of this field may be used to specify a single command as follows:

NOTE: Access to the upper four bits of the command register should be separated by three (3) edges of the X1 clock.

0000 No command.
0001 Reset MR pointer. Causes the MR pointer to point to MR1.
0010 Reset receiver. Resets the receiver as if a hardware reset had been applied. The receiver is disable and the FIFO is flushed.
0011 Reset transmitter. Resets the transmitter as if a hardware reset had been applied
0011 Reset error status. Clears the received break, parity error, framing error, and overrun error bits in the status register (SR[7:4]). Used in character mode to clear OE status (although RB, PE, and FE bits will also be cleared), and in block mode to clear all error status after a block of data has been received.
0101 Reset break change interrupt. Causes the break detect change bit in the interrupt status register (ISR[3]) to be cleared to zero.
0110 Start break. Forces the TxD output low (spacing). If the transmitter is empty, the start of the break condition will be delayed up to two bit times. If the transmitter is active, the break begins when transmission of the character is completed. If a character is in the THR, the start of break is delayed until that character or any others loaded after it have been transmitted (TxEMT must be true before break begins). The transmitter must be enabled to start a break
0111 Stop break. The TxD line will go high (marking) within two bit times. TxD will remain high for one bit time before the next character, if any, is transmitted.
1000 Start C/T. In counter or timer modes, causes the contents of CTUR/CTLR to be preset into the counter/timer and starts the counting cycle. In timer mode, any counting cycle in progress when the command is issued is terminated. In counter mode, has no effect unless a stop C/T command was issued previously.
1001 Stop counter. In counter mode, stops operation of the counter/timer, resets the counter ready bit in the ISR, and forces the MPO output high if it is programmed to be the output of the C/T. In timer mode, resets the counter ready bit in the ISR but has no effect on the counter/timer itself or on the MPO output.
1010 Assert RTSN. Causes the RTSN output (MPO) to be asserted (low).
1011 Negate RTSN.Causes the RTSN output (MPO) to be negated (high).
1100 Reset MPI change interrupt. Causes the MPI change bit in the interrupt status register (ISR[7]) to be cleared to zero.
1100 Reserved.
111x Reserved.

CR[3] – Disable Transmitter
This command terminates operation and resets the TxRDY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CR[2] – Enable Transmitter
Enables operation of the channel A transmitter. The TxRDY status bit will be asserted.

CR[1] – Disable Receiver
This command terminates operation of the receiver immediately; a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special wake-up mode is programmed, the receiver operates even if it is disabled (see Wake-up Mode).

CR[0] – Enable Receiver
Enables operation of the receiver. If not in the special wake-up mode, this also forces the receiver into the search for start bit state.

SR – Channel Status Register

The status register is updated while RDN is negated. Therefore, the bus interface used with this device must not use a static RDN line. The RDN line must be pulsed to allow status register updates.

SR[7] – Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received; further entries to the FIFO are inhibited until the RxD line returns to the marking state for at least one half bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the change in break bit in the ISR (ISR[3]) is set. ISR[3] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry is capable of detecting breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must last until the end of the next character time in order for it to be detected.

SR[6] – Framing Error (FE)
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SR[5]– Parity Error (PE)
This bit is set when the with parity or force parity mode is programmed and the corresponding character in the FIFO was received with incorrect parity. In special wake-up mode, the parity error bit stores the received A/D bit.

SR[4] – Overrun Error (OE)
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost. This bit is cleared by a reset error status command.

SR[3] – Transmitter Empty (TxEMT)
This bit will be set when the transmitter underruns, i.e., both the transmit holding register (THR) and the transmit shift register are empty. It is set after transmission of the last stop bit of a character, If no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU, or when the transmitter is disabled.

SR[2] – Transmitter Ready (TxRDY)
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, e.g., characters loaded in the THR while the transmitter is disabled will not be transmitted.

SR[1] – FIFO Full (FFULL)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the FIFO and there is no character in the receive shift register. If a character is waiting in the receive shift register because the FIFO is full,

FFULL will be reset by the CPU read and then set by the transfer of the character to the FIFO, which causes all three FIFO positions to be occupied.

SR[0] – Receiver Ready (RxRDY)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR, and no more characters are in the FIFO.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects one of two sets of baud rates generated by the BRG.

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.

Set 2: 75, 110, 134.5, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, and 19.2k baud.

The selected set of rates is available for use by the receiver and transmitter. See Table 4 for characteristics of the BRG.

10. *Duty cycle of 16X clock is 50% ±1%

ACR[2:0] – MPO Output Select
This field programs the MPO output pin to provide one of the following:

000 Request-to-send active-low output (RTSN). This output is asserted and negated via the command register. RTSN can be programmed to be automatically reset after the character in the transmitter is completely shifted out or when the receiver FIFO and receiver shift register are full using MR2[5] and MR1[7], respectively.

001 The counter/timer output. In the timer mode, this output is a square wave with a period of twice the value (in clock periods) of the contents of the CTUR and CTLR. In the counter mode, the output remains high until the terminal count is reached, at which time it goes low. the output returns to the high state when the counter is stopped by a stop counter command.

010 The 1X clock for the transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a non-synchronized 1X clock is output.

ACR[6:4] – Counter/Timer Mode and Clock Source Select
This field selects the operating mode of the counter/timer and its clock source as follows:

ACR [6:4]	Mode	Clock Source
0 0 0	Counter	MPI pin
0 0 1	Counter	MPI pin divided by 16
0 1 0	Counter	TxC–1X clock of the transmitter
0 1 1	Counter	Crystal or external clock (X1/CLK) divided by 16
1 0 0	Timer	MPI pin
1 0 1	Timer	MPI pin divided by 16
1 1 0	Timer	Crystal or external clock (X1/CLK)
1 1 1	Timer	Crystal or external clock (X1/CLK) divided by 16

ACR[3] – Power-Down Mode Select
This bit, when set to zero, selects the power-down mode. In this mode, the SCC2691 oscillator is stopped and all functions requiring this clock are suspended. The contents of all registers are saved. It is recommended that the transmitter and receiver be disabled prior to placing the SCC2691 in this mode. Note that this bit must be set to a logic 1 after reset.

011 The 16X clock for the transmitter. This is the clock selected by CSR[3:0] = 1111.

100 The 1X clock for the receiver, which is the clock that samples the received data. If data is not being received, a non-synchronized 1X clock is output.

101 The 16X clock for the receiver. This is the clock selected by CSR[7:4], and is a 1X clock if CSR[7:4] = 1111.

110 The transmitter register empty signal, which is the complement of SR[2]. Active low output.

111 The receiver ready or FIFO full signal (complement of ISR[2]). Active-low output.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the interrupt mask register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output is asserted (low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR; the true status is provided regardless of the contents of the IMR. This register is cleared when the device is reset.

When the power-down mode is enabled, internal circuitry forces the X1/CLK pin to the low state and the X2 pin to the high state. If an external clock is being used to drive the device, it is recommended that the clock source be three-stated or forced low while the UART is in power-down mode in order to prevent the clock driver from being short circuited.

Table 5. BRG Characteristics

Crystal or Clock = 3.6864MHz

Nom Rate (Baud)	Actual 16X* Clock (kHz)	Error (%)
50	0.8	0
75	1.2	0
110	1.759	–0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	–0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2k	307.2	0
38.4k	614.4	0

ISR[7] – MPI Change-of-State
This bit is set when a change-of-state occurs at the MPI input pin. It is reset by a reset change interrupt command.

ISR[6] – MPI Current State
This bit provides the current state of the MPI pin. This information is latched and reflects the state of the pin at the leading edge of the ISR ready cycle.

ISR[4] – Counter Ready
In the counter mode of operation, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.
In the timer mode, this bit is set once each cycle of the generated square wave (every other time the C/T reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the C/T.

ISR[3] – Change in Break
This bit, when set, indicates that the receiver has detected the beginning or end of a

received break. It is reset when the CPU issues a reset break change interrupt command.

ISR[2] – Receiver Ready or FIFO Full
The function of this bit is programmed by MR1[6]. If programmed as receiver ready, it indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the receiver FIFO. If the FIFO contains more characters, the bit will be set again after the FIFO is read. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the FIFO is read and there is no character in the receive shift register. If there is a character waiting in the receive shift register because the FIFO is full, the bit is set again when the waiting character is transferred into the FIFO.

ISR[1] – Transmitter Empty
This bit is a duplicate of TxEMT (SR[3]).

ISR[0] – Transmitter Ready
This bit is a duplicate of TxRDY (SR[2]).

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR cause an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is a '1', the INTRN output is asserted (low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded is H'0002'.

In the timer (programmable divider) mode, the C/T generates a square wave whose period is twice the value (in clock periods) of the CTUR and CTLR. The waveform so generated is often used for a data clock. The formula for calculating the divisor n to load to the CTUR and CTLR for a particular 1X data clock is shown below:

$$n = \frac{C/T\ Clock\ Frequency}{2 \times 16\ Baud\ rate\ desired}$$

Often this division will result in a non-integer number; 26.03, for example. One can only program integer numbers in a digital divider. Therefore, 26 would be chosen. This gives a baud rate error of 0.03/26.3 which is .114%; well within the ability asynchronous mode of operation.

If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half-periods will be.

The counter ready status bit (ISR[4]) is set once each cycle of the square wave. The bit is reset by a stop counter command. The command, however, does not stop the C/T. The generated square wave is output on MPO if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded in CTUR and CTLR. Counting begins upon receipt of a start C/T command. Upon reaching the terminal count, the counter ready interrupt bit (ISR[4]) is set. the counter continues counting past the terminal count until stopped by the CPU. If MPO is programmed to be the output of the C/T, the output remains high until the terminal count is reached, at which time it goes low.

The output returns to the high state and ISR[4] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command. If new values have not been loaded, the previous values are preserved and used for the next count cycle.

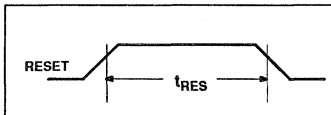


Figure 1. Reset Timing

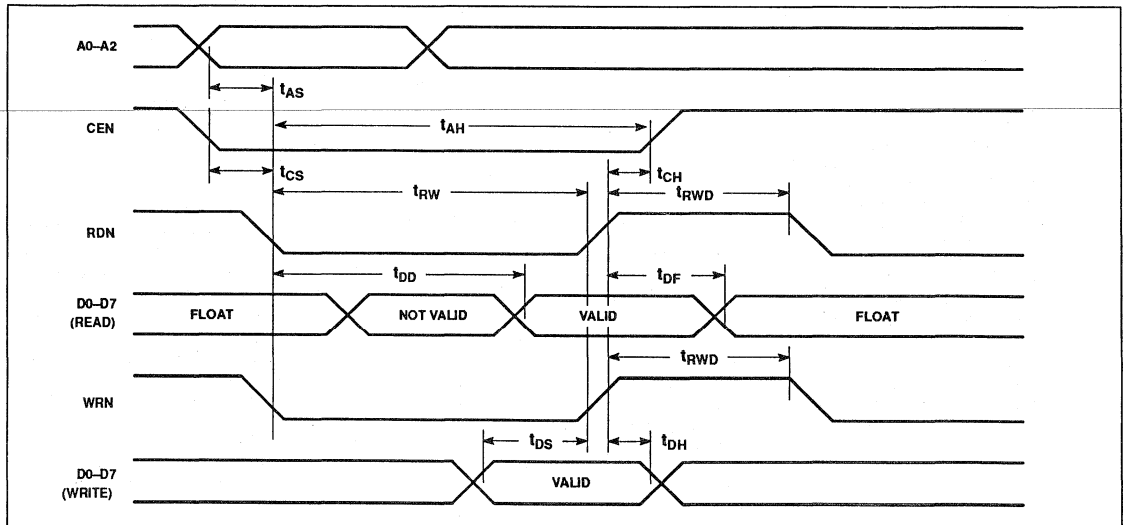


Figure 2. Bus Timing

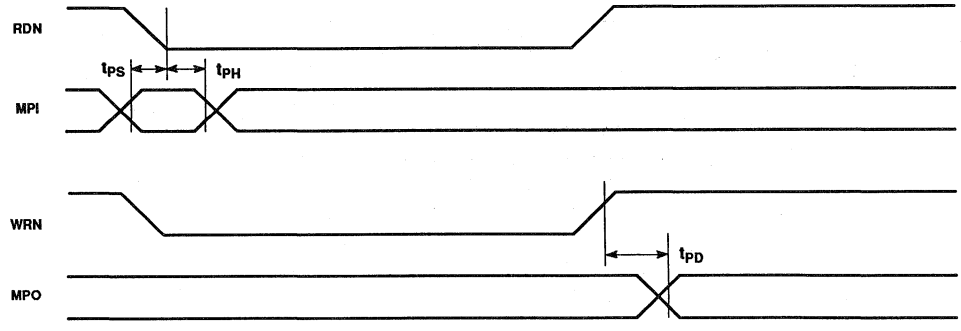
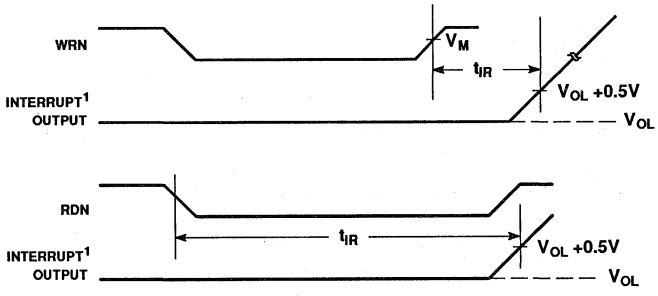


Figure 3. I/O Timing



NOTES:
1. INTRN or MPO when used as interrupt outputs.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from the midpoint of the switching signal, V_M, to a point 0.5V above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 4. Interrupt Timing

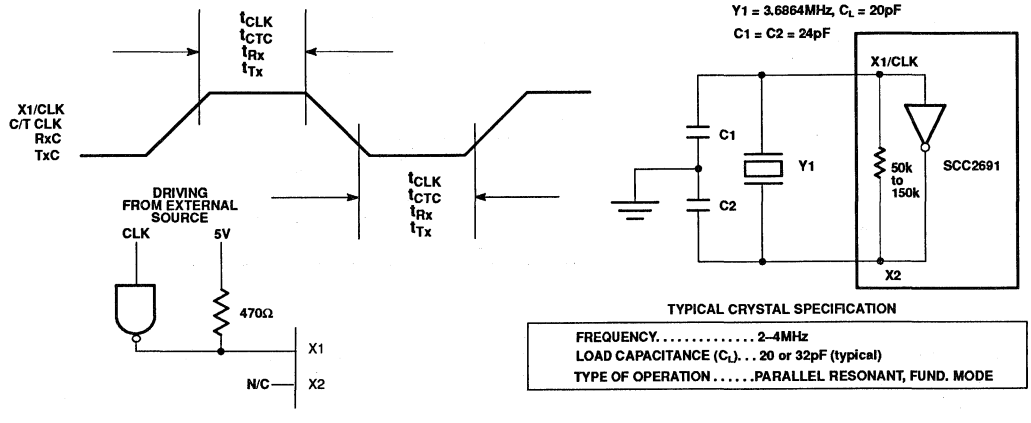


Figure 5. Clock Timing

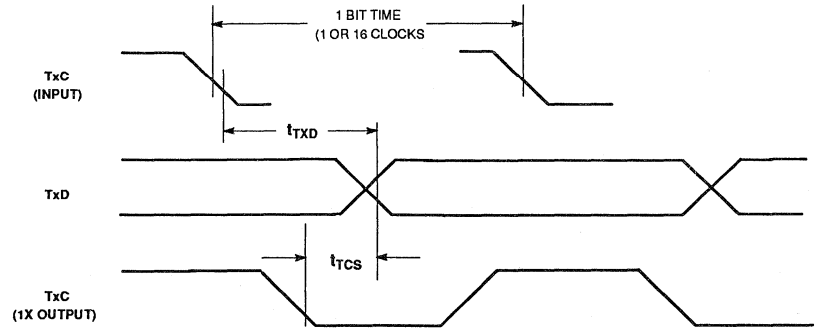


Figure 6. Transmit Timing

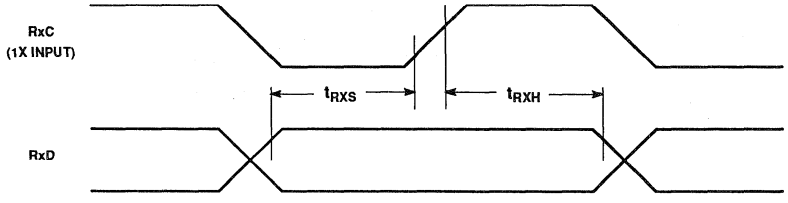
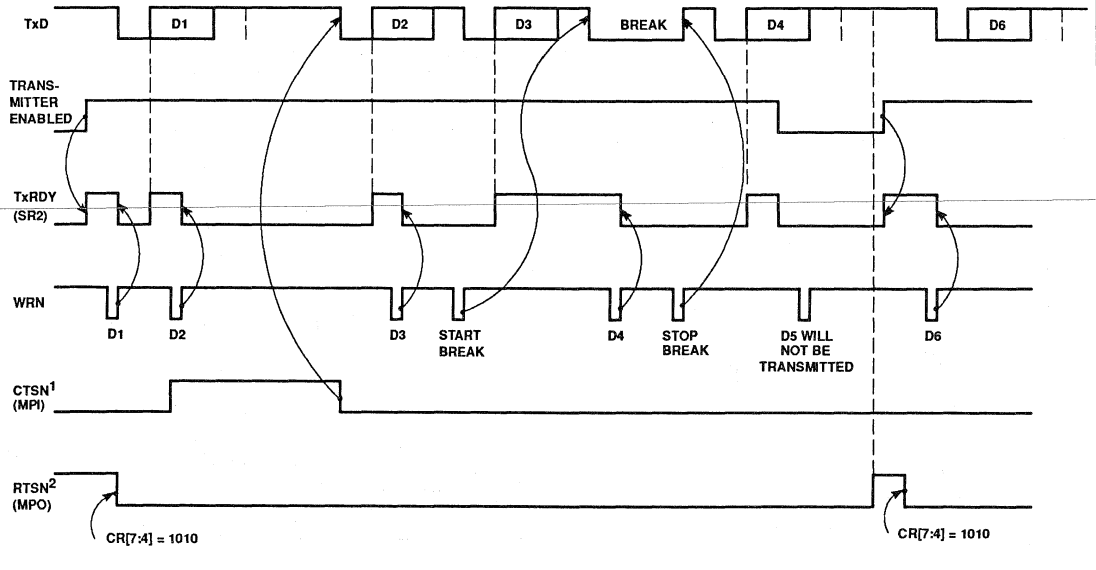


Figure 7. Receive Timing



NOTES:
1. TIMING SHOWN FOR MR2[4] = 1.
2. TIMING SHOWN FOR MR2[5] = 1.

Figure 8. Transmitter Timing

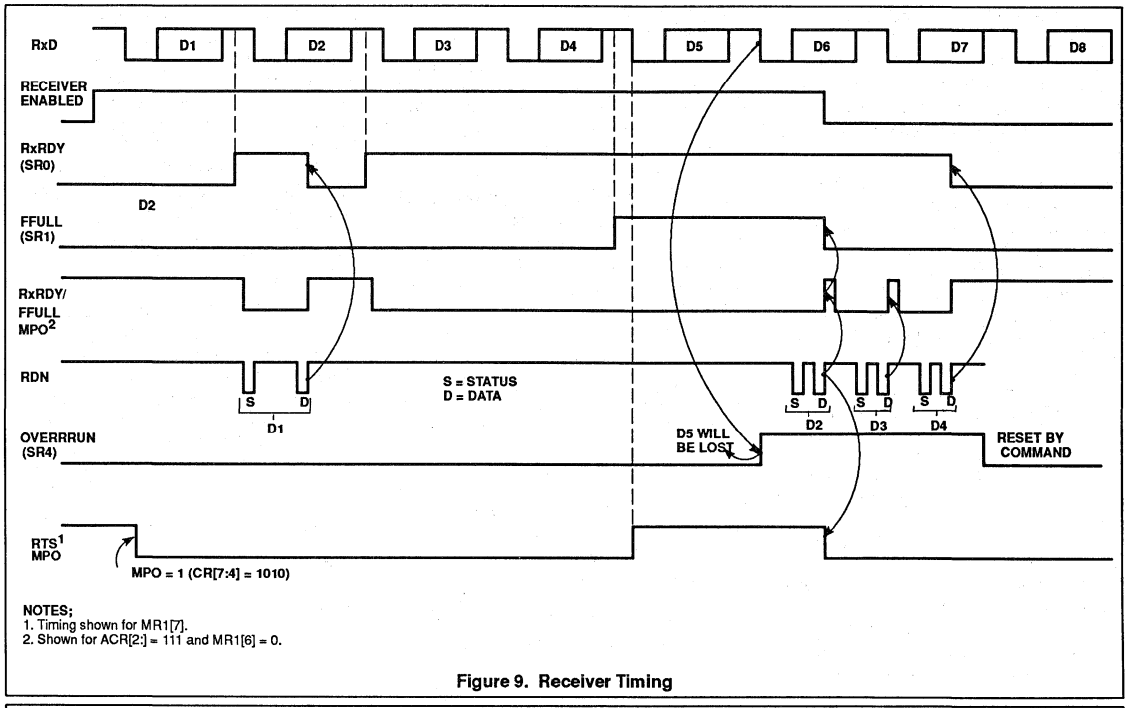


Figure 9. Receiver Timing

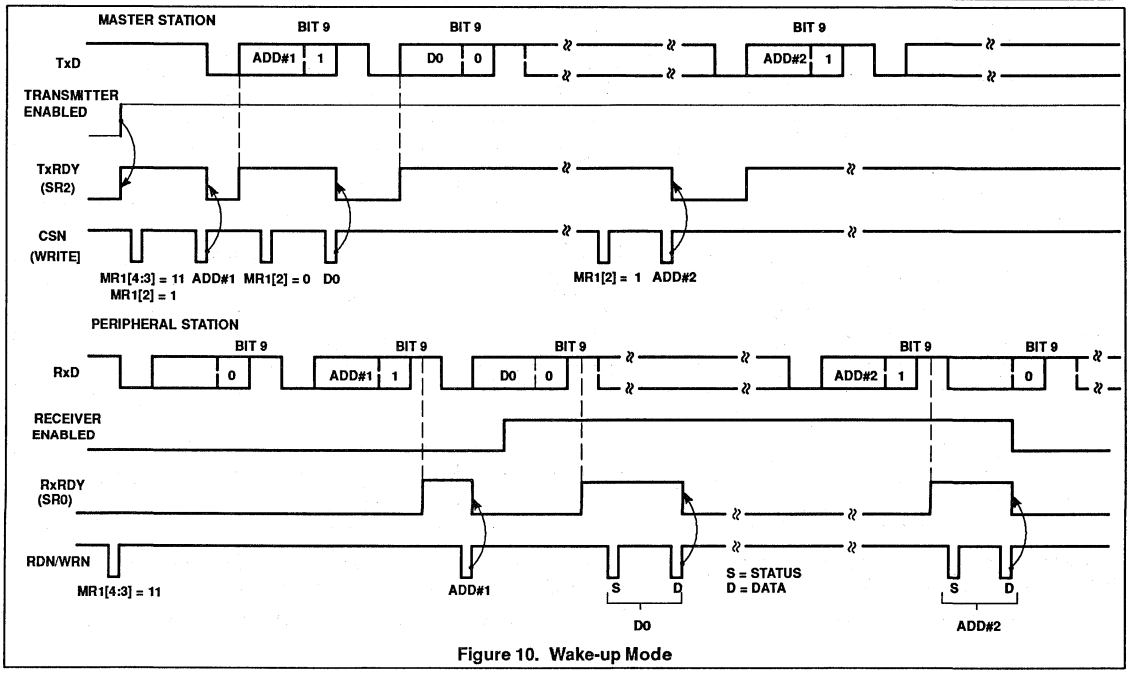


Figure 10. Wake-up Mode

The CTS, RTS, CTS Enable Tx signals

CTS (Clear To Send) is usually meant to be a signal to the transmitter meaning that it may transmit data to the receiver. The CTS input is on pin MPI. The CTS signal is active low; thus, it is called CTSN.

RTS is usually meant to be a signal from the receiver indicating that the receiver is ready to receive data. It is also active low and is, thus, called RTSN. RTSN is on pin MP0. A receiver's RTS output will usually be connected to the CTS input of the associated transmitter. Therefore, one could say that RTS and CTS are different ends of the same wire!

MR2(4) is the bit that allows the transmitter to be controlled by the CTS pin (MPI). When this bit is set to one AND the CTS input is driven high, the transmitter will stop sending data at the end of the present character being serialized. It is usually the RTS output of the receiver that will be connected to the transmitter's CTS input. The receiver will set RTS high when the receiver FIFO is full AND the start bit of the fourth character is sensed. Transmission then stops with four valid characters in the receiver. When MR2(4) is set to one, CTSN must be at zero for the transmitter to operate. If MR2(4) is set to zero, the MP pin will have no effect on the operation of the transmitter.

MR1(7) is the bit that allows the receiver to control MP0. When MP0 is controlled by the receiver, the meaning of that pin will be RTS. However, a point of confusion arises in that MP0 may also be controlled by the transmitter. When the transmitter is controlling this pin, its meaning is not RTS at all. It is, rather, that the transmitter has finished sending its last data byte. Programming the MP0 pin to be controlled by the receiver and the transmitter at the same time is allowed, but would usually be incompatible.

RTS can also be controlled by the commands 1010 and 1011 in the command register. RTS is expressed at the MP0 pin which is still an output port. Therefore, the state of MP0 should be set low (by commands to the CR register) for the receiver to generate the proper RTS signal. The logic at the output is basically a NAND of the MP0 bit register and the RTS signal as generated by the receiver. When the RTS flow control is selected via the MR(7) bit the state of the MP0 register is not changed. Terminating the use of "Flow Control" (via the MR registers) will return the MP0 pin to the control of the MP0 register.

Transmitter Disable Note

The sequence of instructions enable transmitter — load transmit holding register — disable transmitter will result in nothing being sent if the time between the end of loading the transmit holding register and the disable command is less that 3/16 bit time in the 16x mode or one bit time in the 1x mode. Also, if the transmitter, while in the enabled state and underrun condition, is immediately disabled after a single character is loaded to the transmit holding register, that character will not be sent.

In general, when it is desired to disable the transmitter before the last character is sent AND the TxEMT bit is set in the status register (TxEMT is always set if the transmitter has underrun or has just been enabled), be sure the TxRDY bit is active immediately before issuing the transmitter disable instruction. TxRDY sets at the end of the "start bit" time. It is during the start bit that the data in the transmit holding register is transferred to the transmit shift register.

Non-standard baud rates are available as shown in Table 6 below, via the BRG Test function.

Table 6. Baud Rate

	Normal BRG		BRG Test	
CSR[7:4]	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0000	50	75	4,800	7,200
0001	110	110	880	880
0010	134.5	38.4K	1,076	38.4K
0011	200	150	19.2K	14.4K
0100	300	300	28.8K	28.8K
0101	600	600	57.6K	57.6K
0110	1,200	1,200	115.2K	115.2K
0111	1,050	2,000	1,050	2,000
1000	2,400	2,400	57.6K	57.6K
1001	4,800	4,800	4,800	4,800
1010	7,200	1,800	57.6K	14.4K
1011	9,600	9,600	9,600	9,600
1100	38.4K	19.2K	38.4K	19.2K
1101	Timer	Timer	Timer	Timer
1110	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X
1111	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X

NOTE:
Each read on address H'2' will toggle the baud rate test mode. When in the BRG test mode, the baud rates change as shown to the left. This change affects all receivers and transmitters on the DUART. Also, the RTSN output (MP0) become the transmitter 1x clock.

The test mode at address H'2' changes all transmitters and receivers to the 1x mode and connects the output ports to some internal nodes.

Dual asynchronous receiver/transmitter (DUART) SCC2692

DESCRIPTION

The Signetics SCC2692 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip CMOS-LSI communications device that provides two full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruply buffered to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the receiver buffer is full.

Also provided on the SCC2692 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

The SCC2692 is available in three package versions: 40-pin and 28-pin, 0.6" wide, DIPs and a 44-pin PLCC.

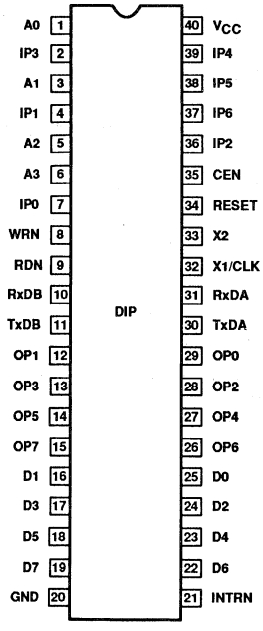
FEATURES

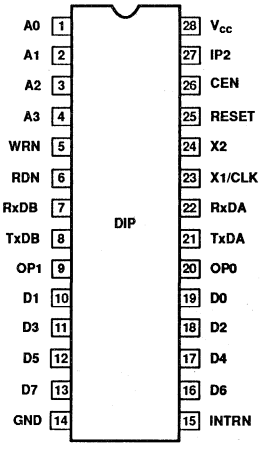
- Dual full-duplex asynchronous receiver/transmitters
- Quadruple buffered receiver data register
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4k baud
  - Non-standard rates to 115.2Kb
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer rates: 1X – 1MB/sec, 16X – 125kB/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Power down mode
- Receiver timeout mode
- Commercial and industrial temperature range versions
- TTL compatible
- Single +5V power supply

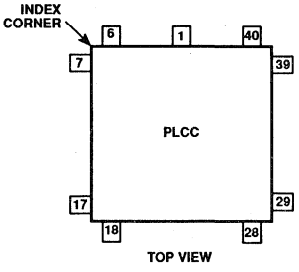
ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±10%, T_A = 0 to +70°C	V_{CC} = +5V ±10%, T_A = -40 to +85°C
40-Pin Cerdip	SCC2692AC1F40	SCC2692AE1F40
28-Pin Cerdip	SCC2692AC1F28	SCC2692AE1F28
40-Pin Plastic DIP	SCC2692AC1N40	SCC2692AE1N40
28-Pin Plastic DIP	SCC2692AC1N28	SCC2692AE1N28
44-Pin Plastic LCC	SCC2692AC1A44	SCC2692AE1A44

PIN CONFIGURATIONS



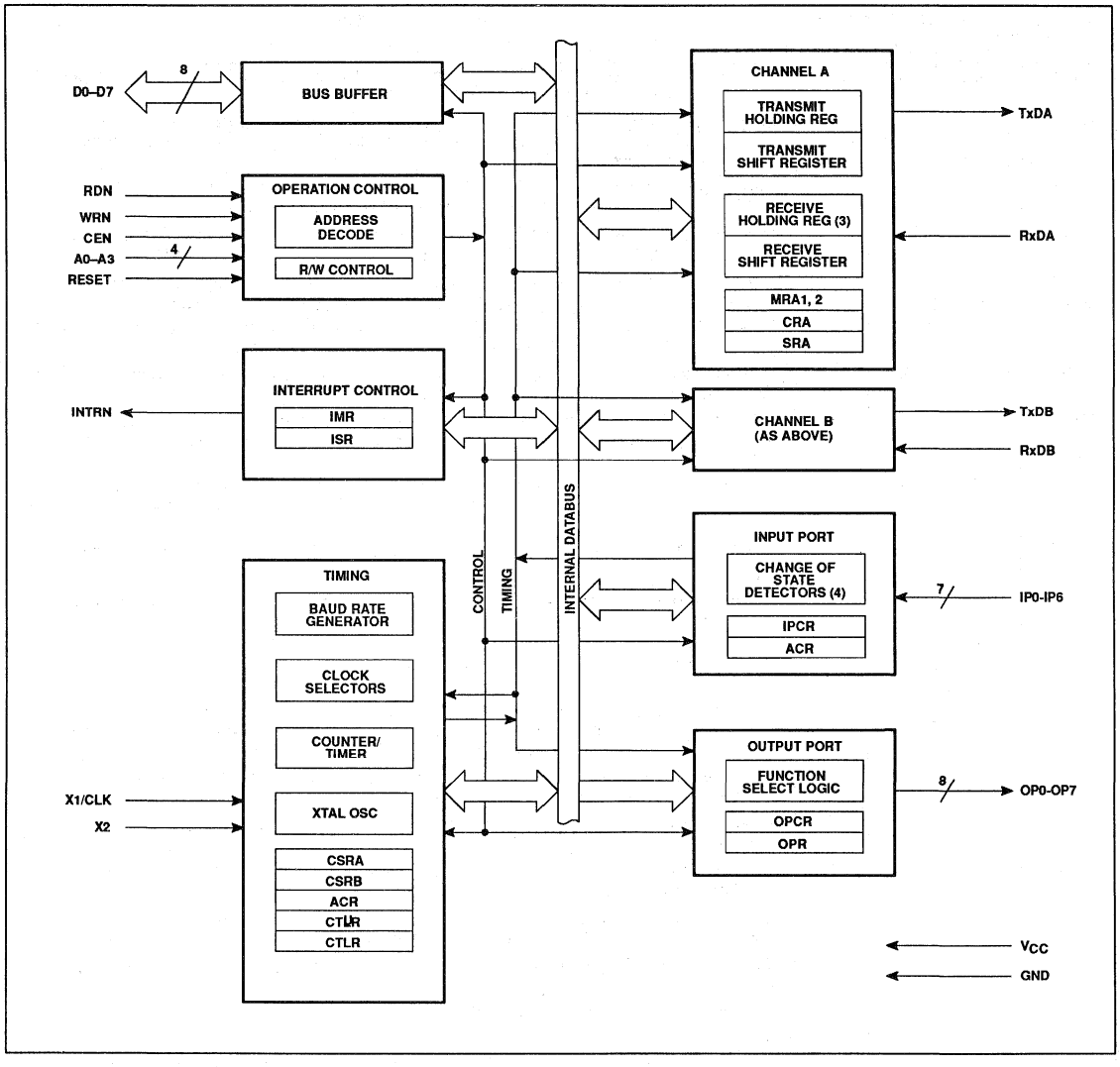




TOP VIEW

PIN/FUNCTION		PIN/FUNCTION	
1	NC	23	NC
2	A0	24	INTRN
3	IP3	25	D6
4	A1	26	D4
5	IP1	27	D2
6	A2	28	D0
7	A3	29	OP6
8	IP0	30	OP4
9	WRN	31	OP2
10	RDN	32	OP0
11	RXDB	33	TXDA
12	NC	34	NC
13	TXDB	35	RXDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CEN
18	D1	40	IP2
19	D3	41	IP6
20	D5	42	IP5
21	D7	43	IP4
22	GND	44	VCC

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	APPLICABLE		TYPE	NAME AND FUNCTION
	40,44	28		
D0-D7	X	X	I/O	**Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	X	X	I	**Chip Enable:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the WRN, RDN and A0-A3 inputs. When High, places the D0-D7 lines in the 3-State condition.
WRN	X	X	I	**Write Strobe:** When Low and CEN is also Low, the contents of the data bus are loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	X	X	I	**Read Strobe:** When Low and CEN is also Low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0-A3	X	X	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	X	X	I	**Reset:** A High level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0-OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Resets Test modes.
INTRN	X	X	O	**Interrupt Request:** Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	X	X	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5).
X2	X	X	I	**Crystal 2:** Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5). If X1/CLK is driven from an external source, this pin can be left open or connected to ground.
RxDA	X	X	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	X	X	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	X	X	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
TxDB	X	X	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is High, 'space' is Low.
OP0	X	X	O	**Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	X	X	O	**Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	X		O	**Output 2:** General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	X		O	**Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	X		O	**Output 4:** General purpose output or Channel A open-drain, active-Low, RxRDYAN/FFULLAN output.
OP5	X		O	**Output 5:** General purpose output or Channel B open-drain, active-Low, RxRDYBN/FFULLBN output.
OP6	X		O	**Output 6:** General purpose output or Channel A open-drain, active-Low, TxRDYAN output.
OP7	X		O	**Output 7:** General purpose output, or Channel B open-drain, active-Low, TxRDYBN output.
IP0	X		I	**Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	X		I	**Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	X	X	I	**Input 2:** General purpose input or counter/timer external clock input.
IP3	X		I	**Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.

PIN DESCRIPTION (Continued)

SYMBOL	APPLICABLE		TYPE	NAME AND FUNCTION
	40,44	28		
IP4	X		I	**Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	X		I	**Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6	X		I	**Input 6:** General purpose input or Channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
V_{CC}	X	X	I	**Power Supply:** +5V supply input.
GND	X	X	I	**Ground**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	Note 4	°C
T_{STG}	Storage temperature range	-65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	-0.5 to +7.0	V
V_S	Voltage from any pin to GND[3]	-0.5 to V_{CC} +0.5	V
P_D	Power dissipation	750	mW

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
V_{IL}	Input low voltage					V
V_{IH}	Input high voltage (except X1/CLK)[6]		2.0		0.8	V
V_{IH}	Input high voltage (except X1/CLK)[7]		2.5			V
V_{IH}	Input high voltage (X1/CLK)		0.8 V_{CC}			V
V_{OL}	Output low voltage	I_{OL} = 2.4mA			0.4	V
V_{OH}	Output high voltage (except OD outputs)[4]	I_{OH} = -400µA	V_{CC} -0.5			V
I_{IX1PD}	X1/CLK input current - power down	V_{IN} = 0 to V_{CC}	-10		+10	µA
I_{ILX1}	X1/CLK input low current - operating	V_{IN} = 0	-75		0	µA
I_{IHX1}	X1/CLK input high current - operating	V_{IN} = V_{CC}	0		75	µA
I_{OHX2}	X2 output high current - operating	V_{OUT} = V_{CC}, X1 = 0	0		+75	µA
I_{OHX2S}	X2 output high short circuit current - operating	V_{OUT} = 0, X1 = 0	-10		-1	mA
I_{OLX2}	X2 output low current - operating	V_{OUT} = 0, X1 = V_{CC}	-75		0	µA
I_{OLX2S}	X2 output low short circuit current - operating and power down	V_{OUT} = V_{CC}, X1 = V_{CC}	1		10	mA
I_I	Input leakage current:					
	All except input port pins	V_{IN} = 0 to V_{CC}	-10		+10	µA
	Input port pins	V_{IN} = 0 to V_{CC}	-20		+10	µA
I_{OZH}	Output off current high, 3-state data bus	V_{IN} = V_{CC}			10	µA
I_{OZL}	Output off current low, 3-state data bus	V_{IN} = 0V	-10			µA
I_{ODL}	Open-drain output low current in off-state	V_{IN} = 0	-10			µA
I_{ODH}	Open-drain output high current in off-state	V_{IN} = V_{CC}			10	µA
I_{CC}	Power supply current[5]					
	Operating mode	TTL input levels			10	mA
		CMOS input levels			10	mA
	Power down mode[8]	TTL input levels			3.0	mA
		CMOS input levels			2.0	mA

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7KΩ to V_{CC}.
5. All outputs are disconnected. Inputs are switching between TTL levels of 2.4V and 0.4V or CMOS levels of V_{CC} -0.2V and V_{SS} + 0.2V.
6. $T_A \geq 0°C$
7. $T_A < 0°C$
8. See UART application note for 5µA.

AC CHARACTERISTICS[1, 2, 4]

SYMBOL	PARAMETER	LIMITS Min	LIMITS Typ[3]	LIMITS Max	UNIT
Reset Timing (See Figure 1)					
t_{RES}	RESET pulse width	200			ns
Bus Timing[5] (See Figure 2)					
t_{AS}	A0-A3 setup time to RDN, WRN Low	10			ns
t_{AH}	A0-A3 hold time from RDN, WRN Low	100			ns
t_{CS}	CEN setup time to RDN, WRN Low	0			ns
t_{CH}	CEN hold time from RDN, WRN High	0			ns
t_{RW}	WRN, RDN pulse width	225			ns
t_{DD}	Data valid after RDN Low			175	ns
t_{DA}	RDN Low to data bus active[7]	15			ns
t_{DF}	Data bus floating after RDN High			125	ns
t_{DI}	RDN High to data bus invalid[7]	20			ns
t_{DS}	Data setup time before WRN High	100			ns
t_{DH}	Data hold time after WRN High	20			ns
t_{RWD}	High time between reads and/or writes[5, 6]	200			ns

AC CHARACTERISTICS (Continued)[1, 2, 4]

SYMBOL	PARAMETER	LIMITS Min	Typ[3]	Max	UNIT
Port Timing[5] (See Figure 3)					
t_{PS}	Port input setup time before RDN Low	0			ns
t_{PH}	Port input hold time after RDN High	0			ns
t_{PD}	OP_n output valid from WRN High			400	ns
Interrupt Timing (See Figure 4)					
t_{IR}	INTRN (or OP3-OP7 when used as interrupts) negated from:				
	Read RHR (RxRDY/FFULL interrupt)			300[9]	ns
	Write THR (TxRDY interrupt)			300[9]	ns
	Reset command (break change interrupt)			300[9]	ns
	Stop C/T command (counter interrupt)			300[9]	ns
	Read IPCR (input port change interrupt)			300[9]	ns
	Write IMR (clear of interrupt mask bit)			300[9]	ns
Clock Timing (See Figure 5)					
t_{CLK}	X1/CLK High or Low time	100			ns
f_{CLK}	X1/CLK frequency[10]	0	3.6864	4	MHz
t_{CTC}	CTCLK (IP2) High or Low time	100			ns
f_{CTC}	CTCLK (IP2) frequency[8]	0		4	MHz
t_{RX}	RxC High or Low time	220			ns
f_{RX}	RxC frequency (16X)[8]	0		2	MHz
	(1X)[8]	0		1	MHz
t_{TX}	TxC High or Low time	220			ns
f_{TX}	TxC frequency (16X)[8]	0		2	MHz
	(1X)[8]	0		1	MHz
Transmitter Timing (See Figure 6)					
t_{TXD}	TxD output delay from TxC Low (TxC input pin)			350	ns
t_{TCS}	Output delay from TxC Low to TxD data output (TxC 1x output pin)	0		150	ns
Receiver Timing (See Figure 7)					
t_{RXS}	RxD data setup time to RxC High	240			ns
t_{RXH}	RxD data hold time from RxC High	200			ns

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7KΩ to V_{CC}.
5. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. CEN and RDN (also CEN and WRN) are ORed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
6. If CEN is used as the 'strobing' input, the parameter defines the minimum High times between one CEN and the next. The RDN signal must be negated for t_{RWD} to guarantee that any status register changes are valid.
7. Guaranteed by characterization of sample units.
8. Minimum frequencies are not tested but are guaranteed by design.
9. 325ns maximum for T_A > 70°C.
10. Operation to 0MHz is assured by design. Minimum test frequency is 2.0MHz.

BLOCK DIAGRAM

The SCC2692 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the Block Diagram.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer.

Interrupt Control

A single active-Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR). The IMR can be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to

determine all currently active interrupting conditions.

Outputs OP3-OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART.

If an external clock is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 5.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. A 3.6864MHz crystal or external clock must be used to get the standard baud rate. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

The Counter/Timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

Communications Channels A and B

Each communications channel of the SCC2692 comprises a full-duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

Input Port

The inputs to this unlatched 7-bit port can be read by the CPU by performing a read operation at address H'D'. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always read as a logic 1. The pins of this port can also serve as auxiliary inputs to certain portions fo the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs, lasting longer than 25 - 50µs, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU.

The input port pulse detection circuitry uses a 38.4KHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25µs (this assumes that the clock input is 3.6864MHz). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs "coincident with the first sample pulse". The 50µs time refers to the situation in which the change-of-state is "just missed" and the first change-of-state is not detected until 25µs later.

Output Port

The output port pins may be controlled by the OPR, OPCR, MR and CR registers. Via appropriate programming they may be just another parallel port to external circuits, or they may represent many internal conditions of the UART. When this 8-bit port is used as a general purpose output, the pins so defined will assume the compliment of the associated bit in the Output Port Register (OPR). OPR(n) = 1 results in OP(n) = Low and vice versa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operation at address H'E' with the accompanying data specifying the bits to be reset (1 = set, 0 = no change). Likewise, a bit is reset by a write at address H'F' with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Outputs can be also individually assigned specific functions by appropriate programming of the Channel A mode registers (MR1A, MR2A), the Channel B mode registers (MR1B, MR2B), and the Output Port Configuration Register (OPCR).

OPERATION

Transmitter

The SCC2692 is conditioned to transmit data when the transmitter is enabled through the command register. The SCC2692 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When a character is loaded into the Transmit Holding Register (THR), the above conditions are negated. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again which means one full character time of buffering is provided. Characters cannot be loaded into the THR while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains High and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the THR.

If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous Low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS operation is enable, the CTSN input must be Low in

order for the character to be transmitted. If it goes High in the middle of a transmission, the character in the shift register is transmitted and TxDA then remains in the marking state until CTSN goes Low. The transmitter can also control the deactivation of the RTSN output. If programmed, the RTSN output will be reset one bit time after the character in the transmit shift register and transmit holding register (if any) are completely transmitted, if the transmitter has been disabled.

Receiver

The SCC2692 is conditioned to receive data when enabled through the command register. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive Holding Register (RHR) and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than 8 bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1. The RxD input must return to a High condition for at least one-half bit time before a search for the next start bit begins.

The RHR consists of a First-In-First-Out (FIFO) stack with a capacity of three characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4] will be set-upon receipt of the start bit of the new (overrunning) character.

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

Timeout Mode

The timeout mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RHR, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU may not know there is data left in the FIFO. The CTU and CTL value would be programmed for just over one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all of the characters from the FIFO, but the last character received has started the count. If there is no new data during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

This mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the timeout mode for that channel. Writing a 'Cx' to CRA or CRB will disable the timeout mode. The timeout mode should only be used by one channel at once, since it uses the C/T. CTU and CTL must be loaded with a value greater than the normal receive character period. The timeout mode disables the regular START/STOP Counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RHR, the C/T is stopped after 1 C/T clock, reloaded with the value in CTU and CTL and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate

Table 1. SCC2692 Register Addressing

A3	A2	A1	A0	READ (RDN = 0)	WRITE (WRN = 0)
0	0	0	0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	BRG Test	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RHRA)	Tx Holding Register A (THRA)
0	1	0	0	Input Port Change Register (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Register (CRUR)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Register (CTLR)
1	0	0	0	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	1X/16X Test	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RHRB)	Tx Holding Register B (THRB)
1	1	0	0	Reserved	Reserved
1	1	0	1	Input Port (IPR)	Output Port Conf. Register (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command
1	1	1	1	Stop Counter Command	Reset Output Port Bits Command

an interrupt. Since receiving a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Timeout Mode On' command, CRx = 'Ax', will also clear the counter ready bit and stop the counter until the next character is received.

Multidrop Mode

The DUART is equipped with a wake up mode for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wakeup' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the THR.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RHR FIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems.

For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to MR1X by RESET or by issuing a 'reset pointer' command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1X, switches the pointer to MR2X. The pointer then remains at MR2X, so that subsequent accesses are always to MR2X unless the pointer is reset to MR1X as described above.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'0A' should never be read during normal operation since they are reserved for internal diagnostics.

MR1A – Channel A Mode Register 1

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRA. After reading or writing MR1A, the pointer will point to MR2A.

MR1A[7] – Channel A Receiver Request-to-Send Control

This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR1A[7] = 1 causes RTSAN to be negated upon receipt of a valid start bit if the Channel A FIFO is full. However, OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

MR1A[6] – Channel A Receiver Interrupt Select

This bit selects either the Channel A receiver ready status (RxRDY) or the Channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to

be output on OP4 if it is programmed as an interrupt output via the OPCR.

MR1A[5] – Channel A Error Mode Select
This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break) for Channel A. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

MR1A[4:3| – Channel A Parity Mode Select
If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data MR1A[4:3] = 11 selects Channel A to operate in the special multidrop mode described in the Operation section.

MR1A[2] – Channel A Parity Type Select
This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

MR1A[1:0] – Channel A Bits Per Character Select
This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2A – Channel A Mode Register 2

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

MR2A[7:6] – Channel A Mode Select
Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The Channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop has been re-transmitted.

MR2A[5] – Channel A Transmitter Request-to-Send Control
This bit controls the deactivation of the RTSAN output (OP0) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR2A[5] = 1 causes OPR[0] to be reset automatically one bit time after the characters in the Channel A transmit shift register and in the THR, if any, are completely transmitted including the programmed number of stop bits, if the transmitter is not enabled. This feature can be used to automatically terminate the transmission of a message as follows:

1. Program auto-reset mode: MR2A[5] = 1.
2. Enable transmitter.
3. Assert RTSAN: OPR[0] = 1.
4. Send message.
5. Disable transmitter after the last character is loaded into the Channel A THR.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

Note: When TxEMT and TxRDY bits are at one just before a write to the Transmit Holding register, a command to disable the transmitter should be delayed until the TxRDY is at one again. TxRDY will set to one at the end of the start bit time.

MR2A[4] – Channel A Clear-to-Send Control
If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IPO) each time it is ready to send a character. If IPO is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character..

MR2A[3:0] – Channel A Stop Bit Length Select
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1-9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1-1/16 to 2 stop

bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit is enabled).

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

Table 2. Register Bit Formats

	BIT 7	BIT 6	BIT 5	BIT 4 BIT 3	BIT 2	BIT 1 BIT 0
	RxRTS CONTROL	**RxINT SELECT**	**ERROR MODE**	**PARITY MODE**	**PARITY TYPE**	**BITS PER CHARACTER**
MR1A MR1B	0 = No 1 = Yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multidrop Mode	0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8

	BIT 7 BIT 6	BIT 5	BIT 4	BIT 3 BIT 2 BIT 1 BIT 0
	CHANNEL MODE	**TxRTS CONTROL**	**CTS ENABLE Tx**	**STOP BIT LENGTH***
MR2A MR2B	00 = Normal 01 = Auto-Echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 4 = 0.813 8 = 1.563 C = 1.813 1 = 0.625 5 = 0.875 9 = 1.625 D = 1.875 2 = 0.688 6 = 0.938 A = 1.688 E = 1.938 3 = 0.750 7 = 1.000 B = 1.750 F = 2.000

NOTE:
*Add 0.5 to values shown for 0 – 7 if channel is programmed for 5 bits/char.

	BIT 7 BIT 6 BIT 5 BIT 4	BIT 3 BIT 2 BIT 1 BIT 0
	RECEIVER CLOCK SELECT	**TRANSMITTER CLOCK SELECT**
CSRA CSRB	See Text	See Text

	BIT 7 BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MISCELLANEOUS COMMANDS	**DISABLE Tx**	**ENABLE Tx**	**DISABLE Rx**	**ENABLE Rx**
CRA CRB	See Text and Timing Requirement	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
Access to the upper four bits of the command register should be separated by three (3) edges of the X1 clock.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RECEIVED BREAK*	**FRAMING ERROR***	**PARITY ERROR***	**OVERRUN ERROR**	**TxEMT**	**TxRDY**	**FFULL**	**RxRDY**
SRA SRB	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
* These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a "reset error status" command. In character mode they are discarded when the corresponding data character is read from the FIFO.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3 BIT 2	BIT 1 BIT 0
	OP7	**OP6**	**OP5**	**OP4**	**OP3**	**OP2**
OPCR	0 = OPR[7] 1 = TxRDYB	0 = OPR[6] 1 = TxRDYA	0 = OPR[5] 1 = RxRDY/ FFULLB	0 = OPR[4] 1 = RxRDY/ FFULLA	00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB(1X) 11 = RxCB(1X)	00 = OPR[2] 01 = TxCA(16X) 10 = TxCA(1X) 11 = RxCA(1X)

Table 2. Register Bit Formats (Continued)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	BRG SET SELECT	COUNTER/TIMER MODE AND SOURCE			DELTA IP 3 INT	DELTA IP 2 INT	DELTA IP 1 INT	DELTA IP 0 INT
ACR	0 = set 1 1 = set 2	See Table 4			0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	DELTA IP 3	DELTA IP 2	DELTA IP 1	DELTA IP 0	IP 3	IP 2	IP 1	IP 0
IPCR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	INPUT PORT CHANGE	DELTA BREAK B	RxRDY/ FFULLB	TxRDYB	COUNTER READY	DELTA BREAK A	RxRDY/ FFULLA	TxRDYA
ISR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IN. PORT CHANGE INT	DELTA BREAK B INT	RxRDY/ FFULLB INT	TxRDYB INT	COUNTER READY INT	DELTA BREAK A INT	RxRDY/ FFULLA INT	TxRDYA INT
IMR	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]
CTUR								

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]
CTLR								

MR1B – Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to MR1A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

MR2B – Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode register are identical to the bit definitions for MR2A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

CSRA – Channel A Clock Select Register

CSRA[7:4] – Channel A Receiver Clock Select

This field selects the baud rate clock for the Channel A transmitter. The field definition is shown in Table 3.

CSRA[3:0] – Channel A Transmitter Clock Select

This field selects the baud rate clock for the Channel A transmitter. The field definition is as shown in Table 3, except as follows:

CSRA[3:0]	ACR[7] = 0	ACR[7] = 1
1110	IP3-16X	IP3-16X
1111	IP3-1X	IP3-1X

The transmitter clock is always a 16X clock except for CSRA[3:0] = 1111.

Table 3. Baud Rate

CSRA[7:4]	ACR[7] = 0	ACR[7] = 1
0000	50	75
0001	110	110
0010	134.5	134.5
0011	200	150
0100	300	300
0101	600	600
0110	1,200	1,200
0111	1,050	2,000
1000	2,400	2,400
1001	4,800	4,800
1010	7,200	1,800
1011	9,600	9,600
1100	38.4K	19.2K
1101	Timer	Timer
1110	IP4-16X	IP4-16X
1111	IP4-1X	IP4-1X

NOTE: The receiver clock is always a 16X clock except for CSRA[7:4] = 1111. Also, see Table 6 for baud rates available in BRG Test.

CSRB – Channel B Clock Select Register

CSRB[7:4] – Channel B Receiver Clock Select
This field selects the baud rate clock for the Channel B receiver. The field definition is as shown in Table 3, except as follows:

CSRB[7:4]	ACR[7] = 0	ACR[7] = 1
1110	IP6-16X	IP6-16X
1111	IP6-1X	IP6-1X

The receiver clock is always a 16X clock except for CSRB[7:4] = 1111.

CSRB[3:0] – Channel B Transmitter Clock Select
This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 3, except as follows:

CSRB[3:0]	ACR[7] = 0	ACR[7] = 1
1110	IP5-16X	IP5-16X
1111	IP5-1X	IP5-1X

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

CRA – Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

CRA[7:4] – Miscellaneous Commands
Sequential writes to CR(7:4) should be separated by three edges of the X1 clock.

The encoded value of this field may be used to specify a single command as follows:

0000 No command.
0001 Reset MR pointer. Causes the Channel A MR pointer to point to MR1.
0010 Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.
0011 Reset transmitter. Resets the Channel A transmitter as if a hardware reset had been applied.
0100 Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.
0101 Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.
0110 Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.
0111 Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted.
1000 Assert RTSN. Causes the RTSN output to be asserted (Low).
1001 Negate RTSN. Causes the RTSN output to be negated (High).
1010 Set Timeout Mode On. The receiver in this channel will restart the C/T as each receive character is transferred from the shift register to the RHR. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset. The counter will not start until the first character is received after the command is issued.
1011 Not used.
1100 Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued to reset the ISR(3) bit.
1101 Not used.
1110 Power Down Mode On. In this mode, the DUART oscillator is stopped and all functions requiring this clock are suspended. The execution of commands other than disable power down mode (1111) requires a X1/CLK. While in the power down mode, do not issue any commands to the CR except the disable power down mode command. The contents of all registers will be saved while in this mode. . It is recommended that the transmitter and receiver be disabled prior to placing the DUART into power down mode. This command is in CRA only.
1111 Disable Power Down Mode. This command restarts the oscillator. After invoking this command, wait for the oscillator to start up before writing further commands to the CR. This command is in CRA only.

CRA[3] – Disable Channel A Transmitter
This command terminates transmitter operation and resets the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CRA[2] – Enable Channel A Transmitter
Enables operation of the Channel A transmitter. The TxRDY status bit will be asserted.

CRA[1] – Disable Channel A Receiver
This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

CRA[0] – Enable Channel A Receiver
Enables operation of the Channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start bit state.

CRB – Channel B Command Register

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, with the exception of comamnds "Ex" and "Fx" which are used for power downmode. These two commands are not used in CRB. All other control actions that apply to CRA also apply to CRB.

SRA – Channel A Status Register

SRA[7] – Channel A Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line to the marking state for at least one-half a bit time (two

successive edges of the internal or external 1X clock).

When this bit is set, the Channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

SRA[6] – Channel A Framing Error
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SRA[5] – Channel A Parity Error
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

In the special multidrop mode the parity error bit stores the receive A/D bit.

SRA[4] – Channel A Overrun Error
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost.

This bit is cleared by a 'reset error status' command.

SRA[3] – Channel A Transmitter Empty (TxEMTA)
This bit will be set when the Channel A transmitter underruns; i.e., both the Transmit Holding Register (THR) and the transmit shift register are empty. It is set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU or when the transmitter is disabled.

SRA[2] – Channel A Transmitter Ready (TxRDYA)
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, e.g., characters loaded into the THR while the transmitter is disabled will not be transmitted.

SRA[1] – Channel A FIFO Full (FFULLA)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

SRA[0] – Channel A Receiver Ready (RxRDYA)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift to the FIFO and reset when the CPU reads the RHR, if after this read there are not more characters still in the FIFO.

SRB – Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

OPCR – Output Port Configuration Register

OPCR[7] – OP7 Output Select
This bit programs the OP7 output to provide one of the following:
0 The complement of OPR[7].
1 The Channel B transmitter interrupt output which is the complement of TxRDYB. When in this mode OP7 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[6] – OP6 Output Select
This bit programs the OP6 output to provide one of the following:
0 The complement of OPR[6].
1 The Channel A transmitter interrupt output which is the complement of TxRDYA. When in this mode OP6 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[5] – OP5 Output Select
This bit programs the OP5 output to provide one of the following:
0 The complement of OPR[5].
1 The Channel B transmitter interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[4] – OP4 Output Select
This field programs the OP4 output to provide one of the following:
0 The complement of OPR[4].
1 The Channel A receiver interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[3:2] – OP3 Output Select
This bit programs the OP3 output to provide one of the following:
00 The complement of OPR[3].
01 The counter/timer output, in which case OP3 acts as an open-drain output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
10 The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
11 The 1X clock for the Channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

OPCR[1:0] – OP2 Output Select
This field programs the OP2 output to provide one of the following:
00 The complement of OPR[2].
01 The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
10 The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
11 The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects one of two sets of baud rates to be generated by the BRG:

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05K, 1.2K, 2.4K, 4.8K, 7.2K, 9.6K, and 38.4K baud.

Set 2: 75, 110, 134.5, 150, 300, 600, 1.2K, 1.8K, 2.0K, 2.4K, 4.8K, 9.6K, and 19.2K baud.

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table 4.

Table 4. Bit Rate Generator Characteristics Crystal or Clock = 3.6864MHz

NORMAL RATE (BAUD)	ACTUAL 16X CLOCK (kHz)	ERROR (%)
50	0.8	0
75	1.2	0
110	1.759	-0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	-0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2K	307.2	0
38.4K	614.4	0

NOTE:
Duty cycle of 16X clock is 50% ± 1%.

ACR[6:4] – Counter/Timer Mode And Clock Source Select
This field selects the operating mode of the counter/timer and its clock source as shown in Table 5.

Table 5. ACR 6:4 Field Definition

ACR 6:4	MODE	CLOCK SOURCE
000	Counter	External (IP2)
001	Counter	TxCA – 1X clock of Channel A transmitter
010	Counter	TxCB – 1X clock of Channel B transmitter
011	Counter	Crystal or external clock (X1/CLK) divided by 16
100	Timer	External (IP2)
101	Timer	External (IP2) divided by 16
110	Timer	Crystal or external clock (X1/CLK)
111	Timer	Crystal or external clock (X1/CLK) divided by 16

ACR[3:0] – IP3, IP2, IP1, IP0 Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7:4] – IP3, IP2, IP1, IP0 Change-of-State
These bits are set when a change-of-state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – IP3, IP2, IP1, IP0 Change-of-State
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR – the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to 00_{16} when the DUART is reset.

ISR[7] – Input Port Change Status
This bit is a '1' when a change-of-state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

ISR[6] – Channel B Change In Break
This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel B 'reset break change interrupt' command.

ISR[5] – Channel B Receiver Ready or FIFO Full
The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that a character has been received in Channel B and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel B FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

ISR[4] – Channel B Transmitter Ready
This bit is a duplicate of TxRDYB (SRB[2]).

ISR[3] – Counter Ready.
In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

ISR[2] – Channel A Change In Break
This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

ISR[1] – Channel A Receiver Ready Or FIFO Full
The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that a character has been received in Channel A and is waiting in the FIFO to be

read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel A FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the ISR[0] and IMR waiting character is loaded into the FIFO.

ISR[0] – Channel A Transmitter Ready
This bit is a duplicate of TxRDYA (SRA[2]).

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3-OP7 or the reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is H'0002'. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. The waveform so generated is often used for a data clock. The formula for calculating the divisor n to load to the CTUR and CTLR for a particular 1X data clock is shown below:

$$n = \frac{C/T \text{ clock Frequency}}{2 \cdot 16 \cdot \text{Baud rate desired}}$$

Often this division will result in a non-integer number; 26.03, for example. One can only program integer numbers in a digital divider. Therefore, 26 would be chosen. This gives a baud rate error of 0.03/26.3 which is .114%; well within the ability asynchronous mode of operation.

If the value in CTUR and CTLR is changed, the current half-period will not be affected, but subsequent half periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read at address A3-A0 = 1110). After this, while in timer mode, the C/T will run continuously. Receipt of a start counter command (read with A3-A0 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3-A0 = H'F'). The command however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter commands. If new values have not been loaded, the previous count values are preserved and used for the next count cycle

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

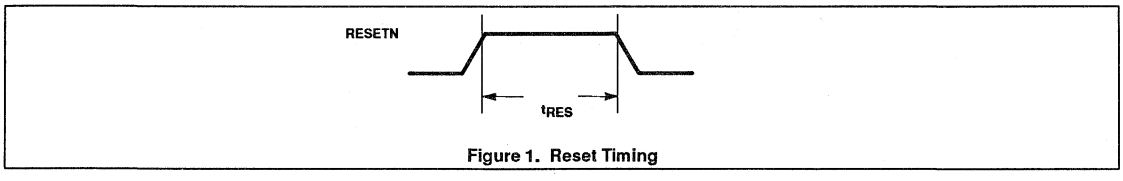


Figure 1. Reset Timing

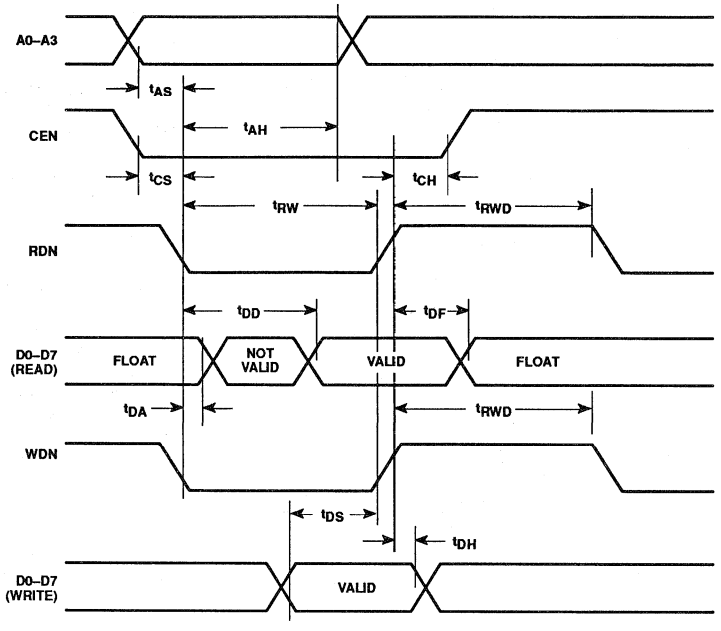
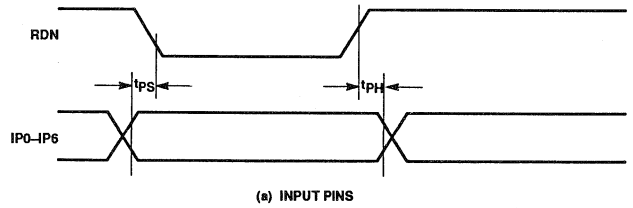
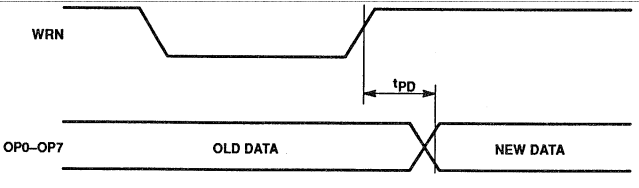


Figure 2. Bus Timing

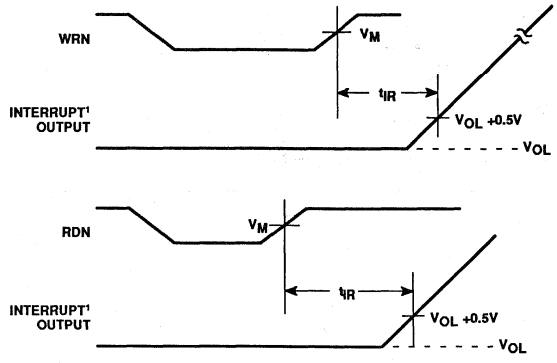


(a) INPUT PINS



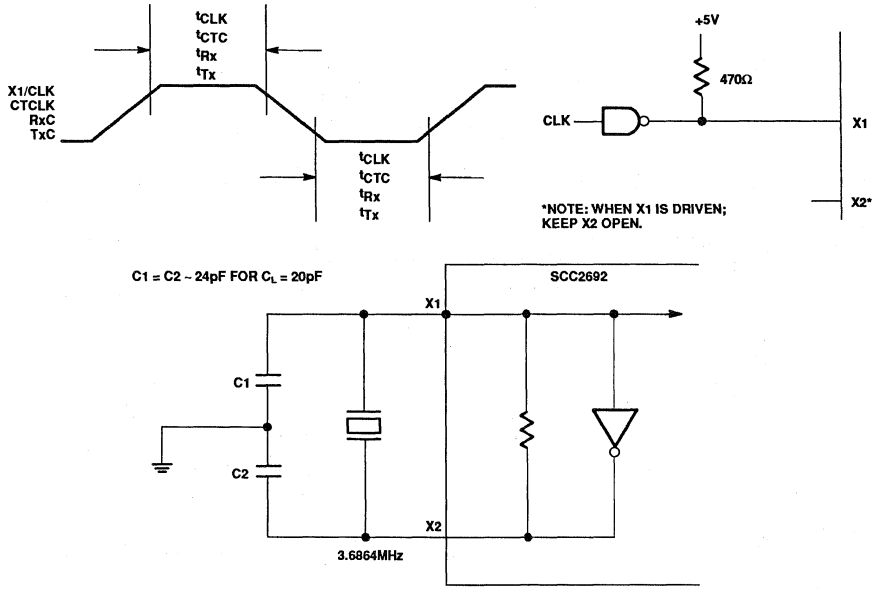
(b) OUTPUT PINS

Figure 3. Port Timing



NOTES:
1. INTRN or OP3-OP7 when used as interrupt outputs.
2. The test for open-drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from the midpoint of the switching signal, V_M, to a point 0.5V above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 4. Interrupt Timing



TYPICAL CRYSTAL SPECIFICATION

FREQUENCY	2–4 MHz
LOAD CAPACITANCE (C_L)	12–32 pF
TYPE OF OPERATION	PARALLEL RESONANT, FUNDAMENTAL MODE

Figure 5. Clock Timing

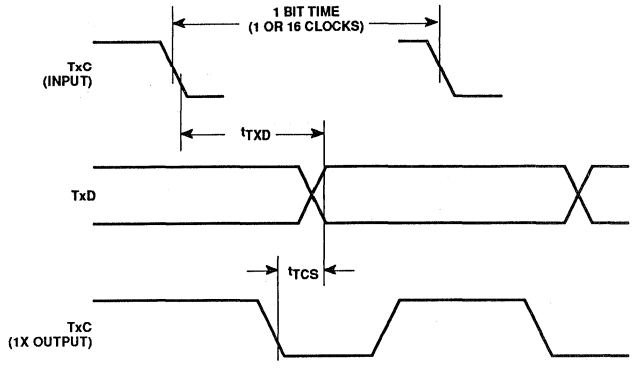


Figure 6. Transmitter External Clocks

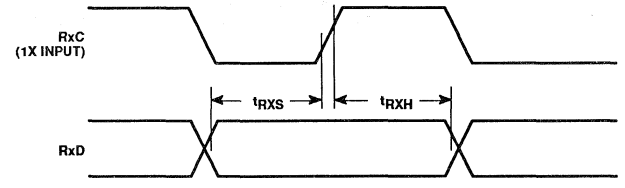
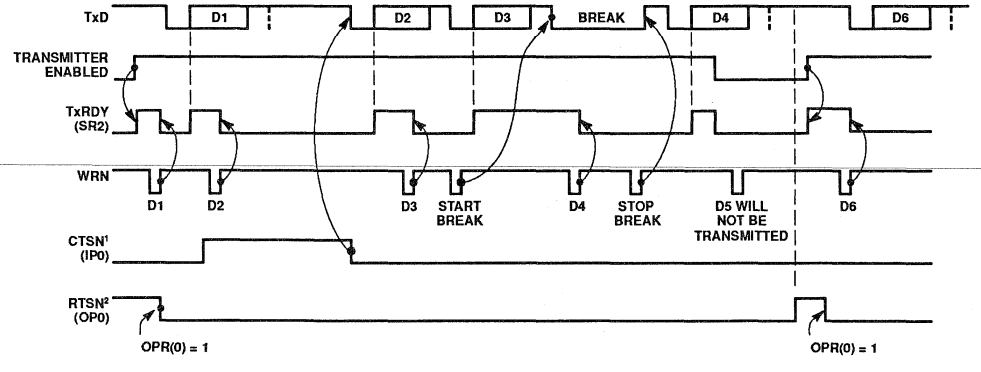
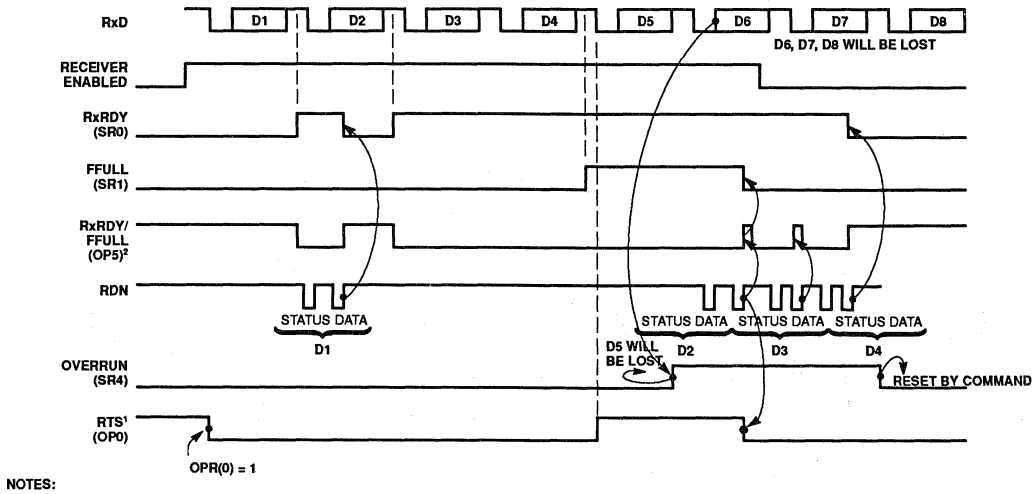


Figure 7. Receiver External Clock



NOTES:
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

Figure 8. Transmitter Timing



NOTES:
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) = 1 and MR(6) = 0.

Figure 9. Receiver Timing

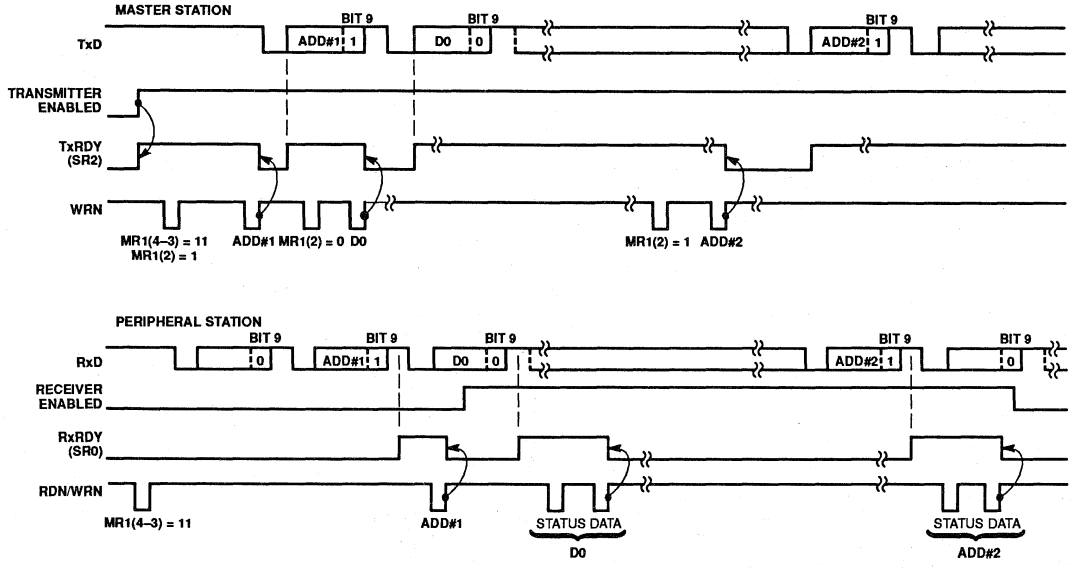


Figure 10. Wake-Up Mode

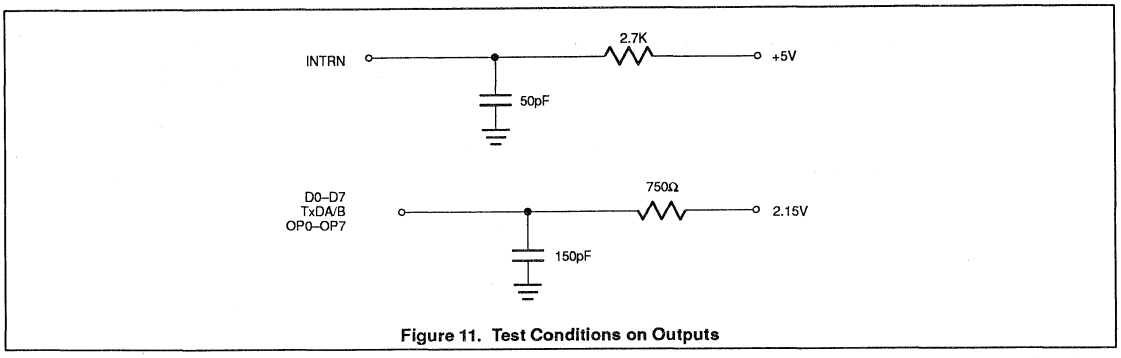


Figure 11. Test Conditions on Outputs

Output Port Notes

The output ports are controlled from four places: the OPCR register, the OPR register, the MR registers and the command register. The OPCR register controls the source of the data for the output ports OP2 through OP7. The data source for output ports OP0 and OP1 is controlled by the MR and CR registers. When the OPR is the source of the data for the output ports, the data at the ports is inverted from that in the OPR register. The content of the OPR register is controlled by the "Set Output Port Bits Command" and the "Reset Output Bits Command". These commands are at E and F, respectively. When these commands are used, action takes place only at the bit locations where ones exist. For example, a one in bit location 5 of the data word used with the "Set Output Port Bits" command will result in OPR5 being set to one. The OP5 would then be set to zero (V_{SS}). Similarly, a one in bit position 5 of the data word associated with the "Reset Output Ports Bits" command would set OPR5 to zero and, hence, the pin OP5 to a one (V_{DD}).

The CTS, RTS, CTS Enable Tx signals

CTS (Clear To Send) is usually meant to be a signal to the transmitter meaning that it may transmit data to the receiver. The CTS input is on pin IP0 for TxA and on IP1 for TxB. The CTS signal is active low; thus, it is called CTSAN for TxA and CTSBN for TxB.

RTS is usually meant to be a signal from the receiver indicating that the receiver is ready to receive data. It is also active low and is, thus, called RTSAN for RxA and RTSBN for RxB. RTSAN is on pin OP0 and RTSBN is on OP1. A receiver's RTS output will usually be connected to the CTS input of the associated transmitter. Therefore, one could say that RTS and CTS are different ends of the same wire!

MR2(4) is the bit that allows the transmitter to be controlled by the CTS pin (IP0 or IP1). When this bit is set to one AND the CTS input is driven high, the transmitter will stop sending data at the end of the present character being serialized. It is usually the RTS output of the receiver that will be connected to the transmitter's CTS input. The receiver will set RTS high when the receiver FIFO is full AND the start bit of the fourth character is sensed. Transmission then stops with four valid characters in the receiver. When MR2(4) is set to one, CTSN must be at zero for the transmitter to operate. If MR2(4) is set to zero, the IP pin will have no effect on the operation of the transmitter.

MR1(7) is the bit that allows the receiver to control OP0. When OP0 (or OP1) is controlled by the receiver, the meaning of that pin will be RTS. However, a point of confusion arises in that OP0 (or OP1) may also be controlled by the transmitter. When the transmitter is controlling this pin, its meaning is not RTS at all. It is, rather, that the transmitter has finished sending its last data byte. Programming the OP0 or OP1 pin to be controlled by the receiver and the transmitter at the same time is allowed, but would usually be incompatible.

RTS can also be controlled by the commands 1000 and 1001 in the command register. RTS is expressed at the OP0 or OP1 pin which is still an output port. Therefore, the state of OP0 or OP1 should be set low (either by commands of the CR register or by writing to the Set Output Ports Register) for the receiver to generate the proper RTS signal. The logic at the output is basically a NAND of the OPR register and the RTS signal as generated by the receiver. When the RTS flow control is selected via the MR(7) bit state of the OPR register is not changed. Terminating the use of "Flow Control" (via the MR registers) will return the OP0 or OP1 pins to the control of the OPR register.

Transmitter Disable Note

The sequence of instructions enable transmitter — load transmit holding register — disable transmitter will result in nothing being sent if the time between the end of loading the transmit holding register and the disable command is less that 3/16 bit time in the 16x mode or one bit time in the 1x mode. Also, if the transmitter, while in the enabled state and underrun condition, is immediately disabled after a single character is loaded to the transmit holding register, that character will not be sent.

In general, when it is desired to disable the transmitter before the last character is sent AND the TxEMT bit is set in the status register (TxEMT is always set if the transmitter has underrun or has just been enabled), be sure the TxRDY bit is active immediately before issuing the transmitter disable instruction. TxRDY sets at the end of the "start bit" time. It is during the start bit that the data in the transmit holding register is transferred to the transmit shift register.

Table 6. Baud Rate

	Normal BRG		BRG Test	
CSR[7:4]	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0000	50	75	4,800	7,200
0001	110	110	880	880
0010	134.5	38.4K	1,076	38.4K
0011	200	150	19.2K	14.4K
0100	300	300	28.8K	28.8K
0101	600	600	57.6K	57.6K
0110	1,200	1,200	115.2K	115.2K
0111	1,050	2,000	1,050	2,000
1000	2,400	2,400	57.6K	57.6K
1001	4,800	4,800	4,800	4,800
1010	7,200	1,800	57.6K	14.4K
1011	9,600	9,600	9,600	9,600
1100	38.4K	19.2K	38.4K	19.2K
1101	Timer	Timer	Timer	Timer
1110	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X
1111	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X

NOTE:
Each read on address H'2' will toggle the baud rate test mode. When in the BRG test mode, the baud rates change as shown to the left. This change affects all receivers and transmitters on the DUART. Also, the RTSN outputs (OP[0] and OP[1]) become the transmitter 1x clock.

The test mode at address H'A' changes all transmitters and receivers to the 1x mode and connects the output ports to some internal nodes.

Dual universal asynchronous receiver/transmitter (DUART)

SC26C92

DESCRIPTION

The SC26C92 is a pin and function replacement for the SCC2692 with added features and deeper FIFOs. Its configuration on power up is that of the 2692. Its differences from the 2692 are: 8 character receiver, 8 character transmit FIFOs, receiver watch dog timer, mode register 0 is added, extended baud rate and overall faster speeds, programmable receiver and transmitter interrupts. (The SCC2692 is not being discontinued.)

The Signetics SC26C92 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip CMOS-LSI communications device that provides two full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver and transmitter is buffered by eight character FIFOs to minimize the potential of receiver overrun, transmitter underrun and to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote transmitter when the receiver buffer is full.

Also provided on the SC26C92 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

The SC26C92 is available in two package versions: 40-pin 0.6" wide DIP and a 44-pin PLCC.

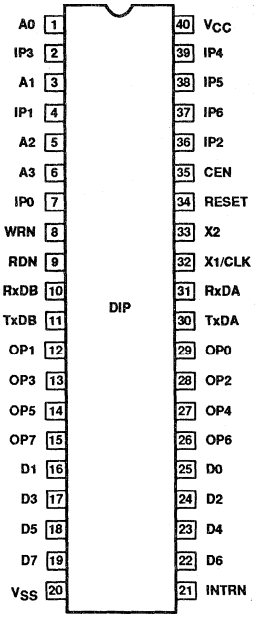
FEATURES

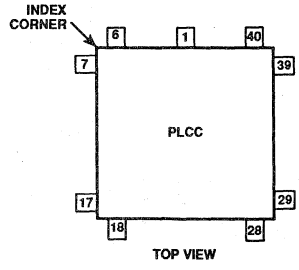
- Dual full-duplex independent asynchronous receiver/transmitters
- 8 character FIFOs for each receiver and transmitter
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4k baud
  - Other baud rates to 230.4k baud at 16X
  - Programmable user-defined rates derived from a programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
  - Each FIFO can be programmed for four different interrupt levels
  - Watch dog timer for each receiver
- Maximum data transfer rates: 1X – 1Mb/sec, 16X – 1Mb/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Power down mode
- Receiver timeout mode
- Single +5V power supply

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±10%, T_A = 0 to +70°C
40-Pin Plastic DIP	SC26C92C1N
44-Pin Plastic LCC	SC26C92C1A

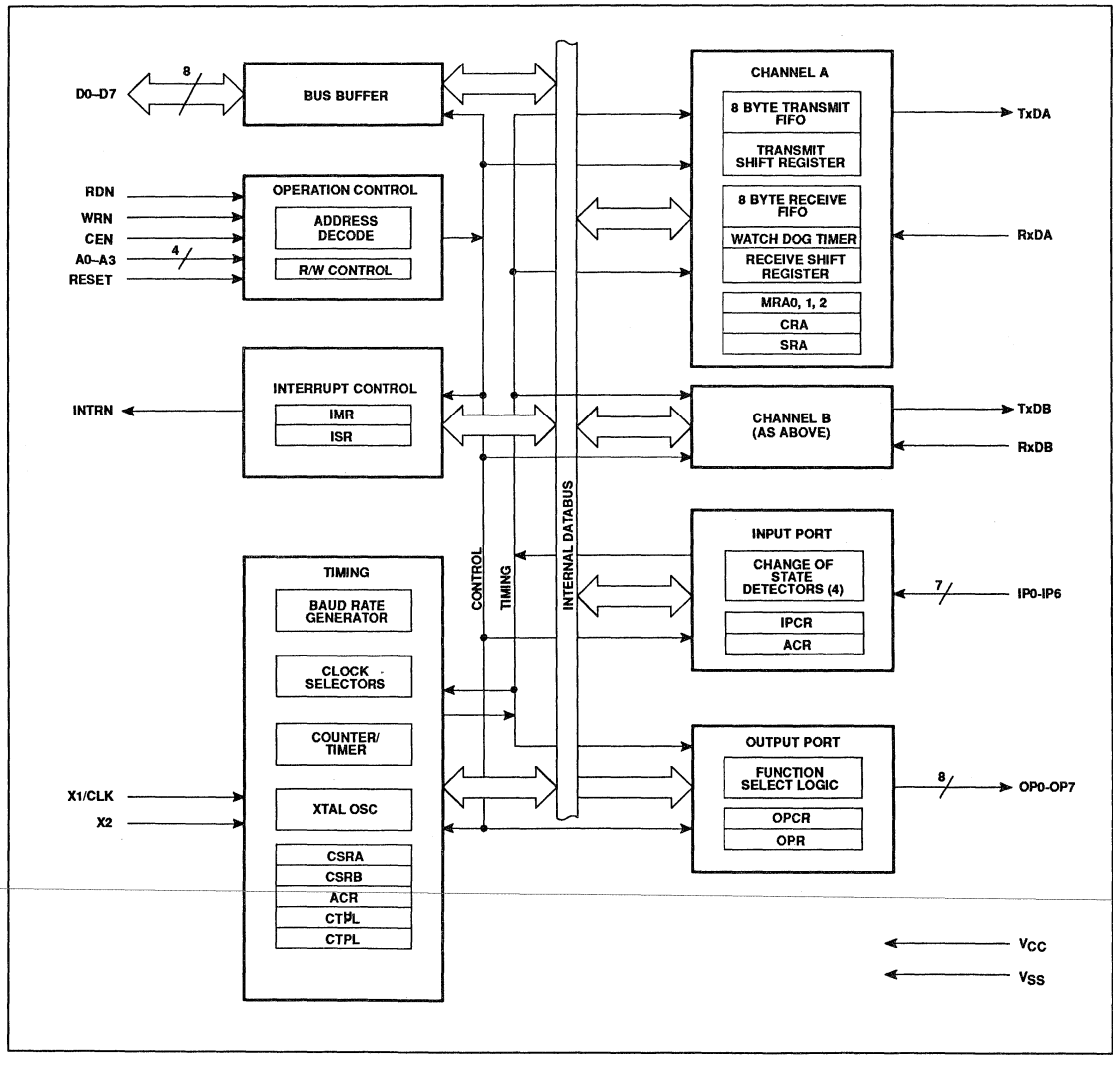
PIN CONFIGURATIONS





PIN/FUNCTION		PIN/FUNCTION	
1	NC	23	NC
2	A0	24	INTRN
3	IP3	25	D6
4	A1	26	D4
5	IP1	27	D2
6	A2	28	D0
7	A3	29	OP6
8	IP0	30	OP4
9	WRN	31	OP2
10	RDN	32	OP0
11	RXDB	33	TXDA
12	NC	34	NC
13	TXDB	35	RXDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CEN
18	D1	40	IP2
19	D3	41	IP6
20	D5	42	IP5
21	D7	43	IP4
22	VSS	44	VCC

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PKG	PIN	NAME AND FUNCTION
	40,44	TYPE	
D0-D7	X	I/O	**Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	X	I	**Chip Enable:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the WRN, RDN and A0-A3 inputs. When High, places the D0-D7 lines in the 3-State condition.
WRN	X	I	**Write Strobe:** When Low and CEN is also Low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	X	I	**Read Strobe:** When Low and CEN is also Low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0-A3	X	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	X	I	**Reset:** A High level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0-OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state.
INTRN	X	O	**Interrupt Request:** Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	X	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5).
X2	X	I	**Crystal 2:** Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5). If X1/CLK is driven from an external source, this pin must be left open.
RxDA	X	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	X	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	X	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
TxDB	X	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is High, 'space' is Low.
OP0	X	O	**Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	X	O	**Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	X	O	**Output 2:** General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	X	O	**Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	X	O	**Output 4:** General purpose output or Channel A open-drain, active-Low, RxA interrupt ISR[1] output.
OP5	X	O	**Output 5:** General purpose output or Channel B open-drain, active-Low, RxB interrupt ISR[5] output.
OP6	X	O	**Output 6:** General purpose output or Channel A open-drain, active-Low, TxA interrupt ISR[0] output.
OP7	X	O	**Output 7:** General purpose output, or Channel B open-drain, active-Low, TxB interrupt ISR[4] output.
IP0	X	I	**Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	X	I	**Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	X	I	**Input 2:** General purpose input or counter/timer external clock input.
IP3	X	I	**Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	X	I	**Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	X	I	**Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6	X	I	**Input 6:** General purpose input or Channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.

PIN DESCRIPTION (Continued)

SYMBOL	PKG	PIN	NAME AND FUNCTION
	40,44	TYPE	
V_{CC}	X	I	**Power Supply:** +5V supply input.
GND	X	I	**Ground**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	Note 4	°C
T_{STG}	Storage temperature range	-65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	-0.5 to +7.0	V
V_S	Voltage from any pin to GND[3]	-0.5 to V_{CC} +0.5	V
P_D	Power dissipation[5]	750	mW

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.
5. Maximum power dissipation of the chip when outputs are loaded externally. For operating current, see DC Electrical Characteristics.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage (except X1/CLK)[6]		2.3			V
V_{IH}	Input high voltage (X1/CLK)		0.8 V_{CC}			V
V_{OL}	Output low voltage	I_{OL} = 2.4mA			0.4	V
V_{OH}	Output high voltage (except OD outputs)[4]	I_{OH} = -400µA	V_{CC} -0.5			V
I_{IX1PD}	X1/CLK input current - power down	V_{IN} = 0 to V_{CC}	-1		+1	µA
I_{ILX1}	X1/CLK input low current - operating	V_{IN} = 0	-100		0	µA
I_{IHX1}	X1/CLK input high current - operating	V_{IN} = V_{CC}	0		100	µA
I_I	Input leakage current:					
	All except input port pins	V_{IN} = 0 to V_{CC}	-1		+1	µA
	Input port pins	V_{IN} = 0 to V_{CC}	-10		+10	µA
I_{OZH}	Output off current high, 3-State data bus	V_{IN} = V_{CC}			1	µA
I_{OZL}	Output off current low, 3-State data bus	V_{IN} = 0V	–1			µA
I_{ODL}	Open-drain output low current in off-state	V_{IN} = 0	–1			µA
I_{ODH}	Open-drain output high current in off-state	V_{IN} = V_{CC}			1	µA
I_{CC}	Power supply current[5]					
	Operating mode	CMOS input levels			25	mA
	Power down mode[7]	CMOS input levels			5.0	mA

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 3.0V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7KΩ to V_{CC}.
5. All outputs are disconnected. Inputs are switching between CMOS levels of V_{CC} -0.2V and V_{SS} + 0.2V.
6. WRN may reach 2.58V in moist environments.
7. See UART application note for power down currents of 5µA or less.

AC CHARACTERISTICS[1, 2, 4]

SYMBOL	PARAMETER	LIMITS Min	Typ[3]	Max	UNIT
Reset Timing (See Figure 1)					
t_{RES}	RESET pulse width	200			ns
Bus Timing[5] (See Figure 2)					
t_{AS}	A0-A3 setup time to RDN, WRN Low	10			ns
t_{AH}	A0-A3 hold time from RDN, WRN Low	45			ns
t_{CS}	CEN setup time to RDN, WRN Low	0			ns
t_{CH}	CEN hold time from RDN, WRN High	0			ns
t_{RW}	WRN, RDN pulse width	110			ns
t_{DD}	Data valid after RDN Low			90	ns
t_{DA}	RDN Low to data bus active[7]	0			ns
t_{DF}	Data bus floating after RDN High			30	ns
t_{DI}	RDN High to data bus invalid[7]	0			ns
t_{DS}	Data setup time before WRN High	75			ns
t_{DH}	Data hold time after WRN High	8			ns
t_{RWD}	High time between reads and/or writes[5, 6]	55			ns
Port Timing[5] (See Figure 3)					
t_{PS}	Port input setup time before RDN Low	0			ns
t_{PH}	Port input hold time after RDN High	0			ns
t_{PD}	OP_n output valid from WRN High			110	ns
Interrupt Timing (See Figure 4)					
t_{IR}	INTRN (or OP3-OP7 when used as interrupts) negated from:				
	Read RxFIFO (RxRDY/FFULL interrupt)			100	ns
	Write TxFIFO (TxRDY interrupt)			100	ns
	Reset command (break change interrupt)			100	ns
	Stop C/T command (counter interrupt)			100	ns
	Read IPCR (input port change interrupt)			100	ns
	Write IMR (clear of interrupt mask bit)			100	ns
Clock Timing (See Figure 5)					
t_{CLK}	X1/CLK High or Low time	80			ns
f_{CLK}	X1/CLK frequency	2	3.6864	4	MHz
t_{CTC}	CTCLK (IP2) High or Low time	55			ns
f_{CTC}	CTCLK (IP2) frequency[8]	0		8	MHz
t_{RX}	RxC High or Low time (16X)	30			ns
f_{RX}	RxC frequency (16X)[8]	0		16	MHz
	(1X)[8, 9]	0		1	MHz
t_{TX}	TxC High or Low time (16X)	30			ns
f_{TX}	TxC frequency (16X)[8]	0		16	MHz
	(1X)[8, 9]	0		1	MHz
Transmitter Timing (See Figure 6)					
t_{TXD}	TxD output delay from TxC Low (TxC input pin)			120	ns
t_{TCS}	Output delay from TxC Low to TxD data output (TxC 1x output pin)	–30		30	ns
Receiver Timing (See Figure 7)					
t_{RXS}	RxD data setup time to RxC High	100			ns
t_{RXH}	RxD data hold time from RxC High	100			ns

NOTES:

1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 3.0V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7KΩ to V_{CC}.
5. Timing is illustrated and referenced to the WRN and RDN inputs. Also, CEN may be the 'strobing' input. CEN and RDN (also CEN and WRN) are ORed internally. The signal asserted last initiates the cycle and the signal negated first terminates the cycle.
6. If CEN is used as the 'strobing' input, the parameter defines the minimum High times between one CEN and the next. The RDN signal must be negated for t_{RWD} to guarantee that any status register changes are valid.
7. Guaranteed by characterization of sample units.
8. Minimum frequencies are not tested but are guaranteed by design.
9. Clocks for 1X mode should be symetrical.

Block Diagram

The SC26C92 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the Block Diagram.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer.

Interrupt Control

A single active-Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR). The IMR can be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions.

Outputs OP3-OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer.

When OP3 to OP7 are programmed as interrupts, their output buffers are changed to the open drain active low configuration.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART.

If an external is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 5.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. Programming bit 0 of MR0 to a "1" gives additional baud rates of 57.6kB, 115.2kB and 230.4kB. These will be in the 16X mode. A 3.6864MHz crystal or external clock must be used to get the standard baud rate. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

The Counter/Timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

Communications Channels A and B

Each communications channel of the SC26C92 comprises a full-duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU via the receive FIFO. Three status bits (Break, Framing and Parity Errors) are also FIFOed with each data character.

Input Port

The inputs to this unlatched 7-bit port can be read by the CPU by performing a read operation at address H'D'. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always read as a logic 1. The pins of this port can also serve as auxiliary inputs to certain portions fo the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs, lasting longer than 25 - 50µs, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU.

The input port pulse detection circuitry uses a 38.4KHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25µs (this assumes that the clock input is 3.6864MHz). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs "coincident with the first sample pulse". The 50µs time refers to the situation in which the change-of-state is "just missed" and the first change-of-state is not detected until 25µs later.

Output Port

The output port pins may be controlled by the OPR, OPCR, MR and CR registers. Via appropriate programming they may be just another parallel port to external circuits, or they may represent many internal conditions of the UART. When this 8-bit port is used as a general purpose output port, the output port pins drive a state which is the complement of the Output Port Register (OPR). The OPR register is set and reset by writing to the SOPR and ROPR addresses. (See the description of the SOPR and ROPR registers). The output pins will drive the inverse data polarity of the OPR registers. The OPCR register conditions these output to be controlled by the OPR or by other signals in the chip.

OPERATION

Transmitter

The SC26C92 is conditioned to transmit data when the transmitter is enabled through the command register. The SC26C92 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be

programmed to generate an interrupt request at OP6 or OP7 and INTRN. When the transmitter is initially enabled the TxRDY and TxEMPTY bits will be set in the status register. When a character is loaded to the transmit FIFO the TxEMPTY bit will be reset. The TxEMPTY will not set until: 1) the transmit FIFO is empty and the transmit shift register has finished transmitting the stop bit of the last character written to the transmit FIFO, or 2) the transmitter is disabled and then re-enabled. The TxRDY bit is set whenever the transmitter is enabled and the TxFIFO is not full. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. Characters cannot be loaded into the TxFIFO while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the TxFIFO, the TxD output remains High and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the TxFIFO.

If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous Low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS option is enabled (MR2[4] = 1), the CTS input at IP0 or IP1 must be Low in order for the character to be transmitted. The transmitter will check the state of the CTS input at the beginning of each character transmitted. If it is found to be High, the transmitter will delay the transmission of any following characters until the CTS has returned to the low state. CTS going high during the serialization of a character will not affect that character.

The transmitter can also control the RTSN outputs, OP0 or OP1 via MR2[5]. When this mode of operation is set, the meaning of the OP0 or OP1 signals will usually be 'end of message'. See description of the MR2[5] bit for more detail.

Receiver

The SC26C92 is conditioned to receive data when enabled through the command register. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive FIFO and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than 8 bits, the most significant unused bits in the RxFIFO are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RxFIFO and the received break bit in the SR is set to 1. The RxD input must return to a High condition for at least one-half bit time before a search for the next start bit begins.

The RxFIFO consists of a First-In-First-Out (FIFO) stack with a capacity of eight characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all eight stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RxFIFO outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RxFIFO is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4] will be set-upon receipt of the start bit of the new (overrunning) character).

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

A 'watchdog timer' is associated with each receiver. Its interrupt is enabled by MR0[7]. The purpose of this timer is to alert the control processor that characters are in the RxFIFO which have not been read and/or the data stream has stopped. This situation may occur at the end of a transmission when the last few characters received are not sufficient to cause an interrupt.

This counter times out after 64 bit times. It is reset each time a character is transferred from the receiver shift register to the RxFIFO or a read of the RxFIFO is executed.

Receiver Timeout Mode

In addition to the watch dog timer described in the receiver section, the counter/timer may be used for a similar function. Its programmability, of course, allows much greater precision of time out intervals.

The timeout mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RxFIFO, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the RxFIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU may not know there is data left in the FIFO. The CTU and CTL value would be programmed for just over one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all of the characters from the FIFO, but the last character received has started the count. If there is no new data during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

This mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the timeout mode for that channel. Writing a 'Cx' to CRA or CRB will disable the timeout mode. The timeout mode should only be used by one channel at once, since it uses the C/T. CTU and CTL must be loaded with a value greater than the normal receive character period. The timeout mode disables the regular START/STOP Counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RxFIFO, the C/T is stopped after 1 C/T clock, reloaded with the value in CTU and CTL and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Receiving a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Timeout Mode On' command, CRx = 'Ax', will also clear the counter ready bit and stop the counter until the next character is received.

Multidrop Mode

The DUART is equipped with a wake up mode for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wakeup' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the TxFIFO.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RxFIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RxFIFO. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems.

For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Each channel has 3 mode registers (MR0, 1, 2) which control the basic configuration of the channel. Access to these registers is controlled by independent MR address pointers. These pointers are set to 0 or 1 by MR control commands in the command register "Miscellaneous Commands". Each time the MR registers are accessed the MR pointer increments, stopping at MR2. It remains pointing to MR2 until set to 0 or 1 via the miscellaneous commands of the command register. The pointer is set to 1 on reset for compatibility with previous Signetics UART software.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'0A' should never be read during normal operation since they are reserved for internal diagnostics.

Table 1. SC26C92 Register Addressing

A3	A2	A1	A0	READ (RDN = 0)	WRITE (WRN = 0)
0	0	0	0	Mode Register A (MR0A, MR1A, MR2A)	Mode Register A (MR0A, MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	Reserved	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RxFIFOA)	Tx Holding Register A (TxFIFOA)
0	1	0	0	Input Port Change Register (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Preset Register (CTPU)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Preset Register (CTPL)
1	0	0	0	Mode Register B (MR0B, MR1B, MR2B)	Mode Register B (MR0B, MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	Reserved	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RxFIFOB)	Tx Holding Register B (TxFIFOB)
1	1	0	0	Reserved	Reserved
1	1	0	1	Input Port (IPR)	Output Port Conf. Register (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command (SOP12)
1	1	1	1	Stop Counter Command	Reset Output Port Bits Command (ROP12)

NOTE:
The three MR Registers are accessed via the MR Pointer and Commands 1xh and Bxh. (Where "x" represents receiver and transmitter enable/disable control)

The following named registers are the same for Channels A and B.			
Mode Register	MRnA	MRnB	R/W
Status Register	SRA	SRB	R only
Clock Select	CSRA	CSRB	W only
Command Register	CRA	CRB	W only
Receiver FIFO	RxFIFOA	RxFIFOB	R only
Transmitter FIFO	TxFIFOA	TxFIFOB	W only

These registers control the functions which service both Channels.		
Input Port Change Register	IPCR	R
Auxiliary Control Register	ACR	W
Interrupt Status Register	ISR	R
Interrupt Mask Register	IMR	W
Counter Timer Upper Value	CTU	R
Counter Timer Lower Value	CTL	R
Counter Timer Preset Upper	CTPU	W
Counter Timer Preset Lower	CTPL	W
Input Port Register	IPR	R
Output Configuration Register	OPCR	W
Set Output Port Bits	SOPR	W
Reset Output Port Bits	ROPR	W

Table 2. Register Bit Formats

	BIT 7	BIT 6	BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MR0A MR0B	**Rx WATCH DOG**	**RxINT BIT 2**	**TxINT (1:0)**	**DON'T CARE**	**BAUD RATE EXTENDED II**	**TEST 2**	**BAUD RATE EXTENDED 1**
MR0B[3:0] are reserved	0 = Disable 1 = Enable			Set to 0	0 = Normal 1 = Extend II	Set to 0	0 = Normal 1 = Extend

	BIT 7	BIT 6	BIT 5	BIT 4 BIT 3	BIT 2	BIT 1 BIT 0
	Rx CONTROLS RTS	**Rx INT BIT 1**	**ERROR MODE**	**PARITY MODE**	**PARITY TYPE**	**BITS PER CHARACTER**
MR1A MR1B	0 = No 1 = Yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multidrop Mode	0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8

Table 2. Register Bit Formats (Continued)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	CHANNEL MODE		Tx CONTROLS RTS	CTS ENABLE Tx	STOP BIT LENGTH*			
MR2A MR2B	00 = Normal 01 = Auto-Echo 10 = Local loop 11 = Remote loop		0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

NOTE:
*Add 0.5 to values shown for 0 – 7 if channel is programmed for 5 bits/char.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RECEIVER CLOCK SELECT				TRANSMITTER CLOCK SELECT			
CSRA CSRB	See Text				See Text			

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MISCELLANEOUS COMMANDS*				DISABLE Tx	ENABLE Tx	DISABLE Rx	ENABLE Rx
CRA CRB	See Text				0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
*Access to the uppoer four bits of the Command Register should be separated in time by three (3) X1 clock edges.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RECEIVED BREAK*	FRAMING ERROR*	PARITY ERROR*	OVERRUN ERROR	TxEMT	TxRDY	FFULL	RxRDY
SRA SRB	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
* These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a "reset error status" command. In character mode they are discarded when the corresponding data character is read from the FIFO.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3 BIT 2	BIT 1 BIT 0
	OP7	OP6	OP5	OP4	OP3	OP2
OPCR	0 = OPR[7] 1 = TxRDYB	0 = OPR[6] 1 = TxRDYA	0 = OPR[5] 1 = RxRDY/ FFULLB	0 = OPR[4] 1 = RxRDY/ FFULLA	00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB(1X) 11 = RxCB(1X)	00 = OPR[2] 01 = TxCA(16X) 10 = TxCA(1X) 11 = RxCA(1X)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SOPR	See Note	See Note	See Note	See Note	See Note	See Note	See Note	See Note

NOTE:
0 = No Change; 1 = Set

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ROPR	See Note	See Note	See Note	See Note	See Note	See Note	See Note	See Note

NOTE:
0 = No Change; 1 = Reset

	BIT 7	BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	BRG SET SELECT	COUNTER/TIMER MODE AND SOURCE	DELTA IP 3 INT	DELTA IP 2 INT	DELTA IP 1 INT	DELTA IP 0 INT
ACR	0 = set 1 1 = set 2	See Table 4	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

Table 2. Register Bit Formats (Continued)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	DELTA IP 3	DELTA IP 2	DELTA IP 1	DELTA IP 0	IP 3	IP 2	IP 1	IP 0
IPCR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	INPUT PORT CHANGE	DELTA BREAK B	RxRDY/ FFULLB	TxRDYB	COUNTER READY	DELTA BREAK A	RxRDY/ FFULLA	TxRDYA
ISR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IN. PORT CHANGE INT	DELTA BREAK B INT	RxRDY/ FFULLB INT	TxRDYB INT	COUNTER READY INT	DELTA BREAK A INT	RxRDY/ FFULLA INT	TxRDYA INT
IMR	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]
CTPU								

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]
CTPL								

REGISTER DESCRIPTIONS

Mode Registers

MR0 is accessed by setting the MR pointer to 0 via the command register command B.

MR0A

MR0[7] – This bit controls the receiver watch dog timer. 0 = disable, 1 = enable. When enabled, the watch dog timer will generate a receiver interrupt if the receiver FIFO has not been accessed within 64 bit times of the receiver 1X clock. This is used to alert the control processor that data is in the RxFIFO that has not been read. This situation may occur when the byte count of the last part of a message is not large enough to generate an interrupt.

MR0[6] – Bit 2 of receiver FIFO interrupt level. This bit along with Bit 6 of MR1 sets the fill level of the 8 byte FIFO that generates the receiver interrupt.

MR0[6]	MR1[6]	Interrupt Condition
0	0	1 or more bytes in FIFO (Rx RDY)
0	1	3 or more bytes in FIFO
1	0	6 or more bytes in FIFO
1	1	8 bytes in FIFO (Rx FULL)

MR0[5:4] – Tx interrupt fill level.

MR0[5]	MR0[4]	Interrupt Condition
0	0	8 bytes empty (Tx EMPTY)
0	1	4 or more bytes empty
1	0	6 or more bytes empty
1	1	1 or more bytes empty (Tx RDY)

MR0[3] – Not used. Should be set to 0.

MR0[2:0] – These bits are used to select one of the six baud rates (see Table 3).

000 Normal mode
001 Extended mode I
100 Extended mode II

Other combinations should not be used

Note: MR0[3:0] are not used in channel B and should be set to 0.

MR1A

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CR command 1. After reading or writing MR1A, the pointer will point to MR2A.

MR1A[7] – Channel A Receiver Request-to-Send Control (Flow Control)
This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR1A[7] = 1 causes RTSAN to be negated (OP0 is driven to a '1' [V_{CC}]) upon receipt of a valid start bit if the Channel A FIFO is full. This is the beginning of the reception of the ninth byte. If the FIFO is not read before the start of the tenth byte, an overrun condition will occur and the tenth byte will be lost. However, the bit in OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

MR1[6] – Bit 1 of the receiver interrupt control. See description under MR0[6].

MR1A[5] – Channel A Error Mode Select
This bit select the operating mode of the three FIFOed status bits (FE, PE, received

break) for Channel A. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

MR1A[4:3] – Channel A Parity Mode Select
If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data MR1A[4:3] = 11 selects Channel A to operate in the special multidrop mode described in the Operation section.

MR1A[2] – Channel A Parity Type Select
This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

MR1A[1:0] – Channel A Bits Per Character Select
This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2A – Channel A Mode Register 2

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

MR2A[7:6] – Channel A Mode Select
Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently.
MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The Channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop has been re-transmitted.

MR2A[5] – Channel A Transmitter Request-to-Send Control
This bit controls the deactivation of the RTSAN output (OP0) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0].
MR2A[5] = 1 caused OPR[0] to be reset automatically one bit time after the characters in the Channel A transmit shift register and in the TxFIFO, if any, are completely transmitted including the programmed number of stop bits, if the transmitter is not enabled. This feature can be used to automatically terminate the transmission of a message as follows:

1. Program auto-reset mode: MR2A[5] = 1.
2. Enable transmitter.
3. Asset RTSAN: OPR[0] = 1.
4. Send message.
5. Disable transmitter after the last character is loaded into the Channel A TxFIFO.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

NOTE: If the transmitter is idle at Step 5 (above), wait for TxRDY[SR(2)] to set before disabling the transmitter. The transmitter is idle whenever TxEMT and TxRDY bits are both set.

MR2A[4] – Channel A Clear-to-Send Control
If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IPO) each time it is ready to send a character. If IPO is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character..

MR2A[3:0] – Channel A Stop Bit Length Select
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1-9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1-1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a 'mark' condition at the center of the stop bit position (one bit time after the last

data bit, or after the parity bit if enabled is sampled).

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

MR0B – Channel B Mode Register 0

MR0B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR0 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR0B, the pointer will point to MR1B.

The bit definitions for this register are identical to MR0A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs. MR0B[3:0] are reserved.

MR1B – Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to MR1A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

MR2B – Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode register are identical to the bit definitions for MR2A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

CSRA – Channel A Clock Select Register

CSRA[7:4] – Channel A Receiver Clock Select
This field selects the baud rate clock for the Channel A transmitter. The field definition is shown in Table 3.

CSRA[3:0] – Channel A Transmitter Clock Select
This field selects the baud rate clock for the Channel A transmitter. The field definition is as shown in Table 3, except as follows:

CSRA[3:0]	ACR[7] = 0	ACR[7] = 1
1110	IP3-16X	IP3-16X
1111	IP3-1X	IP3-1X

The transmitter clock is always a 16X clock except for CSR[3:0] = 1111.

Table 3. Baud Rate

	MR0[0] = 0 (Normal Mode)		MR0[0] = 1 (Extended Mode I)		MR0[2] = 1 (Extended Mode II)	
CSRA[7:4]	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0000	50	75	50	450	4,800	7,200
0001	110	110	110	110	880	880
0010	134.5	134.5	134.5	230.4K	1,076	1,076
0011	200	150	200	900	19.2K	14.4K
0100	300	300	1800	1800	28.2K	38.6K
0101	600	600	3600	3600	57.6K	57.6K
0110	1,200	1,200	7200	7,200	115.2K	115.2
0111	1,050	2,000	1,050	2,000	1,050	2,000
1000	2,400	2,400	14.4K	14.4K	57.6K	57.6K
1001	4,800	4,800	28.8K	28.8K	4,800	4,800
1010	7,200	1,800	7,200	1,800	57.6K	14.4K
1011	9,600	9,600	57.6K	57.6K	9,600	9,600
1100	38.4K	19.2K	230.4K	115.2K	38.4K	19.2K
1101	Timer	Timer	Timer	Timer	Timer	Timer
1110	IP4-16X	IP4-16X	IP4-16X	IP4-16X	IP4-16X	IP4-16X
1111	IP4-1X	IP4-1X	IP4-1X	IP4-1X	IP4-1X	IP4-1X

NOTE: The receiver clock is always a 16X clock except for CSRA[7:4] = 1111.

CSRB – Channel B Clock Select Register

CSRB[7:4] – Channel B Receiver Clock Select
This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 3, except as follows:

CSRB[7:4]	ACR[7] = 0	ACR[7] = 1
1110	IP6-16X	IP6-16X
1111	IP6-1X	IP6-1X

The transmitter clock is always a 16X clock except for CSRB[7:4] = 1111.

CSRB[3:0] – Channel B Transmitter Clock Select
This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 3, except as follows:

CSRB[3:0]	ACR[7] = 0	ACR[7] = 1
1110	IP5-16X	IP5-16X
1111	IP5-1X	IP5-1X

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

CRA – Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

CRA[7:4] – Miscellaneous Commands
Execution of the commands in the upper four bits of this register must be separated by 3 X1 clock edges. Other reads or writes (including writes tot he lower four bits) may be inserted to achieve this separation.

CRA[7:4] – Command

0000 No command.
0001 Reset MR pointer. Causes the Channel A MR pointer to point to MR1.
0010 Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.
0011 Reset transmitter. Resets the Channel A transmitter as if a hardware reset had been applied.
0100 Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.
0101 Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.
0110 Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the TxFIFO, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.
0111 Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted.
1000 Assert RTSN. Causes the RTSN output to be asserted (Low).
1001 Negate RTSN. Causes the RTSN output to be negated (High).
1010 Set Timeout Mode On. The receiver in this channel will restart the C/T as each receive character is transferred from the shift register to the RxFIFO. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset. (See also Watchdog timer description in the receiver section.)
1011 Set MR pointer to '0'
1100 Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued to force a reset of the ISR(3) bit.
1101 Not used.
1110 Power Down Mode On. In this mode, the DUART oscillator is stopped and all functions requiring this clock are suspended. The execution of commands other than disable power down mode (1111) requires a X1/CLK. While in the power down mode, do not issue any commands to the CR except the disable power down mode command. The contents of all registers will be saved while in this mode. . It is recommended that the transmitter and receiver be disabled prior to placing the DUART into power down mode. This command is in CRA only.
1111 Disable Power Down Mode. This command restarts the oscillator. After invoking this command, wait for the oscillator to start up before writing further commands to the CR. This command is in CRA only. For maximum power reduction input pins should be at V_{SS} or V_{DD}.

CRA[3] – Disable Channel A Transmitter
This command terminates transmitter operation and reset the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the TxFIFO when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CRA[2] – Enable Channel A Transmitter
Enables operation of the Channel A transmitter. The TxRDY and TxEMT status bits will be asserted if the transmitter is idle.

CRA[1] – Disable Channel A Receiver
This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

CRA[0] – Enable Channel A Receiver
Enables operation of the Channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start-bit state.

CRB – Channel B Command Register

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, with the exception of comamnds "Ex" and "Fx" which are used for power downmode. These two commands are not used in CRB. All other control actions that apply to CRA also apply to CRB.

SRA – Channel A Status Register

SRA[7] – Channel A Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line returns to the marking state for at least one-half a bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the Channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

This bit is reset by command 4 (0100) written to the command register or by receiver reset.

SRA[6] – Channel A Framing Error
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SRA[5] – Channel A Parity Error
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

In the special multidrop mode the parity error bit stores the receive A/D (Address/Data) bit.

SRA[4] – Channel A Overrun Error
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost.

This bit is cleared by a 'reset error status' command.

SRA[3] – Channel A Transmitter Empty (TxEMTA)
This bit will be set when the Channel A transmitter underruns; i.e., both the Transmit Holding Register (TxFIFO) and the transmit shift register are empty. It is set after transmission of the last stop bit of a character if no character is in the TxFIFO awaiting transmission. It is reset when the TxFIFO is loaded by the CPU or when the transmitter is disabled or reset.

SRA[2] – Channel A Transmitter Ready (TxRDYA)
This bit, when set, indicates that the transmit FIFO is not full and ready to be loaded with another character. This bit is cleared when the transmit FIFO is loaded by the CPU and there are (after this load) no more empty locations in the FIFO. It is set when a character is transferred to the transmit shift register. TxRDYA is reset when the transmitter is disabled and is set when the transmitter is first enabled. Characters loaded to the TxFIFO while this bit is 0 will be lost. This bit has different meaning from ISR[0].

SRA[1] – Channel A FIFO Full (FFULLA)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all eight FIFO positions are occupied. It is reset when the CPU reads the receive FIFO. If a character is waiting in the receive shift register because the FIFO is full, FFULLA will not be reset when the CPU reads the receive FIFO. This bit has different meaning from ISR1 when MR1 6 is programmed to a '1'.

SRA[0] – Channel A Receiver Ready (RxRDYA)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the receive FIFO, only if (after this read) there are no more characters in the FIFO.

SRB – Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

OPCR – Output Port Configuration Register

OPCR[7] – OP7 Output Select
This bit programs the OP7 output to provide one of the following:
0 The complement of OPR[7].
1 The Channel B transmitter interrupt output which is the complement of ISR[4]. When in this mode OP7 acts as an open- drain output. Note that this output is not masked by the contents of the IMR.

OPCR[6] – OP6 Output Select
This bit programs the OP6 output to provide one of the following:
0 The complement of OPR[6].
1 The Channel A transmitter interrupt output which is the complement of ISR[0]. When in this mode OP6 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[5] – OP5 Output Select
This bit programs the OP5 output to provide one of the following:
0 The complement of OPR[5].
1 The Channel B receiver interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[4] – OP4 Output Select
This field programs the OP4 output to provide one of the following:
0 The complement of OPR[4].
1 The Channel A receiver interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[3:2] – OP3 Output Select
This bit programs the OP3 output to provide one of the following:
00 The complement of OPR[3].
01 The counter/timer output, in which case OP3 acts as an open-drain output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
10 The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
11 The 1X clock for the Channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

OPCR[1:0] – OP2 Output Select
This field programs the OP2 output to provide one of the following:
00 The complement of OPR[2].
01 The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
10 The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
11 The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

SOPR – Set the Output Port Bits (OPR)

SOPR[7:0] – Ones in the byte written to this register will cause the corresponding bit positions in the OPR to set to 1. Zeros have no effect.

ROPR – Reset Output Port Bits (OPR)

ROPR[7:0] – Ones in the byte written to the ROPR will cause the corresponding bit positions in the OPR to set to 0. Zeros have no effect.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects one of two sets of baud rates to be generated by the BRG (see Table 3).

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table 4.

Table 4. Bit Rate Generator Characteristics Crystal or Clock = 3.6864MHz

NORMAL RATE (BAUD)	ACTUAL 16X CLOCK (kHz)	ERROR (%)
50	0.8	0
75	1.2	0
110	1.759	-0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	-0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2K	307.2	0
38.4K	614.4	0

NOTE:
Duty cycle of 16X clock is 50% ± 1%.

ACR[6:4] – Counter/Timer Mode And Clock Source Select
This field selects the operating mode of the counter/timer and its clock source as shown in Table 5.

Table 5. ACR 6:4 Field Definition

ACR 6:4	MODE	CLOCK SOURCE
000	Counter	External (IP2)
001	Counter	TxCA – 1X clock of Channel A transmitter
010	Counter	TxCB – 1X clock of Channel B transmitter
011	Counter	Crystal or external clock (X1/CLK) divided by 16
100	Timer	External (IP2)
101	Timer	External (IP2) divided by 16
110	Timer	Crystal or external clock (X1/CLK)
111	Timer	Crystal or external clock (X1/CLK) divided by 16

ACR[3:0] – IP3, IP2, IP1, IP0 Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7:4] – IP3, IP2, IP1, IP0 Change-of-State
These bits are set when a change-of-state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – IP3, IP2, IP1, IP0 Change-of-State
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR – the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to H'00' when the DUART is reset.

ISR[7] – Input Port Change Status
This bit is a '1' when a change-of-state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

ISR[6] – Channel B Change In Break
This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel B 'reset break change interrupt' command.

ISR[5] – RxB Interrupt
This bit indicates that the channel B receiver is interrupting according to the fill level programmed by the MR0 and MR1 registers. This bit has a different meaning than the receiver ready/full bit in the status register.

ISR[4] – TxB Interrupt
This bit indicates that the channel B transmitter is interrupting according to the interrupt level programmed in the MR0[5:4] bits. This bit has a different meaning than the Tx RDY bit in the status register.

ISR[3] – Counter Ready.
In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

ISR[2] – Channel A Change In Break
This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

ISR[1] – RxA Interrupt
This bit indicates that the channel A receiver is interrupting according to the fill level programmed by the MR0 and MR1 registers. This bit has a different meaning than the receiver ready/full bit in the status register.

ISR[0] – TxA Interrupt
This bit indicates that the channel A transmitter is interrupting according to the interrupt level programmed in the MR0[5:4] bits. This bit has a different meaning than the Tx RDY bit in the status register.

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3-OP7 or the reading of the ISR.

CTPU and CTPL – Counter/Timer Registers

The CTPU and CTPL hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTPU/CTPL registers is H'0002'. Note that these registers are write-only and cannot be read by the CPU.

In the timer mode, the C/T generates a square wave whose period is twice the value

(in C/T clock periods) of the CTPU and CTPL. The waveform so generated is often used for a data clock. The formula for calculating the divisor n to load to the CTPU and CTPL for a particular 1X data clock is shown below.

$$n = \frac{C/T\ Clock\ Frequency}{2 \times 16 \times Baud\ rate\ desired}$$

Often this division will result in a non-integer number; 26.03, for example. One can only program integer numbers in a digital divider. Therefore, 26 would be chosen. This gives a baud rate error of 0.03/26.3 which is .114%; well within the ability asynchronous mode of operation.

If the value in CTPU and CTPL is changed, the current half-period will not be affected, but subsequent half periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read at address A3-A0 = 1110). After this, while in timer mode, the C/T will run continuously. Receipt of a start counter command (read with A3-A0 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTPU and CTPL.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3-A0 = H'F'). The command however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

In the counter mode, the value C/T loaded into CTPU and CTPL by the CPU is counted down to 0.. Counting begins upon receipt of a start counter command. Upon reaching terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTPU and CTPL at any time, but the new count becomes effective only on the next start counter commands. If new values have not been loaded, the previous count values are preserved and used for the next count cycle

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTPU and CTPL.

When the C/T clock divided by 16 is selected, the maximum divisor becomes 1,048,575.

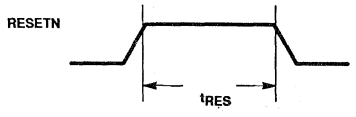


Figure 1. Reset Timing

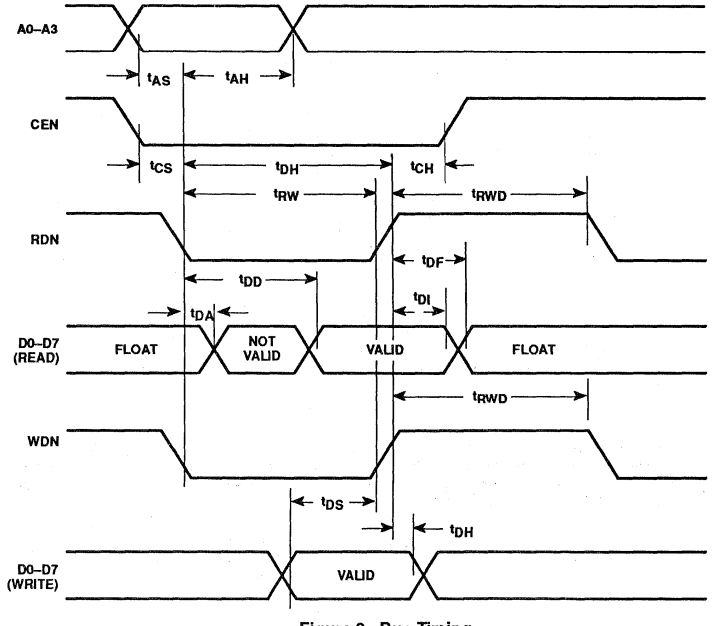


Figure 2. Bus Timing

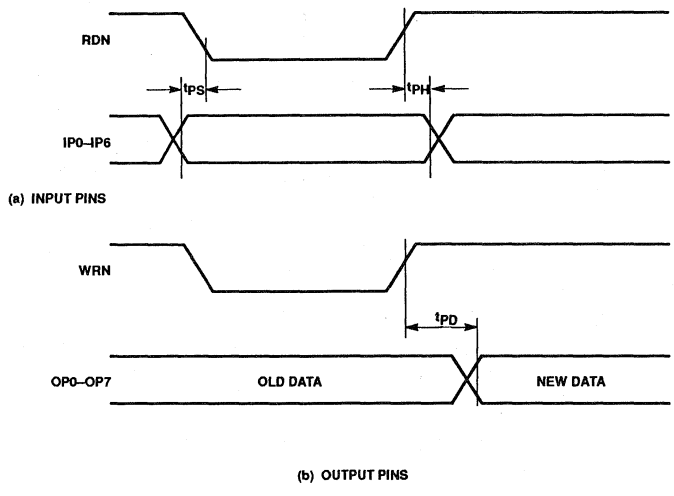
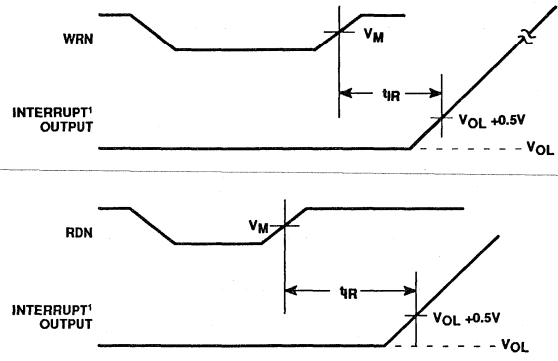
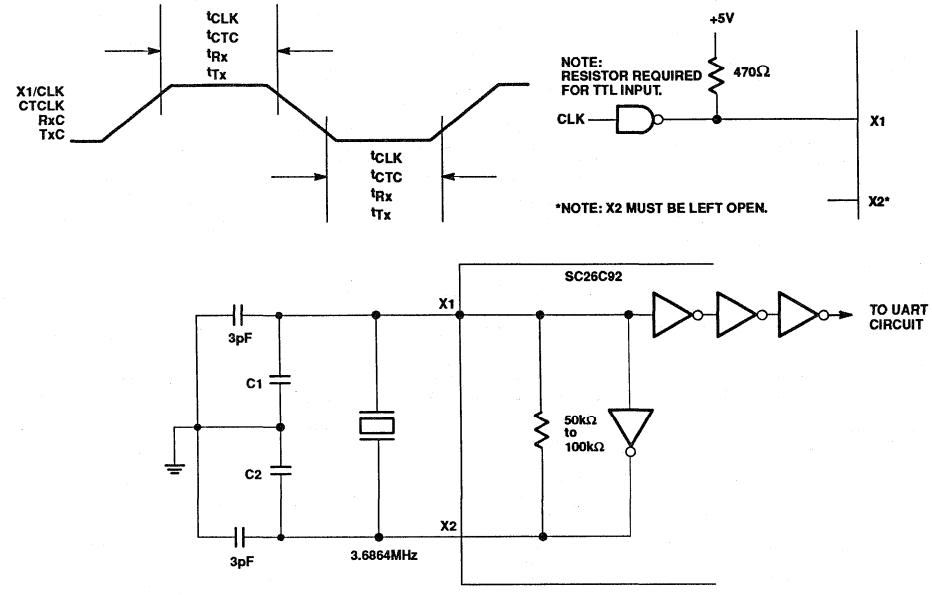


Figure 3. Port Timing



NOTES:
1. INTRN or OP3-OP7 when used as interrupt outputs.
2. The test for open-drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from the midpoint of the switching signal, V_M, to a point 0.5V above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 4. Interrupt Timing



C1 = C2 ~ 24pF FOR C_L = 20pF
C1 and C2 should be chosen according to the crystal manufacturer's specification.
C1 and C2 values will include any parasitic capacitance of the wiring and X1 X2 pins.
Gain at 3.6864MHz: 9 to 13 dB
Phase at 3.6864MHz: 272 to 276 degrees.

Figure 5. Clock Timing

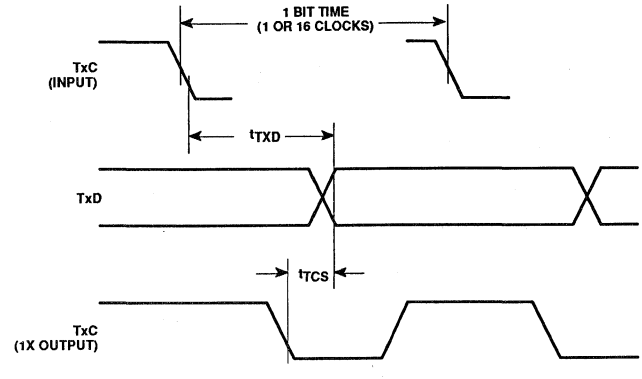


Figure 6. Transmitter External Clocks

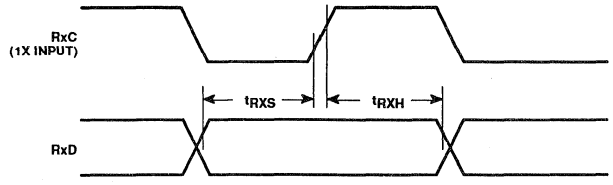
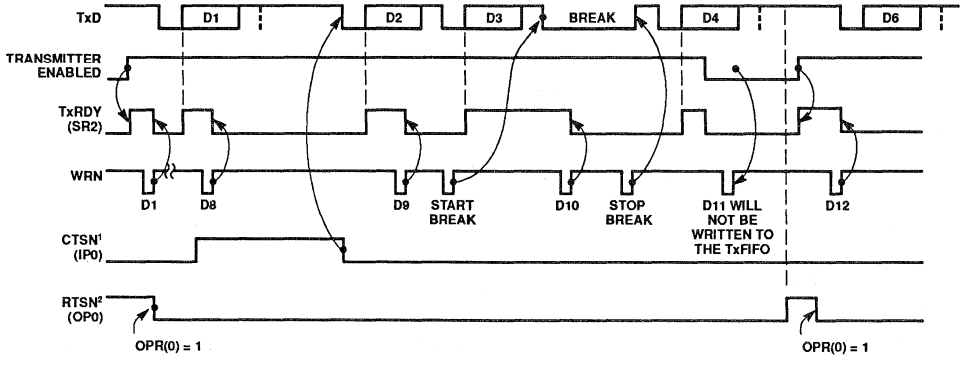
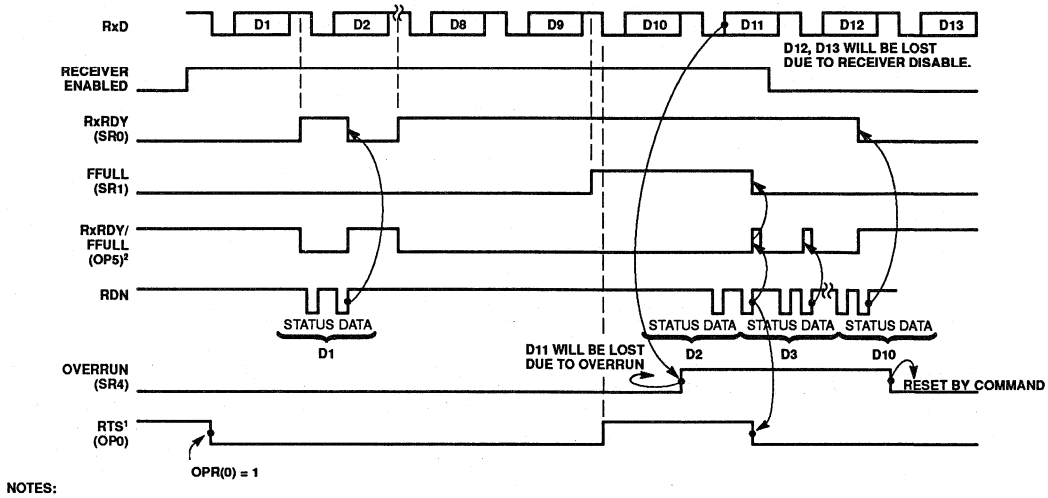


Figure 7. Receiver External Clock



NOTES:
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

Figure 8. Transmitter Timing



NOTES:
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) = 1 and MR(6) = 0.

Figure 9. Receiver Timing

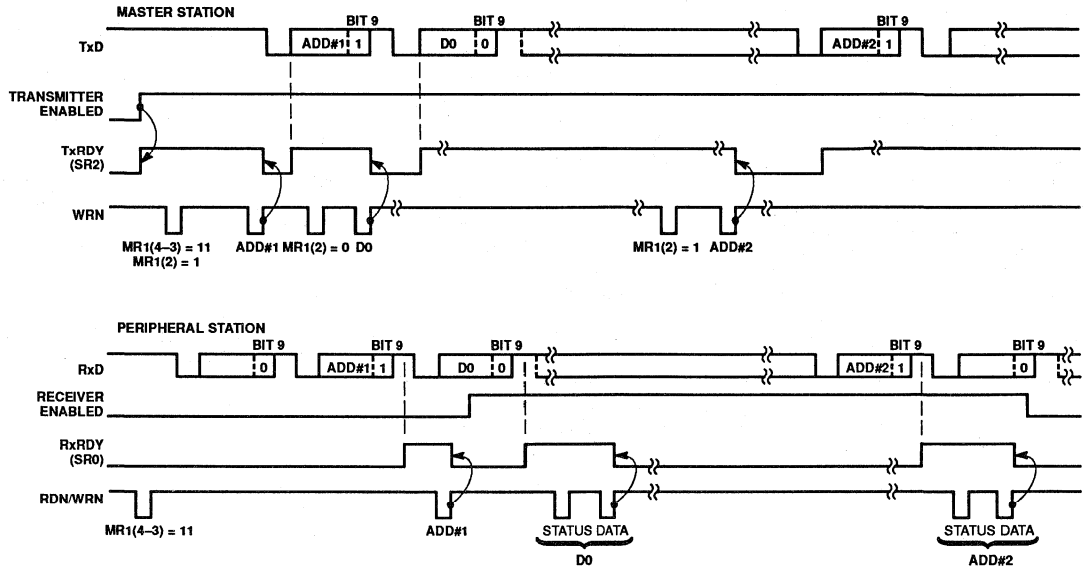


Figure 10. Wake-up Mode

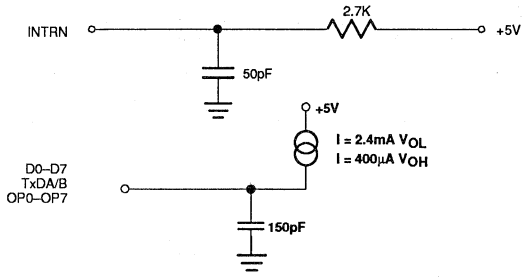


Figure 11. Test Conditions on Outputs

Output Port Notes

The output ports are controlled from four places: the OPCR register, the OPR register, the MR registers and the command register (except the 2681 and 68681) The OPCR register controls the source of the data for the output ports OP2 through OP7. The data source for output ports OP0 and OP1 is controlled by the MR and CR registers. When the OPR is the source of the data for the output ports, the data at the ports is inverted from that in the OPR register. The content of the OPR register is controlled by the "Set Output Port Bits Command" and the "Reset Output Bits Command". These commands are at E and F, respectively. When these commands are used, action takes place only at the bit locations where ones exist. For example, a one in bit location 5 of the data word used with the "Set Output Port Bits" command will result in OPR5 being set to one. The OP5 would then be set to zero (V_{SS}). Similarly, a one in bit position 5 of the data word associated with the "Reset Output Ports Bits" command would set OPR5 to zero and, hence, the pin OP5 to a one (V_{DD}).

The CTS, RTS, CTS Enable Tx signals

CTS (Clear To Send) is usually meant to be a signal to the transmitter meaning that it may transmit data to the receiver. The CTS input is on pin IP0 for TxA and on IP1 for TxB. The CTS signal is active low; thus, it is called CTSAN for TxA and CTSBN for TxB.

RTS is usually meant to be a signal from the receiver indicating that the receiver is ready to receive data. It is also active low and is, thus, called RTSAN for RxA and RTSBN for RxB. RTSAN is on pin OP0 and RTSBN is on OP1. A receiver's RTS output will usually be connected to the CTS input of the associated transmitter. Therefore, one could say that RTS and CTS are different ends of the same wire!

MR2(4) is the bit that allows the transmitter to be controlled by the CTS pin (IP0 or IP1). When this bit is set to one AND the CTS input is driven high, the transmitter will stop sending data at the end of the present character being serialized. It is usually the RTS output of the receiver that will be connected to the transmitter's CTS input. The receiver will set RTS high when the receiver FIFO is full AND the start bit of the ninth character is sensed. Transmission then stops with nine valid characters in the receiver. When MR2(4) is set to one, CTSN must be at zero for the transmitter to operate. If MR2(4) is set to zero, the IP pin will have no effect on the operation of the transmitter.

MR1(7) is the bit that allows the receiver to control OP0. When OP0 (or OP1) is controlled by the receiver, the meaning of that pin will be RTS. However, a point of confusion arises in that OP0 (or OP1) may also be controlled by the transmitter. When the transmitter is controlling this pin, its meaning is not RTS at all. It is, rather, that the transmitter has finished sending its last data byte.

Programming the OP0 or OP1 pin to be controlled by the receiver and the transmitter at the same time is allowed, but would usually be incompatible.

RTS can also be controlled by the commands 1000 and 1001 in the command register. These commands set and reset the bits OPR[0] and OPR[1]. RTS is expressed at the OP0 or OP1 pin which is still an output port. Therefore, the state of OP0 or OP1 should be set low (either by commands of the CR register or by writing to the Set Output Ports Register) for the receiver to generate the proper RTS signal. The logic at the output is basically a NAND of the OPR register and the RTS signal as generated by the receiver. When the RTS flow control is selected via the MR(7) bit state of the OPR register is not changed. Terminating the use of "Flow Control" (via the MR registers) will return the OP0 or OP1 pins to the control of the OPR register.

Dual asynchronous receiver/transmitter (DUART) SCC68692

DESCRIPTION

The Signetics SCC68692 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip CMOS-LSI communications device that provides two full-duplex asynchronous receiver/transmitter channels in a single package. It is compatible with other S68000 family devices and can also interface easily with other microprocessors. The DUART can be used in a polled or interrupt driven systems.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

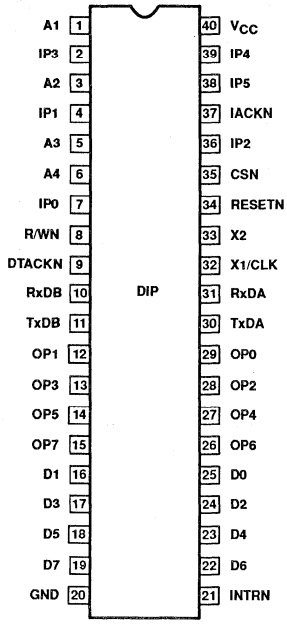
Each receiver is quadruple buffered to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the receiver buffer is full.

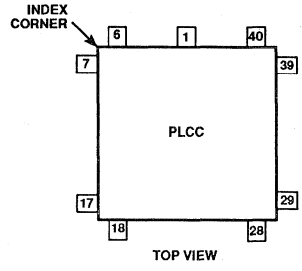
Also provided on the SCC68692 are a multipurpose 6-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

FEATURES

- S68000 bus compatible
- Dual full-duplex asynchronous receiver/transmitters
- Quadruple buffered receiver data register
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4k baud
  - Non-standard rates to 115.2kb
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function 6-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Interrupt vector output on interrupt acknowledge
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer rates: 1X – 1MB/sec, 16X – 125kB/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Power down mode
- Receiver timeout mode
- Commercial and Industrial temperature range versions
- TTL compatible
- Single +5V power supply

PIN CONFIGURATIONS



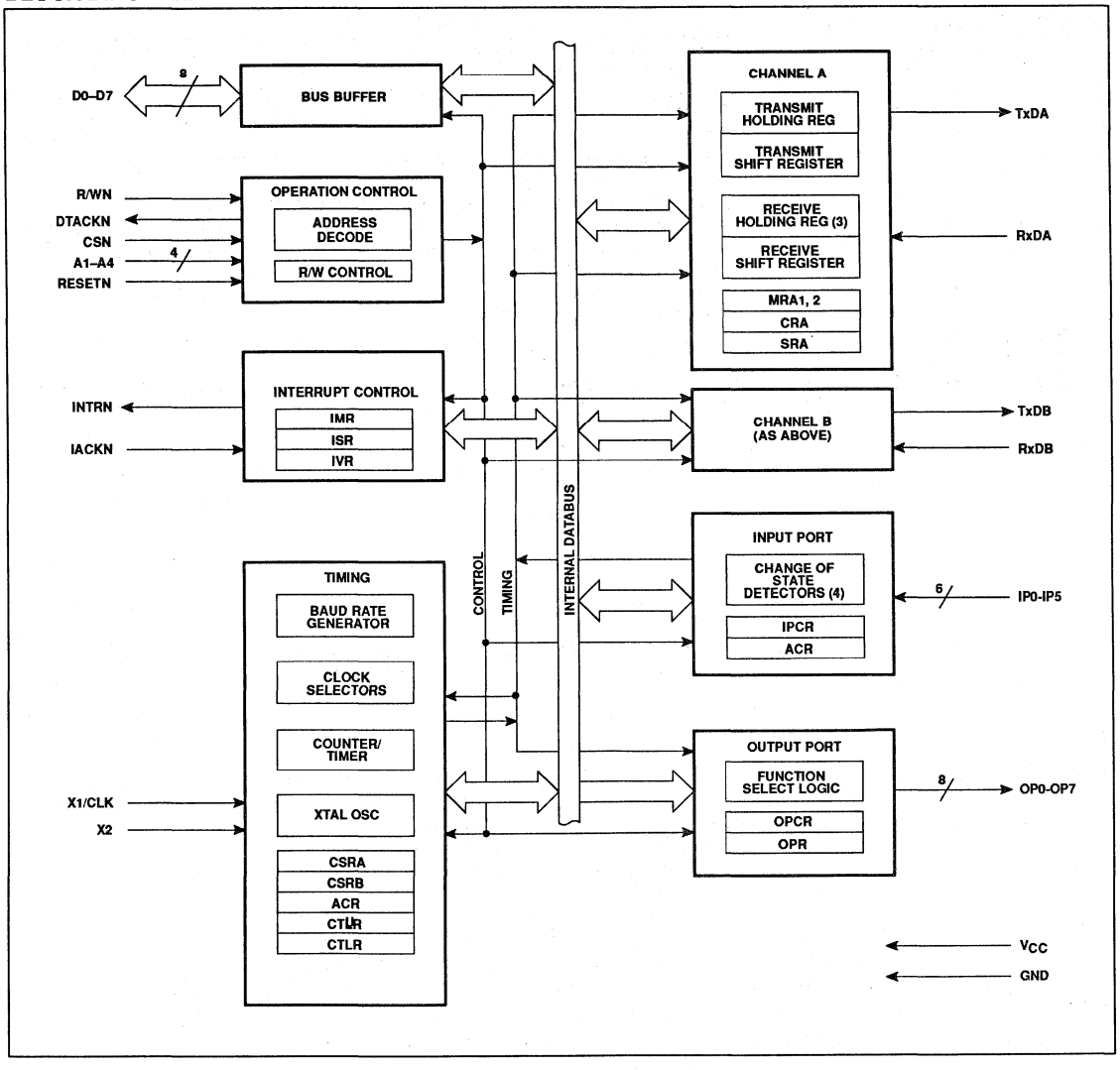


PIN	FUNCTION	PIN	FUNCTION
1	NC	23	NC
2	A1	24	INTRN
3	IP3	25	D6
4	A2	26	D4
5	IP1	27	D2
6	A3	28	D0
7	A4	29	OP6
8	IP0	30	OP4
9	R/WN	31	OP2
10	DTACKN	32	OP0
11	RxDB	33	TxDA
12	NC	34	NC
13	TxDB	35	RxDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CSN
18	D1	40	IP2
19	D3	41	IACKN
20	D5	42	IP5
21	D7	43	IP4
22	GND	44	V_{CC}

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±10%, T_A = 0 to +70°C	V_{CC} = +5V ±10%, T_A = -40 to +85°C
40-Pin Cerdip	SCC68692C1F40	SCC68692E1F40
40-Pin Plastic DIP	SCC68692C1N40	SCC68692E1N40
44-Pin Plastic LCC	SCC68692C1A44	SCC68692E1A44

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NO.	TYPE	NAME AND FUNCTION
D0–D7	25,16,24,17 23,18,22,19	I/O	**Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CSN	35	I	**Chip Enable:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the R/WN and A1–A4 inputs. When CEN is High, the DUART places the D0–D7 lines in the 3-State condition.
R/WN	8	I	**Read/Write:** A High input indicates a read cycle and a low input indicates a write cycle, when a cycle is initiated by assertion of the CSN input.
A1–A4	1,2,5,6	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESETN	34	I	**Reset:** A Low level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), initializes the IVR to hex 0F, puts OP0–OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Resets Test Mode.
DTACKN	9	O	**Data Transfer Acknowledge:** 3-State active-Low output asserted in write, read, or interrupt cycles to indicate proper transfer of data between the CPU and the DUART.
INTRN	21	O	**Interrupt Request:** Active-Low, open-drain output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
IACKN	37	I	**Interrupt Acknowledge:** Active-Low input indicating an interrupt acknowledge cycle. In response, the DUART will place the interrupt vector on the data bus and will assert DTACKN if it has an interrupt pending.
X1/CLK	32	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7).
X2	33	I	**Crystal 2:** Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7). If X1/CLK is driven from an external source, this pin can be left open.
RxDA	31	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	10	I	**Channel B Receive Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	30	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
TxDB	11	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is High, 'space' is Low.
OP0	29	O	**Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	12	O	**Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	28	O	**Output 2:** General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	13	O	**Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	27	O	**Output 4:** General purpose output or Channel A open-drain, active-Low, RxRDYAN/FFULLAN output.
OP5	14	O	**Output 5:** General purpose output or Channel B open-drain, active-Low, RxRDYBN/FFULLBN output.
OP6	26	O	**Output 6:** General purpose output or Channel A open-drain, active-Low, TxRDYAN output.
OP7	15	O	**Output 7:** General purpose output or Channel B open-drain, active-Low, TxRDYBN output.
IP0	7	I	**Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	4	I	**Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	36	I	**Input 2:** General purpose input or Channel B receiver external clock input (RxCB), or counter/timer external clock input. When external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP3	2	I	**Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	39	I	**Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	38	I	**Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
V_{CC}	40	I	**Power Supply:** +5V supply input.
GND	20	I	**Ground**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	Note 4	°C
T_{STG}	Storage temperature range	–65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	–0.5 to +7.0	V
V_S	Voltage from any pin to GND[3]	–0.5 to V_{CC} +0.5	V
P_D	Power dissipation	750	mW

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage (except X1/CLK)[6]		2.0			V
V_{IH}	Input high voltage (except X1/CLK)[7]		2.5			V
V_{IH}	Input high voltage (X1/CLK)		0.8V_{CC}			V
V_{OL}	Output low voltage	I_{OL} = 2.4mA			0.4	V
V_{OH}	Output high voltage (except OD outputs)[4]	I_{OH} = –400µA	V_{CC} –0.5			V
I_{IX1PD}	X1/CLK input current – power down	V_{IN} = 0 to V_{CC}	–10		+10	µA
I_{ILX1}	X1/CLK input low current – operating	V_{IN} = 0	–75		0	µA
I_{IHX1}	X1/CLK input high current – operating	V_{IN} = V_{CC}	0		75	µA
I_{OHX2}	X2 output high current – operating	V_{OUT} = V_{CC}, X1 = 0	0		+75	µA
I_{OHX2S}	X2 output high short circuit current – operating	V_{OUT} = 0, X1 = 0	–10		–1	mA
I_{OLX2}	X2 output low current – operating	V_{OUT} = 0, X1 = V_{CC}	–75		0	µA
I_{OLX2S}	X2 output low short circuit current – operating and power down	V_{OUT} = V_{CC}, X1 = V_{CC}	1		10	mA
I_I	Input leakage current:					
	All except input port pins	V_{IN} = 0 to V_{CC}	–10		+10	µA
	Input port pins	V_{IN} = 0 to V_{CC}	–20		+10	µA
I_{OZH}	Output off current high, 3-State data bus	V_{IN} = V_{CC}			10	µA
I_{OZL}	Output off current low, 3-State data bus	V_{IN} = 0V	–10			µA
I_{ODL}	Open-drain output low current in off State	V_{IN} = 0	–10			µA
I_{ODH}	Open-drain output high current in off State	V_{IN} = V_{CC}			10	µA
I_{CC}	Power supply current[5]					
	Operating mode	TTL input levels			10	mA
		CMOS input levels			10	mA
	Power down mode[12]	TTL input levels			3.0	mA
		CMOS input levels			2.0	mA

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test condition for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
5. All outputs are disconnected. Inputs are switching between TTL levels of 2.4V and 0.4V or CMOS levels of V_{CC} –0.2V and V_{SS} + 0.2V.
6. $T_A \geq 0°C$
7. $T_A < 0°C$

AC CHARACTERISTICS[1, 2, 4]

SYMBOL	FIGURE	PARAMETER	LIMITS Min	LIMITS Typ[3]	LIMITS Max	UNIT
Reset Timing						
t_{RES}	1	RESET pulse width	200			ns
Bus Timing[5]						
t_{AS}	2,3,4	A1–A4 setup time to CSN Low	10			ns
t_{AH}	2,3,4	A1–A4 hold time from CSN Low	100			ns
t_{RWS}	2,3,4	RWN setup time to CSN High	0			ns
t_{RWH}	2,3,4	RWN holdup time to CSN High	0			ns
t_{CSW}[8]	2,3,4	CSN High pulse width	160			ns
t_{CSD}[9]	2,3,4	CSN or IACKN High from DTACKN Low	20			ns
t_{DD}	2,3,4	Data valid from CSN or IACKN Low			175	ns
t_{DA}	2	RDN Low to data bus active[8]	15			ns
t_{DF}	2,3,4	Data bus floating from CSN or IACKN High[8]			125	ns
t_{DI}	2	RDN High to data bus invalid[8]	20			ns
t_{DS}	2,3,4	Data setup time to CLK High	100			ns
t_{DH}	2,3,4	Data hold time from CSN High	0			ns
t_{DAL}	2,3,4	DTACKN Low from read data valid	0			ns
t_{DCR}	2,3,4	DTACKN Low (read cycle) from CLK High			125	ns
t_{DCW}	2,3,4	DTACKN Low (write cycle) form CLK High			125	ns
t_{DAH}	2,3,4	DTACKN High from CSN or IACKN High			100	ns
t_{DAT}	2,3,4	DTACKN High impedance from CSN or IACKN High			125	ns
t_{CSC}[7]	2,3,4	CSN or IACKN setup time to clock High	90			ns
Port Timing[5]						
t_{PS}	5	Port input setup time to CSN Low	0			ns
t_{PH}	5	Port input hold time from CSN High	0			ns
t_{PD}	5	Port output valid from CSN High			400	ns
Interrupt Timing						
t_{IR}	6	INTRN (or OP3–OP7 when used as interrupts) negated from:				
		Read RHR (RxRDY/FFULL interrupt)			300[10]	ns
		Write THR (TxRDY interrupt)			300[10]	ns
		Reset command (break interrupt)			300[10]	ns
		Stop C/T command (counter interrupt)			300[10]	ns
		Read IPCR (input port change interrupt)			300[10]	ns
		Write IMR (clear of interrupt mask bit)			300[10]	ns
Clock Timing						
t_{CLK}	7	X1/CLK High or Low time	100			ns
f_{CLK}	7	X1/CLK frequency	0[11]	3.6864	4	MHz
t_{CTC}	7	CTCLK (IP2) High or Low time	100			ns
f_{CTC}	7	CTCLK (IP2) frequency[9]	100		4	MHz
t_{RX}	7	RxC High or Low time	220			ns
f_{RX}	7	RxC frequency (16X)[9]	100		2	MHz
		(1X)[9]	100		1	MHz
t_{TX}	7	TxC High or Low time	220			ns
f_{TX}	7	TxC frequency (16X)[9]	0		2	MHz
		(1X)[9]	0		1	MHz
Transmitter Timing						
t_{TXD}	8	TxD output delay from TxC Low			350	ns
t_{TCS}	8	Output delay from TxC Low to TxD data output			150	ns
Receiver Timing						
t_{RXS}	9	RxD data setup time to RxC High	240			ns
t_{RXH}	9	RxD data hold time from RxC High	200			ns

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test condition for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
5. This specification will impose maximum 68000 CPU CLK to 6MHz. Higher CPU CLK can be used if repeating bus reads are not performed. Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.
6. This specification imposes a lower bound on CSN and IACKN Low, guaranteeing that it will be Low for at least 1 CLK period. This requirement is made on CSN only to insure assertion of DTACKN and not to guarantee operation of the part.
7. This specification is made only to insure that DTACKN is asserted with respect to the rising edge of the X1/CLK pin as shown in the timing diagram, not to guarantee operation of the part. If the setup time is violated, DTACKN may be asserted as shown, or may be asserted one clock cycle later.
8. Guaranteed by characterization of sample units.
9. Minimum frequencies are not tested but are guaranteed by design.
10. 325ns maximum for T_A > 70°C.
11. Operation to 0MHz is assured by design. Minimum test frequency is 2.0MHz.
12. See UART application note for power down currents less than 5µA.

BLOCK DIAGRAM

The SCC68692 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the Block Diagram.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The DTACKN output is asserted during write and read cycles to indicate to the CPU that data has been latched on a write cycle, or that valid data is present on the bus on a read cycle.

Interrupt Control

A single active-Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR), the Auxiliary Control Register (ACR), and the Interrupt Vector Register (IVR). The IMR may be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. When IACKN is asserted, and the DUART has an interrupt pending, the DUART responds by placing the contents of the IVR register on the data bus and asserting DTACKN.

Outputs OP3–OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART.

If an external is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 7.

If an external clock is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 5.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. A 3.6864MHz crystal or external clock must be used to get the standard baud rate. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

The Counter/Timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

Communications Channels A and B

Each communications channel of the SCC68692 comprises a full-duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

Input Port

The inputs to this unlatched 6-bit port can be read by the CPU by performing a read operation at address H'D'. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always be read as a logic 1 and D6 will reflect the level of IP2. The pins of this port can also serve as auxiliary inputs to certain portions fo the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs, lasting longer than 25 – 50µs, will set the corresponding bit in the input port change register. The bits are

cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU.

The input port pulse detection circuitry uses a 38.4kHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25µs (this assumes that the clock input is 3.6864MHz). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs "coincident with the first sample pulse". The 50µs time refers to the situation in which the change-of-state is "just missed" and the first change-of-state is not detected until 25µs later.

Output Port

The output port pins may be controlled by the OPR, OPCR, MR and the CR registers. Via appropriate programming they may be just another parallel port to external circuits, or they may represent many internal conditions of the UART. When this 8-bit port is used as a general purpose output port, the output port pins assume a state which is the complement of the Output Port Register (OPR). OPR(n) = 1 results in OP(n) = Low and vice versa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operation at address H'E' with the accompanying data specifying the bits to be reset (1 = set, 0 = no change). Likewise, a bit is reset by a write at address H'F' with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Outputs can be also be individually assigned specific functions by appropriate programming of the Channel A mode registers (MR1A, MR2A), the Channel B mode registers (MR1B, MR2B), and the Output Port Configuration Register (OPCR).

OPERATION

Transmitter

The SCC68692 is conditioned to transmit data when the transmitter is enabled through the command register. The SCC68692 indicates
to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When a character is loaded into the Transmit Holding Register (THR), the above conditions are negated. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again which means one full character time of buffering is provided. Characters cannot be loaded into the THR while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains High and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the THR. If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous Low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS operation is enable, the CTSN input must be Low in order for the character to be transmitted. If it goes High in the middle of a transmission, the character in the shift register is transmitted and TxDA then remains in the marking state until CTSN goes Low. The transmitter can also control the deactivation of the RTSN output. If programmed, the RTSN output will be reset one bit time after the character in the transmit shift register and transmit holding register (if any) are completely transmitted, if the transmitter has been disabled.

Receiver

The SCC68692 is conditioned to receive data when enabled through the command register. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7–1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive Holding Register (RHR) and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than 8 bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1. The RxD input must return to a High condition for at least one-half bit time before a search for the next start bit begins.

The RHR consists of a First-In-First-Out (FIFO) stack with a capacity of three characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4] will be set-upon receipt of the start bit of the new (overrunning) character.

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

Timeout Mode

The timeout mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RHR, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU may not know there is data left in the FIFO. The CTU and CTL value would be programmed for just over one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all of the characters from the FIFO, but the last character received has started the count. If there is no new data during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

This mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the timeout mode for that channel. Writing a 'Cx' to CRA or CRB will disable the timeout mode. The timeout mode should only be used by one channel at once, since it uses the C/T. CTU and CTL must be loaded with a value greater than the normal receive character period. The timeout mode disables the regular START/STOP Counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RHR, the C/T is stopped after 1 C/T clock, reloaded with the value in CTU and CTL and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Since receiving a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Timeout Mode On' command, CRx = 'Ax', will also clear the counter ready bit and stop the counter until the next character is received.

Multidrop Mode

The DUART is equipped with a wake up mode for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wakeup' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the THR.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RHR FIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems. For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to MR1x by RESET or by issuing a 'reset pointer' command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1x, switches the pointer to MR2x. The pointer then remains at MR2x, so that subsequent accesses are always to MR2x unless the pointer is reset to MR1x as described above.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'0A' should never be read during normal operation since they are reserved for internal diagnostics.

Table 1. Register Addressing

A3	A2	A1	A0	READ (RDN = 0)	WRITE (WRN = 0)
0	0	0	0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	BRG Test	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RHRA)	Tx Holding Register A (THRA)
0	1	0	0	Input Port Change Register (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Register (CRUR)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Register (CTLR)
1	0	0	0	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	1X/16X Test	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RHRB)	Tx Holding Register B (THRB)
1	1	0	0	Interrupt Vector Register (IVR)	Interrupt Vector Register (IVR)
1	1	0	1	Input Port	Output Port Conf. Register (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command
1	1	1	1	Stop Counter Command	Reset Output Port Bits Command

MR1A – Channel A Mode Register 1

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRA. After reading or writing MR1A, the pointer will point to MR2A.

MR1A[7] – Channel A Receiver Request-to-Send Control

This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR1A[7] = 1 causes RTSAN to be negated upon receipt of a valid start bit if the Channel A FIFO is full. However, OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

MR1A[6] – Channel A Receiver Interrupt Select

This bit selects either the Channel A receiver ready status (RxRDY) or the Channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to be output on OP4 if it is programmed as an interrupt output via the OPCR.

MR1A[5] – Channel A Error Mode Select

This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break) for Channel A. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block" mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

MR1A[4:3] – Channel A Parity Mode Select

If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data MR1A[4:3] = 11 selects Channel A to operate in the special multidrop mode described in the Operation section.

MR1A[2] – Channel A Parity Type Select

This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

MR1A[1:0] – Channel A Bits Per Character Select

This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2A – Channel A Mode Register 2

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

MR2A[7:6] – Channel A Mode Select

Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The Channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop has been retransmitted.

MR2A[5] – Channel A Transmitter Request-to-Send Control

This bit controls the deactivation of the RTSAN output (OP0) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR2A[5] = 1 caused OPR[0] to be reset automatically one bit time after the characters in the Channel A transmit shift register and in the THR, if any, are completely transmitted including the programmed number of stop bits, if the transmitter is not enabled. This feature can be used to automatically terminate the transmission of a message as follows:

1. Program auto-reset mode: MR2A[5] = 1.
2. Enable transmitter.
3. Assert RTSAN: OPR[0] = 1.
4. Send message.
5. Disable transmitter after the last character is loaded into the Channel A THR.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

NOTE: When TxEMT and TxRDY bits are one just before a write to the Transmit Holding register, then a command to disable the transmitter should be delayed until the TxRDY is at one again. TxRDY will set to one at the start bit time.

Table 2. Register Bit Formats

	BIT 7	BIT 6	BIT 5	BIT 4 BIT 3	BIT 2	BIT 1 BIT 0
	RxRTS CONTROL	**RxINT SELECT**	**ERROR MODE**	**PARITY MODE**	**PARITY TYPE**	**BITS PER CHARACTER**
MR1A MR1B	0 = No 1 = Yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multidrop Mode	0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8

	BIT 7 BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	CHANNEL MODE	**TxRTS CONTROL**	**CTS ENABLE Tx**	**STOP BIT LENGTH***			
MR2A MR2B	00 = Normal 01 = Auto-Echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

NOTE: *Add 0.5 to values shown for 0 – 7 if channel is programmed for 5 bits/char.

	BIT 7 BIT 6 BIT 5 BIT 4	BIT 3 BIT 2 BIT 1 BIT 0
	RECEIVER CLOCK SELECT	**TRANSMITTER CLOCK SELECT**
CSRA CSRB	See Text	See Text

	BIT 7 BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MISCELLANEOUS COMMANDS	**DISABLE Tx**	**ENABLE Tx**	**DISABLE Rx**	**ENABLE Rx**
CRA CRB	See Text	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE: Access to the upper four bits of the command register should be separated by three (3) edges of the X1 clock.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RECEIVED BREAK*	**FRAMING ERROR***	**PARITY ERROR***	**OVERRUN ERROR**	**TxEMT**	**TxRDY**	**FFULL**	**RxRDY**
SRA SRB	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:

* These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a "reset error status" command. In character mode they are discarded when the corresponding data character is read from the FIFO.

Table 2. Register Bit Formats (Continued)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3 BIT 2	BIT 1 BIT 0
	OP7	OP6	OP5	OP4	OP3	OP2
OPCR	0 = OPR[7] 1 = TxRDYB	0 = OPR[6] 1 = TxRDYA	0 = OPR[5] 1 = RxRDY/ FFULLB	0 = OPR[4] 1 = RxRDY/ FFULLA	00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB(1x) 11 = RxCB(1x)	00 = OPR[2] 01 = TxCA(16x) 10 = TxCA(1x) 11 = RxCA(1x)

	BIT 7	BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	BRG SET SELECT	COUNTER/TIMER MODE AND SOURCE	DELTA IP3 INT	DELTA IP2 INT	DELTA IP1 INT	DELTA IP0 INT
ACR	0 = set 1 1 = set 2	See Table 4	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	DELTA IP3	DELTA IP2	DELTA IP1	DELTA IP0	IP3	IP2	IP1	IP0
IPCR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IN PORT CHANGE	DELTA BREAK B	RxRDY/ FFULLB	TxRDYB	COUNTER READY	DELTA BREAK A	RxRDY/ FFULLA	TxRDYA
ISR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IN PORT CHANGE INT	DELTA BREAK B INT	RxRDY/ FFULLB INT	TxRDYB INT	COUNTER READY INT	DELTA BREAK A INT	RxRDY/ FFULLA INT	TxRDYA INT
IMR	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]
CTUR								

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]
CTLR								

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IVR[7]	IVR[6]	IVR[5]	IVR[4]	IVR[3]	IVR[2]	IVR[1]	IVR[0]
IVR								

MR2A[4] – Channel A Clear-to-Send Control
If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IPO) each time it is ready to send a character. If IPO is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character.

MR2A[3:0] – Channel A Stop Bit Length Select
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1–9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1–1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit is enabled).

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

MR1B – Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to MR1A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

MR2B – Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode register are identical to the bit definitions for MR2A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

CSRA – Channel A Clock Select Register

CSRA[7:4] – Channel A Receiver Clock Select
This field selects the baud rate clock for the Channel A transmitter. The field definition is shown in Table 3.

CSRA[3:0] – Channel A Transmitter Clock Select
This field selects the baud rate clock for the Channel A transmitter. The field definition is as shown in Table 3, except as follows:

CSRA[3:0]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP3–16X	IP3–16X
1111	IP3–1X	IP3–1X

The transmitter clock is always a 16X clock except for CSRA[3:0] = 1111.

Table 3. Baud Rate

CSRA[7:4]	ACR[7] = 0	Baud Rate ACR[7] = 1
0000	50	75
0001	110	110
0010	134.5	134.5
0011	200	150
0100	300	300
0101	600	600
0110	1,200	1,200
0111	1,050	2,000
1000	2,400	2,400
1001	4,800	4,800
1010	7,200	1,800
1011	9,600	9,600
1100	38.4k	19.2k
1101	Timer	Timer
1110	IP4–16X	IP4–16X
1111	IP4–1X	IP4–1X

NOTE: The receiver clock is always a 16X clock except for CSRA[7:4] = 1111.

CSRB – Channel B Clock Select Register

CSRB[7:4] – Channel B Receiver Clock Select
This field selects the baud rate clock for the Channel B receiver. The field definition is as shown in Table 3, except as follows:

CSRB[7:4]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP2–16X	IP2–16X
1111	IP2–1X	IP2–1X

The receiver clock is always a 16X clock except for CSRB[7:4] = 1111.

CSRB[3:0] – Channel B Transmitter Clock Select
This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 3, except as follows:

CSRB[3:0]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP5–16X	IP5–16X
1111	IP5–1X	IP5–1X

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

CRA – Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.
NOTE: Access to the upper four bits of the command register should be separated by three (3) edges of the X1 clock.

CRA[7:4] – Miscellaneous Commands
The encoded value of this field may be used to specify a single command as follows:
0000 No command.
0001 Reset MR pointer. Causes the Channel A MR pointer to point to MR1.
0010 Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.
0011 Reset transmitter. Resets the Channel A transmitter as if a hardware reset had been applied.
0100 Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.
0101 Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.
0110 Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the

transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.

0111 Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted.

1000 Assert RTSN. Causes the RTSN output to be asserted (Low).

1001 Negate RTSN. Causes the RTSN output to be negated (High).

1010 Set Timeout Mode On. The receiver in this channel will restart the C/T as each receive character is transferred from the shift register to the RHR. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset.

1011 Not used.

1100 Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued

1101 Not used.

1110 Power Down Mode On. In this mode, the DUART oscillator is stopped and all functions requiring this clock are suspended. The execution of commands other than disable power down mode (1111) requires a X1/CLK. While in the power down mode, do not issue any commands to the CR except the disable power down mode command. It is recommended that the transmitter and receiver be disabled prior to placing the DUART into power down mode. This command is in CRA only. Design Note: The part will not output DTACKN while in power down mode. Use automatic DTACKN generation.

1111 Disable Power Down Mode. This command restarts the oscillator. After invoking this command, wait for the oscillator to start up before writing further commands to the CR. This command is in CRA only.

CRA[3] – Disable Channel A Transmitter
This command terminates transmitter operation and reset the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CRA[2] – Enable Channel A Transmitter
Enables operation of the Channel A transmitter. The TxRDY status bit will be asserted.

CRA[1] – Disable Channel A Receiver
This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

CRA[0] – Enable Channel A Receiver
Enables operation of the Channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start bit state.

CRB – Channel B Command Register

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, with the exception of comamnds "Ex" and "Fx" which are used for power downmode. These two commands are not used in CRB. All other control actions that apply to CRA also apply to CRB.

SRA – Channel A Status Register

SRA[7] – Channel A Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line to the marking state for at least one-half a bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the Channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

SRA[6] – Channel A Framing Error
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SRA[5] – Channel A Parity Error
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity. In the special multidrop mode, the parity error bit stores the received A/D bit.

SRA[4] – Channel A Overrun Error
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost. This bit is cleared by a 'reset error status' command.

SRA[3] – Channel A Transmitter Empty (TxEMTA)
This bit will be set when the Channel A transmitter underruns; i.e., both the Transmit Holding Register (THR) and the transmit shift register are empty. It is set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU or when the transmitter is disabled.

SRA[2] – Channel A Transmitter Ready (TxRDYA)
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, e.g., characters loaded into the THR while the transmitter is disabled will not be transmitted.

SRA[1] – Channel A FIFO Full (FFULLA)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the

RHR. If a character is waiting in the receive shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

SRA[0] – Channel A Receiver Ready (RxRDYA)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift to the FIFO and reset when the CPU reads the RHR, if after this read there are not more characters still in the FIFO.

SRB – Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

OPCR – Output Port Configuration Register

OPCR[7] – OP7 Output Select
This bit programs the OP7 output to provide one of the following:

0 The complement of OPR[7].

1 The Channel B transmitter interrupt output which is the complement of TxRDYB. When in this mode OP7 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[6] – OP6 Output Select
This bit programs the OP6 output to provide one of the following:

0 The complement of OPR[6].

1 The Channel A transmitter interrupt output which is the complement of TxRDYA. When in this mode OP6 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[5] – OP5 Output Select
This bit programs the OP5 output to provide one of the following:

0 The complement of OPR[5].

1 The Channel B transmitter interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[4] – OP4 Output Select
This field programs the OP4 output to provide one of the following:

0 The complement of OPR[4].

1 The Channel A receiver interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[3:2] – OP3 Output Select
This bit programs the OP3 output to provide one of the following:

00 The complement of OPR[3].

01 The counter/timer output, in which case OP3 acts as an open-drain output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.

10 The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.

11 The 1X clock for the Channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

OPCR[1:0] – OP2 Output Select
This field programs the OP2 output to provide one of the following:

00 The complement of OPR[2].

01 The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.

10 The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.

11 The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects one of two sets of baud rates to be generated by the BRG.

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.

Set 2: 75, 110, 134.5, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, and 19.2k baud.

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table 4.

Table 4. Bit Rate Generator Characteristics Crystal or Clock = 3.6864MHz

NORMAL BAUD RATE	ACTUAL 16x CLOCK (kHz)	ERROR (%)
50	0.8	0
75	1.2	0
110	1.759	–0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	–0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2k	307.2	0
38.4k	614.4	0

NOTE:
Duty cycle of 16x clock is 50% ± 1%.

ACR[6:4] – Counter/Timer Mode And Clock Source Select
This field selects the operating mode of the counter/timer and its clock source as shown in Table 5.

Table 5. ACR [6:4] Field Definition

[6:4]	MODE	CLOCK SOURCE
000	Counter	External (IP2)
001	Counter	TxCA – 1x clock of Channel A transmitter
010	Counter	TxCB – 1x clock of Channel B transmitter
011	Counter	Crystal or external clock (x1/CLK) divided by 16
100	Timer	External (IP2)
101	Timer	External (IP2) divided by 16
110	Timer	Crystal or external clock (X1/CLK)
111	Timer	Crystal or external clock (X1/CLK) divided by 16

ACR[3:0] – IP3, IP2, IP1, IP0 Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt

output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7:4] – IP3, IP2, IP1, IP0 Change-of-State
These bits are set when a change-of-state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – IP3, IP2, IP1, IP0 Change-of-State
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR – the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to H'00' when the DUART is reset.

ISR[7] – Input Port Change Status
This bit is a '1' when a change-of-state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

ISR[6] – Channel B Change In Break
This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel B 'reset break change interrupt' command.

ISR[5] – Channel B Receiver Ready or FIFO Full
The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that a character has been received in Channel B and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel B FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

ISR[4] – Channel B Transmitter Ready
This bit is a duplicate of TxRDYB (SRB[2]).

ISR[3] – Counter Ready.
In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

ISR[2] – Channel A Change In Break
This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

ISR[1] – Channel A Receiver Ready Or FIFO Full
The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that a character has been received in Channel A and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel A FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the ISR[0] and IMR waiting character is loaded into the FIFO.

ISR[0] – Channel A Transmitter Ready
This bit is a duplicate of TxRDYA (SRA[2]).

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3–OP7 or the reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is H'0002'. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. The waveform so generated is often used for a data clock. The formula for calculating the divisor n to load to the CTUR and CTLR for a particular 1X data clock is shown below:

$$n = \frac{C/T\ Clock\ Frequency}{2 \times 16\ Baud\ rate\ desired}$$

Often this division will result in a non-integer number; 26.03, for example. One can only program integer numbers in a digital divider. Therefore, 26 would be chosen. This gives a baud rate error of 0.03/26.3 which is .114%; well within the ability asynchronous mode of operation.

If the value in CTUR and CTLR is changed, the current half-period will not be affected, but subsequent half periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read at address A3–A0 = 1110). After this, while in timer mode, the C/T will run continuously. Receipt of a start counter command (read with A3–A0 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3–A0 = H'F'). The command however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter commands. If new values have not been loaded, the previous count values are preserved and used for the next count cycle

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

IVR – Interrupt Vector Register

This register contains the interrupt vector. The register is initialized to H'0F' by RESET. The contents of the register are placed on the data bus when the DUART responds to a valid interrupt acknowledge cycle.

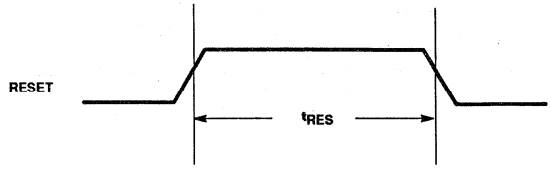


Figure 1. Reset Timing

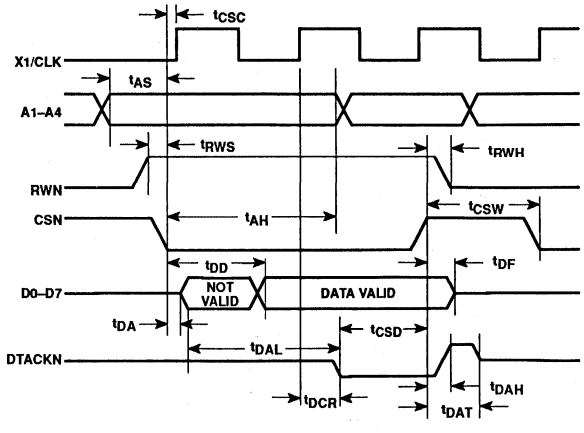


Figure 2. Bus Timing (Read Cycle)

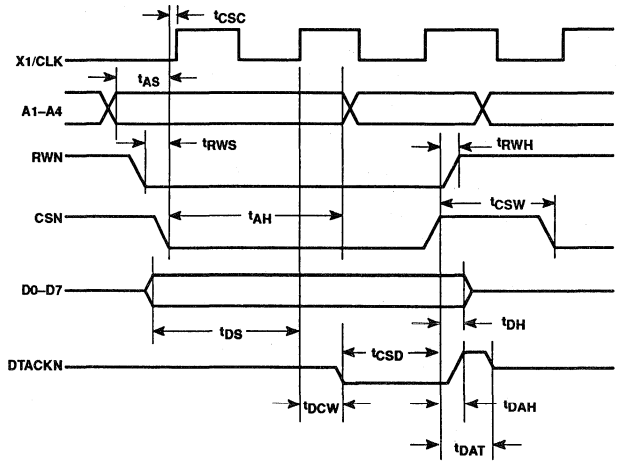


Figure 3. Bus Timing (Write Cycle)

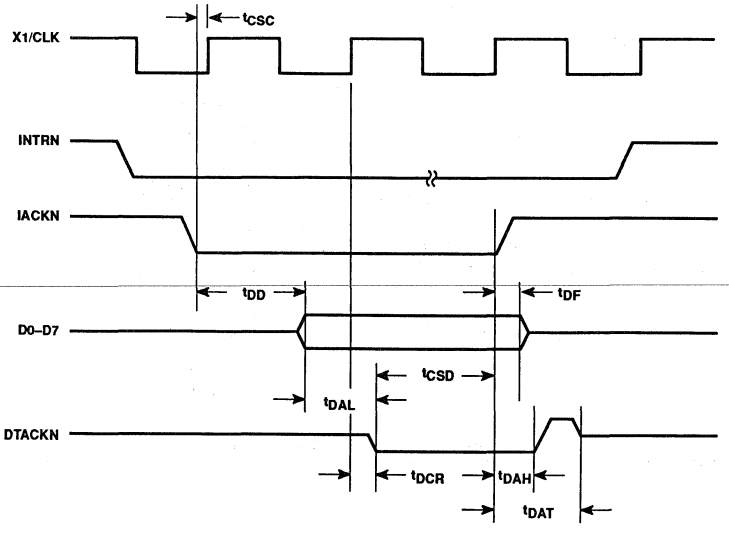


Figure 4. Interrupt Cycle Timing

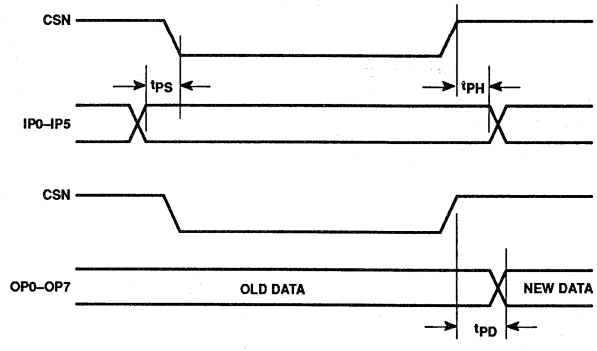
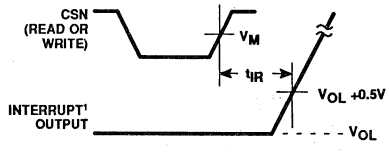


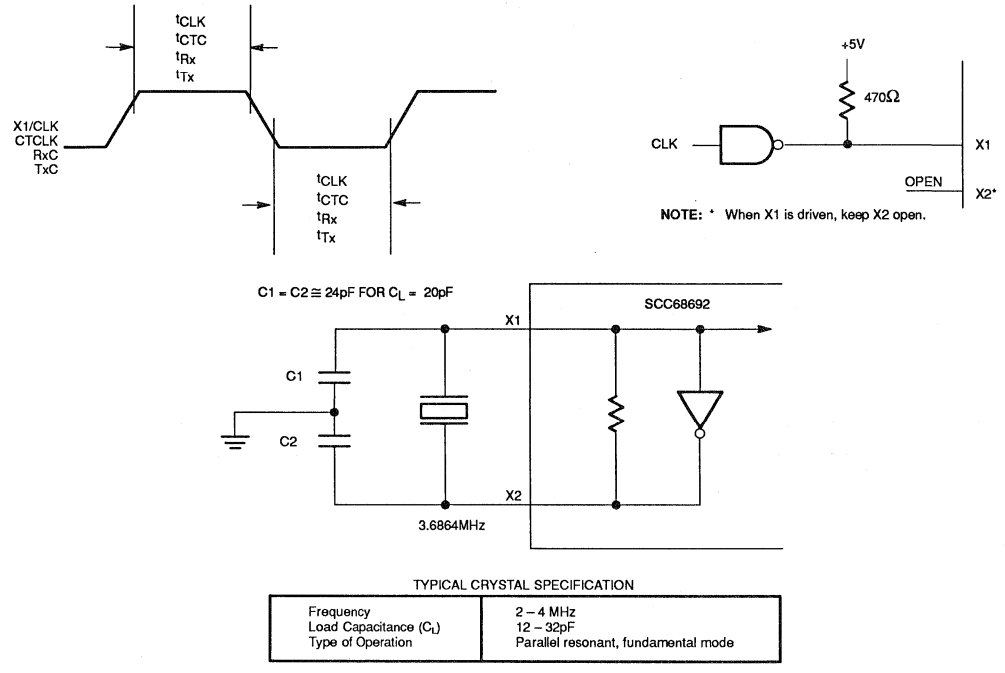
Figure 5. Port Timing



NOTES:

1. INTRN or OP3 – OP7 when used as interrupt outputs.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from themidpoint of the switching signal, V_M, to a point 0.5 volts above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 6. Interrupt Timing



TYPICAL CRYSTAL SPECIFICATION

Frequency	2 – 4 MHz
Load Capacitance (C_L)	12 – 32pF
Type of Operation	Parallel resonant, fundamental mode

Figure 7. Clock Timing

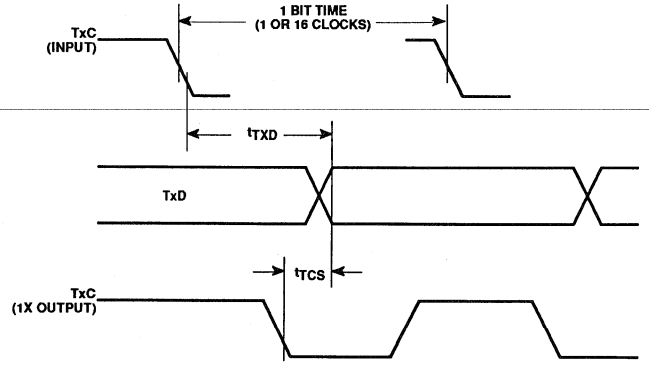


Figure 8. Transmit Timing

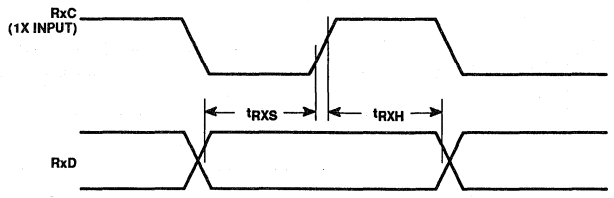
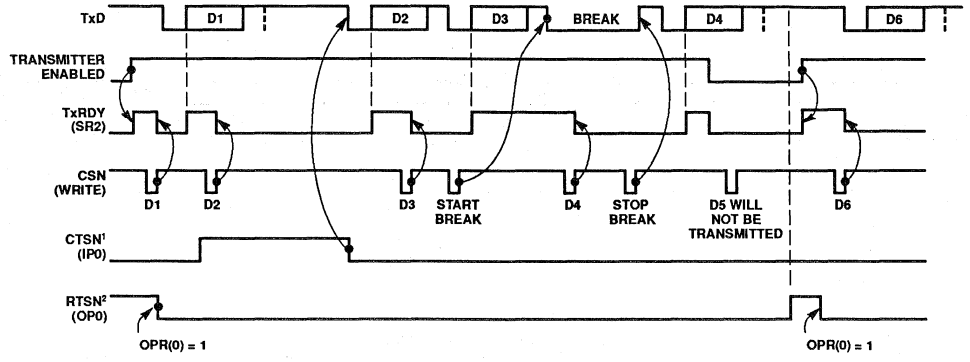
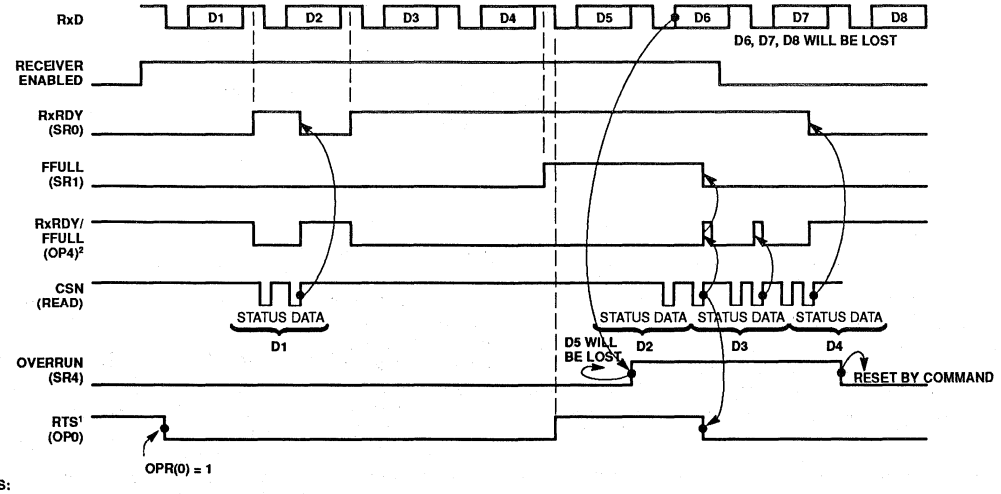


Figure 9. Receive Timing



NOTES:
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

Figure 10. Transmitter Timing



NOTES:
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) and MR1(6) = 0.

Figure 11. Receiver Timing

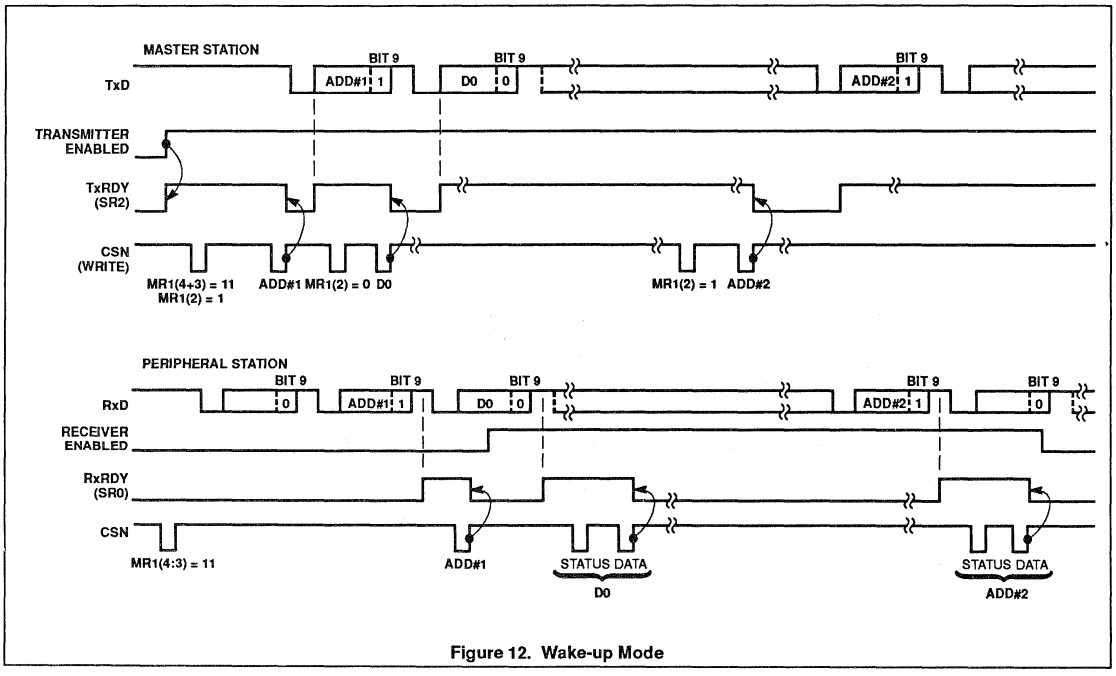


Figure 12. Wake-up Mode

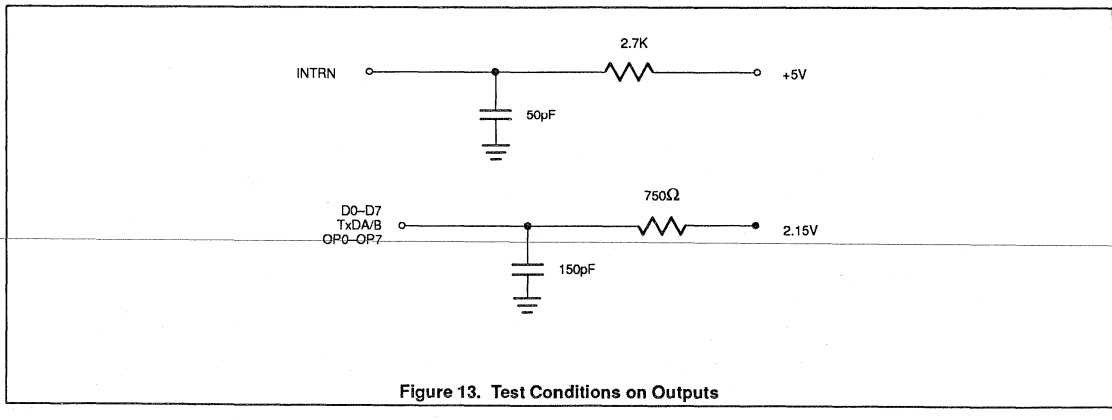


Figure 13. Test Conditions on Outputs

Output Port Notes

The output ports are controlled from four places: the OPCR register, the OPR register, the MR registers and the command register. The OPCR register controls the source of the data for the output ports OP2 through OP7. The data source for output ports OP0 and OP1 is controlled by the MR and CR registers. When the OPR is the source of the data for the output ports, the data at the ports is inverted from that in the OPR register. The content of the OPR register is controlled by the "Set Output Port Bits Command" and the "Reset Output Bits Command". These commands are at E and F, respectively. When these commands are used, action takes place only at the bit locations where ones exist. For example, a one in bit location 5 of the data word used with the "Set Output Port Bits" command will result in OPR5 being set to one. The OP5 would then be set to zero (V_{SS}). Similarly, a one in bit position 5 of the data word associated with the "Reset Output Ports Bits" command would set OPR5 to zero and, hence, the pin OP5 to a one (V_{DD}).

The CTS, RTS, CTS Enable Tx signals

CTS (Clear To Send) is usually meant to be a signal to the transmitter meaning that it may transmit data to the receiver. The CTS input is on pin MPI. The CTS signal is active low; thus, it is called CTS.

RTS is usually meant to be a signal from the receiver indicating that the receiver is ready to receive data. It is also active low and is, thus, called RTSN. RTSN is on pin MP0. A receiver's RTS output will usually be connected to the CTS input of the associated transmitter. Therefore, one could say that RTS and CTS are different ends of the same wire!

MR2(4) is the bit that allows the transmitter to be controlled by the CTS pin (MPI). When this bit is set to one AND the CTS input is driven high, the transmitter will stop sending data at the end of the present character being serialized. It is usually the RTS output of the receiver that will be connected to the transmitter's CTS input. The receiver will set RTS high when the receiver FIFO is full AND the start bit of the fourth character is sensed. Transmission then stops with four valid characters in the receiver. When MR2(4) is set to one, CTSN must be at zero for the transmitter to operate. If MR2(4) is set to zero, the MP pin will have no effect on the operation of the transmitter.

MR1(7) is the bit that allows the receiver to control MP0. When MP0 is controlled by the receiver, the meaning of that pin will be RTS. However, a point of confusion arises in that MP0 may also be controlled by the transmitter. When the transmitter is controlling this pin, its meaning is not RTS at all. It is, rather, that the transmitter has finished sending its last data byte. Programming the MP0 pin to be controlled by the receiver and the transmitter at the same time is allowed, but would usually be incompatible.

RTS can also be controlled by the commands 1000 and 1001 in the command register. RTS is expressed at the MP0 pin which is still an output port. Therefore, the state of MP0 should be set low (either by commands of the CR register or by writing to the Set Output Ports Register) for the receiver to generate the proper RTS signal. The logic at the output is basically a NAND of the MP0 bit register and the RTS signal as generated by the receiver. When the RTS flow control is selected via the MR(7) bit the state of the MP0 register is not changed. Terminating the use of "Flow Control" (via the MR registers) will return the MP0 pin to the control of the MP0 register.

Transmitter Disable Note

The sequence of instructions enable transmitter — load transmit holding register — disable transmitter will result in nothing being sent if the time between the end of loading the transmit holding register and the disable command is less that 3/16 bit time in the 16x mode or one bit time in the 1x mode. Also, if the transmitter, while in the enabled state and underrun condition, is immediately disabled after a single character is loaded to the transmit holding register, that character will not be sent.

In general, when it is desired to disable the transmitter before the last character is sent AND the TxEMT bit is set in the status register (TxEMT is always set if the transmitter has underrun or has just been enabled), be sure the TxRDY bit is active immediately before issuing the transmitter disable instruction. TxRDY sets at the end of the "start bit" time. It is during the start bit that the data in the transmit holding register is transferred to the transmit shift register.

Non-standard baud rates are available as shown in Table 6 below, via the BRG Test function.

Table 6. Baud Rate

	Normal BRG		BRG Test	
CSR[7:4]	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0000	50	75	4,800	7,200
0001	110	110	880	880
0010	134.5	38.4K	1,076	38.4K
0011	200	150	19.2K	14.4K
0100	300	300	28.8K	28.8K
0101	600	600	57.6K	57.6K
0110	1,200	1,200	115.2K	115.2K
0111	1,050	2,000	1,050	2,000
1000	2,400	2,400	57.6K	57.6K
1001	4,800	4,800	4,800	4,800
1010	7,200	1,800	57.6K	14.4K
1011	9,600	9,600	9,600	9,600
1100	38.4K	19.2K	38.4K	19.2K
1101	Timer	Timer	Timer	Timer
1110	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X
1111	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X

NOTE:
Each read on address H'2' will toggle the baud rate test mode. When in the BRG test mode, the baud rates change as shown to the left. This change affects all receivers and transmitters on the DUART. Also, the RTSN output (MP0) become the transmitter 1x clock.

The test mode at address H'2' changes all transmitters and receivers to the 1x mode and connects the output ports to some internal nodes.

Quad universal asynchronous receiver/transmitter (QUART) SC26C94

DESCRIPTION

The 26C94 quad universal asynchronous receiver/transmitter (QUART) combines four enhanced Signetics industry-standard UARTs with an innovative interrupt scheme that can vastly minimize host processor overhead. It is implemented using Signetics' high-speed CMOS process that combines small die size and cost with low power consumption.

The operating speed of each receiver and transmitter can be selected independently at one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the QUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

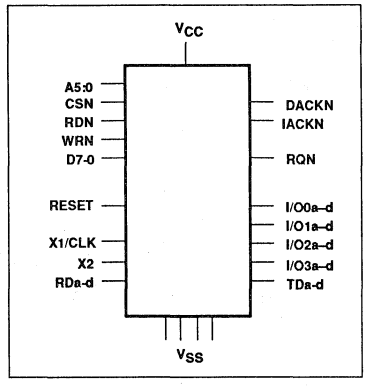
Each receiver is buffered with eight character FIFOs (first-in-first-out memories) and one shift register to minimize the potential for receiver overrun and to reduce interrupt overhead in interrupt driven systems. In addition, a handshaking capability is provided to disable a remote UART transmitter when the receiver buffer is full. (RTS control)

The 2694 provides a power-down mode in which the oscillator is stopped and the register contents are stored. This results in reduced power consumption on the order of several magnitudes. The QUART is fully TTL compatible and operates from a single +5V power supply.

FEATURES

- New low overhead interrupt control
- Four Signetics industry-standard UARTs
- Eight byte receive FIFO and eight byte transmit FIFO for each UART
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Baud rate for the receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4K baud Non-standard rates to 1.0M baud
  - User-defined rates from the programmable counter/timer associated with each of two blocks
  - External 1x or 16x clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex), automatic echo, local loop back, remote loopback
- Programmable interrupt priorities
- Identification of highest priority interrupt
- Global interrupt register set provides data from interrupting channel
- Vectored interrupts with programmable vector format
- IACKN and DTACKN signals
- Built-in baud rate generator with choice of 18 rates

PIN CONFIGURATIONS



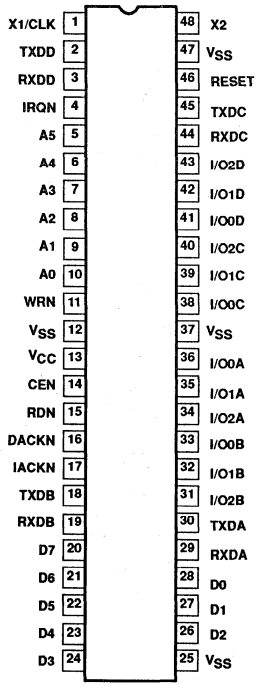
- Four I/O pins per UART for modem controls, clocks, etc.
- Power down mode
- High-speed CMOS technology
- 52-pin PLCC and 48-pin DIP
- Commercial and industrial temperature ranges available
- On-chip crystal oscillator
- TTL compatible
- Single +5V power supply with low power mode
- Two multifunction programmable 16-bit counter/timers
- 1MHz 16x mode operation
- 30ns data bus release time
- "Watch Dog" timer for each receiver

ORDERING INFORMATION

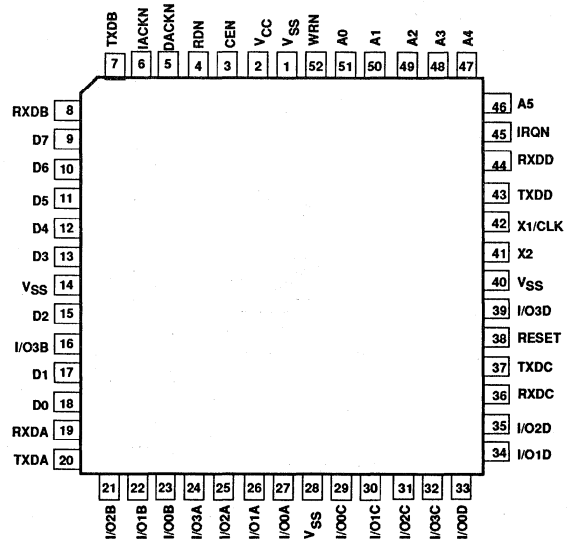
PACKAGES	V_{CC} = +5V ±10%, T_A = 0°C to +70°C	V_{CC} = +5V ±10%, T_A = –40°C to +85°C
48-Pin Plastic DIP	SC26C94C1N	SC26C94A1N
52-Pin PLCC	SC26C94C1A	SC26C94A1A

PIN CONFIGURATIONS

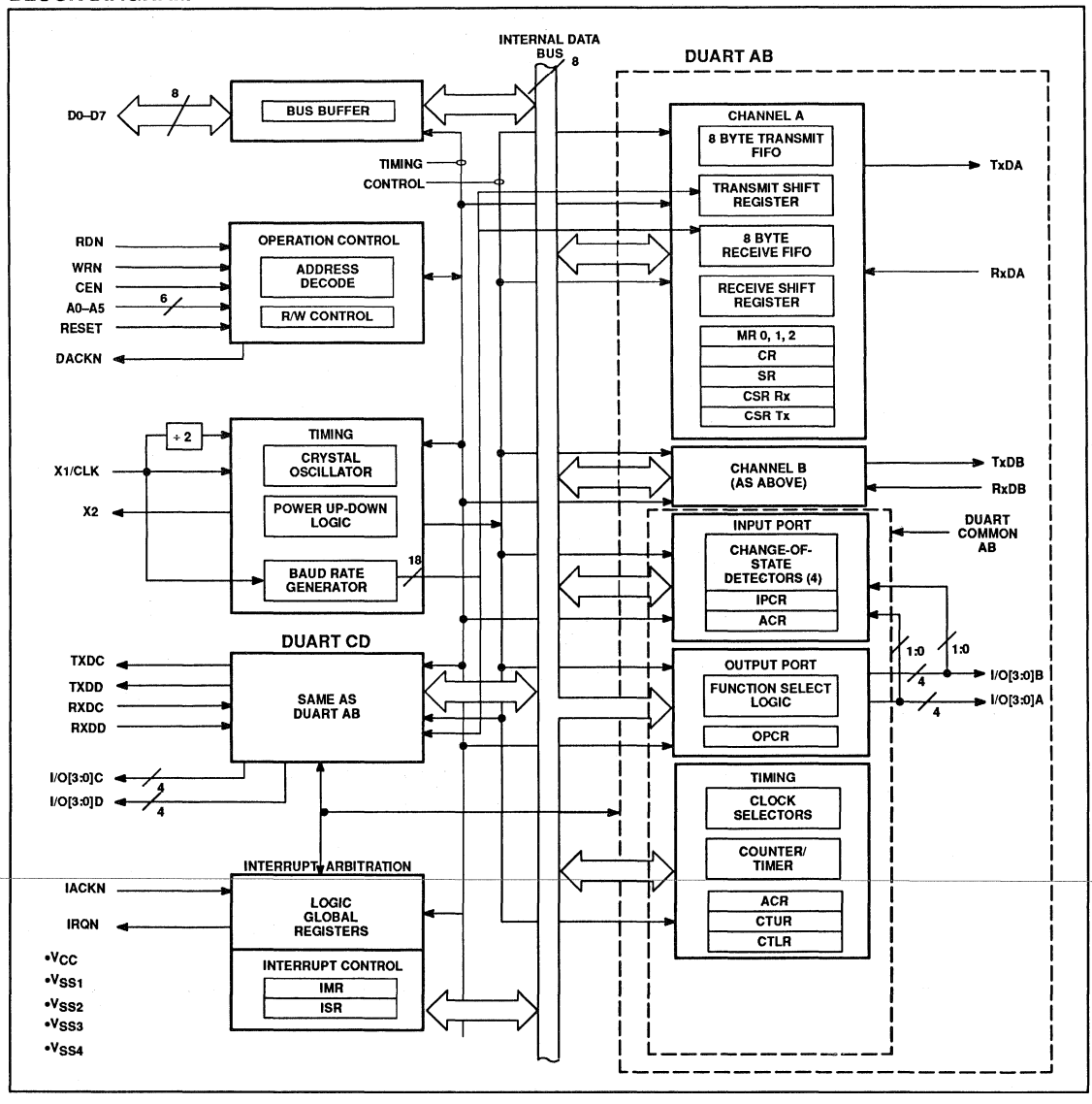
48-Pin Dual-In-Line Package



52-Pin PLCC Package



BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	TYPE	NAME AND FUNCTION
CEN	I	**Chip Select:** Active low input that, in conjunction with RDN or WRN, indicates that the host MPU is trying to access a QUART register. CEN must be inactive when IACKN is asserted.
A5:0	I	**Address Lines:** These inputs select a 26C94 register to be read or written by the host MPU.
D7:0	I/O	**8-bit Bidirectional Data Bus:** Used by the host MPU to read and write 26C94 registers.
RDN	I	**Read Strobe:** Active low input. When this line is asserted simultaneously with CEN, the 26C94 places the contents of the register selected by A5:0 on the D7:0 lines.
WRN	I	**Write Strobe:** Active low input. When this line is asserted simultaneously with CEN, the c2694 writes the data on D7:0 into the register selected by A5:0.
DACKN	O	**Data ACKnowledge:** Active low, open-drain output to the host MPU, which is asserted subsequent to a read or write operation. For a read operation, assertion of DACKN indicates that register data is valid on D7:0. For a write operation, it indicates that the data on D7:0 has been captured into the indicated register. This signal corresponds to READYN on 80x86 processors and DTACKN on 680x0 processors.
IRQN	O	**Interrupt Request:** This active low open-drain output to the host MPU indicating that one or more of the enabled UART interrupt sources has reached an interrupt value which exceeds that pre-programmed by host software. The IRQN can be used directly as a 680x0 processor input; it must be inverted for use as an 80x86 interrupt input. This signal requires an external pull-up resistor.
IACKN	I	**Interrupt ACKnowledge:** Active low input indicating that the host MPU is acknowledging an interrupt requested by this device. The 26C94 responds to the assertion of this signal by placing an interrupt vector on D7-D0 and asserting DACKN. This signal updates the CIR register in the interrupt logic.
TDa-d	O	**Transmit Data:** Serial outputs from the four UARTs.
RDa-d	I	**Receive Data:** Serial inputs to the four UARTs/
I/O0a-d	I/O	**Input/Output 0:** A multi-use input or output signal for each UART. These pins can be used as general purpose inputs, Clear to Send inputs, 1X or 16X Transmit Clock outputs or general purpose outputs. Change-of-state detection is provided for these pins.
I/O1a-d	I/O	**Input/Output 1:** A multi-use input or output signal for each UART. These pins can be used as general purpose or 1X or 16X transmit clock inputs, or general purpose 1X or 16X receive clock outputs. Change-of-state detection is provided for these pins. In addition, I/O1a and I/O1c can be used as Counter/Timer inputs and I/O1b and I/O1d can be used as Counter/Timer outputs.
I/O2a-d	I/O	**Input/Output 2:** A multi-use input or output signal for each UART. These pins can be used as general purpose inputs, 1X or 16X receive clock inputs, general purpose outputs, RTS output or 1X or 16X receive clock outputs.
I/O3a-d	I/O	**Input/Output 3:** A multi-use input or output signal for each UART. These pins can be used as general purpose inputs, 1X or 16X transmit clock inputs, general purpose outputs, or 1X or 16X transmit clock outputs.
RESET	I	**Master Reset:** Active high reset for the 26C94 logic. Must be asserted at power-up, may be asserted at other times that the system is to be reset and restarted. OSC set to divide by 1, MR pointer set to 1, DACKN enabled, I/O pins to input. Registers reset: OMR, CIR. IRQN, DTACKN, IVR Interrupt Vector, Power Down, Test registers, FIFO pointers, Baud rate generator, Error Status, Watch Dog Timers, IMR, Change of State detectors, counter/timer to timer, Transmitter and Receiver controllers.
X1/CLK	I	**Crystal 1 or Communication Clock:** This pin is normally connected to one side of a 3.6864MHz or a 7.3728MHz crystal, or can be connected to an external clock up to 8MHz.
X2	O	**Crystal 2:** If a crystal is used, this pin should be connected to its other terminal. If an external clock is applied to X1, this pin should be left unconnected.
V_{CC}, V_{SS1}, V_{SS2}, V_{SS3}, V_{SS4}		**Power and grounds:** respectively.

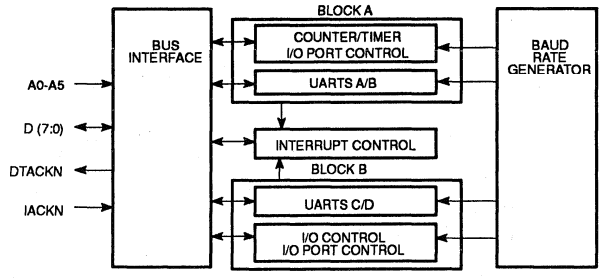


Figure 1. Channel Architecture

Table 1. QUART Registers

A5:0	READ (RDN = Low)	WRITE (WRN = Low)
000000	Mode Register a (MR0a, MR1a, MR2a)	Mode Register a (MR0a, MR1a, MR2a)
000001	Status Register a (SRa)	Clock Select Register a (CSRa)
000010	Reserved	Command Register a (CRa)
000011	Receive Holding Register a (RxFIFOa)	Transmit Holding Register a (TxFIFOa)
000100	Input Port Change Reg ab (IPCRab)	Auxiliary Control Reg ab (ACRab)
000101	Interrupt Status Reg ab (ISRab)	Interrupt Mask Reg ab (IMRab)
000110	Counter/Timer Upper ab (CTUab)	Counter/Timer Upper Reg ab (CTURab)
000111	Counter/Timer Lower ab (CTLab)	Counter/Timer Lower Reg ab (CTLRab)
001000	Mode Register b (MR0b, MR1b, MR2b)	Mode Register b (MR0b, MR1b, MR2b)
001001	Status Register b (SRb)	Clock Select Register b (CSRb)
001010	Reserved	Command Register b (CRb)
001011	Receive Holding Register b (RxFIFOb)	Transmit Holding Register b (TxFIFOb)
001100	Output Port Register ab (OPRab)	Output Port Register ab (OPRab)
001101	Input Port Register ab (IPRab)	I/OPCRa (I/O Port Control Reg a)
001110	Start Counter ab	I/OPCRb (I/O Port Control Reg b)
001111	Stop Counter ab	Reserved
010000	Mode Register c (MR0c, MR1c, MR2c)	Mode Register c (MR0c, MR1c, MR2c)
010001	Status Register c (SRc)	Clock Select Register c (CSRc)
010010	Reserved	Command Register c (CRc)
010011	Receive Holding Register c (RxFIFOc)	Transmit Holding Register c (TxFIFOc)
010100	Input Port Change Reg cd (IPCRcd)	Auxiliary Control Reg cd (ACRcd)
010101	Interrupt Status Reg cd (ISRcd)	Interrupt Mask Reg cd (IMRcd)
010110	Counter/Timer Upper cd (CTUcd)	Counter/Timer Upper Reg cd (CTURcd)
010111	Counter/Timer Lower cd (CTLcd)	Counter/Timer Lower Reg cd (CTLRcd)
011000	Mode Register d (MR0d, MR1d, MR2d)	Mode Register d (MR0d, MR1d, MR2d)
011001	Status Register d (SRd)	Clock Select Register d (CSRd)
011010	Reserved	Command Register d (CRd)
011011	Receive Holding Register d (RxFIFOd)	Transmit Holding Register d (TxFIFOd)
011100	Output Port Register cd (OPRcd)	Output Port Register cd (OPRcd)
011101	Input Port Register cd (IPRcd)	I/OPCRc (I/O Port Control Reg c)
011110	Start Counter cd	I/OPCRd (I/O Port Control Reg d)
011111	Stop Counter cd	Reserved
100000	Bidding Control Register a (BCRa)	Bidding Control Register a (BCRa)
100001	Bidding Control Register b (BCRb)	Bidding Control Register b (BCRb)
100010	Bidding Control Register c (BCRc)	Bidding Control Register c (BCRc)
100011	Bidding Control Register d (BCRd)	Bidding Control Register d (BCRd)
100100	Reserved	Power Down
100101	Reserved	Power Up
100110	Reserved	Disable DACKN
100111	Reserved	Enable DACKN
101000	Current Interrupt Register (CIR)	Reserved
101001	Global Interrupt Channel Reg (GICR)	Interrupt Vector Register (IVR)
101010	Global Int Byte Count Reg (GIBCR)	Update CIR
101011	Global Receive Holding Reg (GRxFIFO)	Global Transmit Holding Reg (GTxFIFO)
101100	Interrupt Control Register (ICR)	Interrupt Control Register (ICR)
101101	Reserved	BRG Rate. 00 = low; 01 = high
101110	Reserved	Set X1/CLK divide by two
101111	Reserved	Set X1/CLK Normal
110000–111000	Reserved	Reserved
111001	Test Mode	Test Mode
111010–111111	Reserved	Reserved

FUNCTIONAL BLOCKS

The QUART is composed of four Signetics industry–standard UARTs, each having a separate transmit and receive channel.

The Basic UART cells in the QUART are configured with 8-byte Receive FIFOs and 8-byte Transmit FIFOs. Hardware supports interrupt priority arbitration based on the number of bytes available in the transmit and receive FIFOs, counter/timers, change of state detectors, break detect or receiver error. Attempts to push a full FIFO or pop an empty FIFO do not affect the count.

Baud Rate Generator

The baud rate generator used in the QUART is the same as that used in other Signetics industry standard UARTs. It provides 18 basic Baud rates from 50 baud to 38,400 baud. It has been enhanced to provide to provide other baud rates up to 230,400 baud based on a 3.6364MHz clock. With an 8.0MHz clock rates to 500K baud. Other rates are available by setting the BRG rate to high at address 2D hex or setting Test 1 on at address 39 hex. See Table 3. These two modes are controlled by writing 00 or 01 to the addresses above. They are both set to 00 on reset. External Rx and Tx clocks yield rates to 1MHz in the 16X mode.

BLOCK DIAGRAM

As shown in the block diagram, the QUART consists of: data bus buffer, interrupt control, operation control, timing, and four receiver and transmitter channels. The four channels are divided into two different blocks, each block independent of the other.

Channel Blocks

There are two blocks (Block Diagram), each containing two sets of receiver/transmitters. In the following discussion, the description applies to Block A which contains channels a and b. However, the same information applies to all channel blocks.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the QUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The functions performed by the CPU read and write operations are shown in Table 1.

Mode registers (MR) 0, 1 and 2 are accessed via an address counter. This counter is set to one (1) by reset or a command 1x to the Command Register for compatibility with other Signetics software. It is set to 0 via a command Bx to the Command Register (CR). The address counter is incremented with each access to the MR until it reaches 2 at which time it remains at 2. All subsequent accesses to the MR will be to MR2 until the MR counter is changed by a reset or an MR counter command.

The Mode Registers control the basic configuration of the UART channels. There is one for each UART. (Transmitter/receiver pair)

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, power up/down logic and a divide by 2 selector. Closely associated with the timing block are two 16-bit counter/timers; one for each DUART.

Oscillator

The crystal oscillator operates directly from a 3.6864MHz crystal connected across the X1/CLK and X2 inputs with a minimum of external components. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. If an external clock is used instead of a crystal, X1 must be driven and X2 left floating as shown in Figure 11. The clock serves as the basic timing reference for the baud rate generator (BRG), the counter/timer, and other internal circuits. A clock frequency, within the limits specified in the electrical specifications, must be supplied even if the internal BRG is not used.

Baud Rate Generator

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. The eighteen BRG rates are grouped in two groups. Eight of the 18 are common to each group. The group selection is controlled by ACR[7]. See the Baud Rate Table 3. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The clock selectors allow the independent selection, by the receiver and transmitter, of any of these baud rates or an external timing signal.

Counter/Timer

The counter timer is a 16-bit programmable divider that operates in one of three modes: counter, timer, time out. In the timer mode it generates a square wave. In the counter mode it generates a time delay. In the time out mode it monitors the time between received characters. The C/T uses the numbers loaded into the Counter/Timer Lower Register (CTLR) and the Counter/Timer Upper Register (CTUR) as its divisor.

There are two counter/timers in the QUART; one for each block. The counter/timer clock source and mode of operation (counter or timer) is selected by the Auxiliary Control Register bits 6 to 4 (ACR[6:4]). The output of the counter/timer may be used for a baud rate and/or may be output to the I/O pins for some external function that may be totally unrelated to data transmission. The counter/timer also sets the counter/timer ready bit in the Interrupt Status Register (ISR) when its output transitions from 1 to 0.

A register read address (see Table 1) is reserved to issue a start counter/timer command and a second register read address is reserved to issue a stop command. The value of D(7:0) is ignored. The START command always loads the contents of CTUR, CTLR to the counting registers. The STOP command always resets the ISR(3) bit in the interrupt status register.

Timer Mode

In the timer mode a symmetrical square wave is generated whose half period is equal in time to division of the selected counter/timer clock frequency by the 16-bit number loaded in the CTLR CTUR. Thus, the frequency of the counter/timer output will be equal to the counter/timer clock frequency divided by twice the value of the CTUR CTLR. While in the timer mode the ISR bit 3 (ISR[3]) will be set each time the counter/timer transitions from 1 to 0. (High to low) This continues regardless of issuance of the stop counter command. ISR[3] is reset by the stop counter command. NOTE: Reading of the CTU and CTL registers in the timer mode is not meaningful.

When the C/T is used to generate a baud rate *and* the C/T is selected through the CSR then the receivers and/or transmitter will be operating in the 16x mode. Calculation for the number 'n' to program the counter timer upper and lower registers is shown below.

$$n = \frac{\text{C/T Clock Frequency}}{2 * 16 * \text{Baud rate desired}}$$

Often this division will result in a non-integer number; 26.3 for example. One can only program integer numbers to a digital divider. Therefore 26 would be chosen. This gives a baud rate error of 0.3/26.3 which is 1.14%; well within the ability of the asynchronous mode of operation.

Counter Mode

In the counter mode the counter/timer counts the value of the CTLR CTUR down to zero and then sets the ISR[3] bit and sets the counter/timer output from 1 to 0. It then rolls over to 65,365 and continues counting with no further observable effect.

Reading the C/T in the counter mode outputs the present state of the C/T. If the C/T is not

stopped, a read of the C/T may result in changing data on the data bus.

Timeout Mode

The timeout mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RxFIFO, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. If the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU will not be interrupted for the remaining characters in the RxFIFO.

By programming the C/T such that it would time out in just over one character time, the above situation could be avoided. The processor would be interrupted any time the data stream had stopped for more than one character time. NOTE: This is very similar to the watch dog time of MR0. The difference is in the programmability of the delay time and that the watchdog timer is restarted by either a receiver load to the RxFIFO or a system read from it.

This mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the timeout mode for that channel. Writing a 'Cx' to CRA or CRB will disable the timeout mode. The timeout mode should only be used by one channel at a time.

The timeout mode disables the regular START/STOP counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RxFIFO, the C/T is stopped after one C/T clock, reloaded with the value in CTUR and CTLR and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Since receiving a character restarts the C/T, the receipt of a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Timeout Mode On' command, CRx='Ax', will also clear the counter ready bit and stop the counter until the next character is received.

The counter timer is controlled with six commands: Start/Stop C/T, Read/Write Counter/Timer lower register and Read/Write Counter/Timer upper register. These commands have slight differences depending on the mode of operation. Please see the detail of the commands under the CTLR CTUR Register descriptions.

Receiver and Transmitter

The QUART has four full-duplex asynchronous receiver/transmitters. The operating frequency for the receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input.

Registers associated with the communications channel are the mode registers (MR0, MR1 and MR2) Clock Select Register (CSR), Command Register (CR), Status Register (SR), Transmit FIFO (TxFIFO), and the Receive FIFO (RxFIFO). The transmit and receive FIFOs are each eight characters deep. The receive FIFO also stores three status bits with each character.

Transmitter

The transmitter accepts parallel data from the CPU and converts it to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the TxFIFO, the TxD output remains high and the TxEMT bit in the SR will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character in the TxFIFO. In the 16X clock mode, this also re-synchronizes the internal 1X transmitter clock so that transmission of the new character begins with minimum delay.

If the transmitter is disabled it continues operating until the character currently being transmitted and any characters in the TxFIFO, including parity and stop bits, have been transmitted. New data cannot be loaded to the TxFIFO when the transmitter is disabled.

The transmitter can be forced to send a break (a continuous low condition) by issuing a START BREAK command via the CR register. The break is terminated by a STOP BREAK command or a transmitter reset..

The TxFIFO empty positions are encoded as a three bit number for presentation to the bidding logic. The coding will equal the number of bytes that remain to be filled. That is, a binary number of 101 will mean five bytes may be loaded; 111 means 7, etc. Eight positions will be indicated by a binary 111 *and* the FIFO empty bit will be set.

Receiver

The receiver accepts serial data on the RxD pin, converts the serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition, and presents the assembled character to the CPU via the receiver FIFO.

The receiver operates in two modes: the 1X and 16X. The 16X mode is the more robust of the two. It allows the receiver to establish a phase relation to the remote transmitter clock within 1/16 of a bit time and also allows validation of the start bit. The 1X mode does not validate the start bit and assumes that the receiver clock rising edge is centered in the data bit cell. The use of the 1X mode implies that the transmitter clock is available to the receiver.

When operating in the 16X mode and after the receiver has been enabled the receiver state machine will look for a high to low transition on the RxD input. The detection of this transition will cause the divider being driven by the 16X clock to be reset to zero and continue counting. When the counter reaches 7 the RxD input is sampled again and if still low a valid START BIT will be detected. If the RxD input is high at count 7 then an invalid start bit will have been sensed and the receiver will then look for another high to low transition and begin validating again.

When a valid start bit is detected the receiver state machine allows the 16X divider circuit to continue counting 0 to 15. Each time the receiver passes count 7 (the theoretical center of the bit time) another data bit is clocked into the receiver shift register until the proper number of bits have been received including the parity bit, if used, and 1/2 stop bit. After the STOP BIT is detected the receiver state machine will wait until the next falling edge of the X1 clock and then clock the assembled character and its status bits into the receiver FIFO on the next rising edge of the X1 clock. The delay from the detection of the STOP BIT to the loading of the character to the RxFIFO will be from one half to one and one half X1 clock periods. Receiver Status Register bits for FIFO READY, FIFO FULL, parity error, framing error, break detect will also set at this time. The most significant bits for data characters less than eight bits will be set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (i.e. framing error) and RxD remains low for one-half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled). The parity error, framing error and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set.

If a break condition is detected (RxD is low for the entire character including the stop bit), only one character consisting of all zeros will be loaded in the FIFO and the received break

bit in the SR is set to 1. The "Change of Break" bit in the ISR at position 2 or 6 is also set at this time. Note that the "Change of Break" bit will set again when the break condition terminates. The RxD input must return to a high condition for two successive clock edges of the 1X clock (internal or external) before a search for the next start bit begins.

NOTE: If the RxD input is low when the receiver is enabled and remains low for at least 9/16 of a bit time a valid start bit will be seen and data (probably random) will be clocked into the receiver FIFO. If the line remains low for a full character time plus a stop bit then a break will be detected.

Each receiver is equipped with a watchdog timer. This timer is enabled by MR0[7] and counts 64 RxC1X clocks. Its purpose is to alert the controlling CPU that data is in the FIFO which has not been read. This situation may occur at the end of a message when the last group of characters was not long enough to cause an interrupt.

RECEIVER FIFO

The RxFIFO consists of a first-in-first-out (FIFO) with a capacity of eight characters. Data is loaded from the receive shift register into the top-most empty position of the FIFO. The RxRDY bit in the status register (SR) is set whenever one or more characters are available to be read; a FFULL status bit is set if all eight stack positions are filled with data. The number of filled positions is encoded into a 3-bit value. This value is sent to the interrupt bidding logic where it is used to generate an interrupt. A read of the RxFIFO, outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits are 'popped' thus emptying a FIFO position for new data. **NOTE: The number of filled positions in the RxFIFO is coded as actual number filled positions. Seven filled will be coded as 7. Eight filled positions will be coded as 7 *and* the RxFIFO full status bit will be set.**

In addition to the data word, three status bits (parity error, framing error, and received break) are appended to each data character in the FIFO. Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical OR of the status for all characters coming to the top of the FIFO since the last reset error command was issued. In either mode, reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RxFIFO is read. Therefore, the SR should be read prior to reading the corresponding data character.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exists, the contents of the FIFO are not affected: the character previously in the shift register is lost and the overrun error status bit, SR[4], will be set upon receipt of the start bit of the new (overrunning) character.

A "watchdog" timer is associated with each receiver. Its interrupt is enabled by MR0[7]. The purpose of this timer is alerting the control processor that characters are in the RxFIFO which have not been read and/or the datastream has stopped. This situation may occur at the end of a transmission when the last few characters received are not sufficient to cause an interrupt.

This counter times out after 64 bit times. It is reset each time a character is transferred from the Receive shift register to the RxFIFO or a read of the RxFIFO is executed.

WAKE-UP MODE

In addition to the normal transmitter and receiver operation described above, the QUART incorporates a special mode which provides automatic "wakeup" of a receiver through address frame (or character) recognition for multi-processor or multi-station communications. This mode is selected by programming MR1[4:3] to '11'.

In this mode of operation a 'master' station transmits an address character to the several 'slave' stations on the line. The address character is identified by setting its parity bit to 1. The slave stations will usually have their receivers partially enabled as a result of setting MR1[4:3] to 11. When the receivers see a parity bit set to one they will load that character to the RxFIFO and set the RxRDY bit in the status register. The user would usually set the receiver interrupt to occur on RxRDY as well. (All characters whose parity bits are set to 0 will be ignored). The local processor at the slave station will read the 'address' character just received. The local processor will test for an address match for this station and if match occurs it will enable the local receiver and receive the following data characters. The master will normally follow an address character(s) with data characters. Since the data characters transmitted by the master will have their parity bits set to zero, stations other than the addressed one(s) will ignore the data.

NOTE: The time between address and data fields must be enough for the local processor to test the address character and enable the receiver. At bit times approaching 10µs this may begin to be a point of concern.

A transmitted character consists of a start bit, the programmed number of data and stop bits and an "address/data" bit. The parity bit is used as the address or data indicator. The polarity of the A/D bit is selected by setting MR1[2] to zero or one; zero indicates that the current byte is data, while one indicates that the current byte is addresses. The desired polarity of the A/D bit (parity) should be programmed before the TxFIFO is loaded.

While in this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character in the RxFIFO if the received A/D bit is a one, but discards the received character if the received A/D bit is a zero. If enabled, all received characters are then transferred to the CPU via the RxFIFO. In either case, the data bits are loaded in the data FIFO while the A/D bit is loaded in the status FIFO position normally used for parity error (SR[5]). Framing error, overrun error, and break detect operate normally whether or not the receiver is enabled.

INPUT OUTPUT (I/O) PINS

There are 16 multi-use pins; four for each UART. These pins are accessed and controlled via the Input Port Register (IPR), I/O Port Control Register (I/OPCR), Input Port Change Register (IPCR), and Output Port Register (OPR). They may be individually programmed to be inputs or outputs. See Table 5.

I/O0x and I/O1x pins have change of state detectors. The change of state detectors sample the input ports every 26.04µs (with the X1 clock at 3.686400MHz) and set the change bit in the IPCR if the pin has changed since it was last read. Whether the pins are programmed as inputs or outputs the change detectors still operate and report changes accordingly. See the register descriptions of the I/O ports for the detailed use of these features.

Interrupt Priority System

The interrupt control for the QUART has been designed to provide very low interrupt service overhead for the controlling processor while maintaining a high degree of flexibility in setting the importance of interrupts generated in different functional blocks of the device.

This is accomplished by allowing each function of the QUART (18 total) which may cause an interrupt to generate a variable numeric code which contains the identity of the source, channel number and severity level. This code is compared (at the X1 clock rate or the X1 clock rate divided by 2) to an interrupt threshold. When the interrupting source generates a code that is numerically greater than the interrupt threshold the IRQN is asserted

This is referred to as the bidding process. The winning bid contains, in different fields, all the characteristics of the winning bidder.

This data may be used in several ways to steer the controlling processor to the proper type and amount of service required (usually the amount of service refers to the number of bytes written to the transmitter or read from the receiver). Access to the winning bid is provided via the CIR (Current Interrupt Register), interrupt vectors, modified interrupt vectors and Global registers.

Functional Description of the Interrupt Arbitration

The QUART contains eighteen sources which may cause an interrupt:

7. Four receiver data FIFO filled functions.
8. Four receiver BREAK detect functions.
9. Four transmitter FIFO space available functions.
10. Four "Change of State" detectors.
11. Two counter/timers.

The interrupt logic at each source produces a numeric code that identifies its interrupt priority condition currently pending. This code is compared to a programmable Interrupt Threshold via the arbitration logic which determines if the IRQN should be asserted. The arbitration logic only judges those possible interrupt sources which have been allowed to bid via the IMR (Interrupt Mask Register).

The arbitration logic produces a value which is the concatenation of the channel number, interrupt type, FIFO fill level and user-defined fields. The channel number and interrupt type fields are hardwired. During the "bid arbitration" process all bids from enabled sources are presented, simultaneously, to an internal interrupt bus. The bidding system and formats are discussed in more detail in following sections.

The interrupt arbitration logic insures that the interrupt with the numerically largest bid value will be the only source driving the interrupt bus at the end of the arbitration period. The arbitration period follows the period of the X1 clock. The maximum speed is 4.0MHz. If a higher speed X1 clock is used then the X1 clock "divide by 2" feature must be used.

The value of the winning bid determined during the arbitration cycle is compared to the "Interrupt Threshold" contained in the ICR (Interrupt Control Register). If the winning bid exceeds the value of the ICR the IRQN is asserted.

Priority Arbitration and Bidding

Each of the five "types" of interrupts has slightly different "bid" value, as follows:

Receivers

# rcv'd	rEr	1	1	Chan #
3	1	1	1	2

Transmitters

0	# avail	1	0	Chan #
1	3	1	1	2

Break Detect

Programmable	1	0	0	Chan #
3	1	1	1	2

Change of State

Programmable	0	0	1	Chan #
3	1	1	1	2

Counter/Timer

Programmable	0	1	0	1	Chan #
2	1	1	1	1	2

Bits shown above as '0' or '1' are hard-wired inputs to the arbitration logic. Their presence allows determination of the interrupt type and they insure that no bid will have a value of all zeros (a condition that is indistinguishable from not bidding at all). They also serve to set a default priority among the non-receive/transmit types when the programmable fields are all zeros.

The channel number always occupies the two LSBs. Inclusion of the channel number insures that a bid value generated will be unique and that a single "winner" will drive the Interrupt Bus at the end of the arbitration interval. The channel number portion of each UARTs bid is hard-wired with UARTa being channel number 0 and so forth.

As can be seen above, bits 4:2 of the winning bid value can be used to identify the type of interrupt, including whether data was received correctly or not. Like the Channel number field, these bits are hard-wired for each interrupt source.

The "# rcv'd" and "# avail" fields indicate the number of bytes present in the receiver FIFO and the number of empty bytes in the transmitter FIFO, respectively.

NOTE: When there are zero bytes in the receiver's FIFO, it does NOT bid. Similarly, a full transmitter FIFO makes NO bid. In the case where all bids have been disabled by the Interrupt Mask Register or as a result of their byte counts, the active-low Interrupt Bus will return FFh. This value always indicates no interrupt source is active and IRQN will be negated.

The high order bit of the transmitter "bid" is always zero. An empty transmit FIFO is, therefore, fixed at a lower interrupt priority than a 1/2 full receive FIFO. Bit 4 of a receiver bid is the Receiver Error Bit (RER). The RER is the OR of the parity, framing and overrun error conditions. The RER does little to modify the priority of receiver interrupts vs. transmitter interrupts. It is output to the Interrupt Bus to allow inclusion of good data vs. problem data information in the Current Interrupt Register.

The high order bits of bids for received break, CoS (Change of State) and Counter/Timer events are all programmable. By programming ones in these fields, the associated interrupt source can be made more significant than most receiver and all transmitter interrupts. Values near zero in these fields makes them lower priority classes of interrupt.

As shown in Figure 5, the bid arbitration process is controlled by the EVAL/HOLDN signal derived from the oscillator clock.

Receipt of an IACKN signal from the host MPU latches the latest "winning bid" from the latched Interrupt Bus into the Current Interrupt Register (CIR). This logic is diagrammed in Figure 6.

If the IACKN falling edge of Figure 5 occurs during EVAL time, the result from the last arbitration (captured by the Interrupt Bus latches) is stored in CIR. Otherwise, the next EVAL pulse is inhibited and the value in the Interrupt Bus Latches is stored in CIR.

Clearing the Interrupt

Activities which change the state of the ISR will cause the IRQN to assert or negate. In addition, the accessing of a global or local RxFIFO or TxFIFO reduces the associated byte count for transmitter and receiver data interrupts. If the byte count falls below the threshold value, the interrupt request is withdrawn. Other interrupt conditions are cleared when the interrupting source is cleared.

Once the interrupt is cleared, the programmable value lowered or its byte count value reduced by one of the methods listed above, a different bidder (or no bidder at all) will win the on-going arbitration. When the winning bid drops below the Interrupt Threshold Register's value, the IRQN pin will negate.

Arbitration - Aftermath

At the end of the arbitration, i.e., the falling edge of EVAL, the winning interrupt source is driving its Channel number, number of bytes (if applicable) and interrupt type onto the Interrupt Bus. These values are captured into a latch by the trailing edge of EVAL. The output of this latch is used by the Interrupt Threshold comparator; the winning value is

captured into another set of latches called the Current Interrupt Register (CIR) at the time of an Interrupt Acknowledge cycle or execution of the "Update CIR" command.

The Current Interrupt Register and associated read logic is shown in Figure 6. Interrupting channel number and the three bit interrupt type code and FIFO fill level are readable via the Internal Data Bus.

The contents of the appropriate receiver or transmitter byte "counter", as captured at the time of IACKN assertion, make up bits 7:5 of the CIR. If the interrupt type stored in the Current Interrupt Register is not a receiver or transmitter data transfer type, the CIR7:5 field will read as the programmable fields of their respective bid formats.

The buffers driving the CIR to the DBUS also provide the means of implementing the Global Interrupting Channel and Global Byte Count Registers, described in a later section.

The winning bid channel number and interrupt type fields can also be used to generate part of the Interrupt Vector, as defined by the Interrupt Control Register.

Interrupt Context

The channel number of the winning "bid" is used by the address decoders to provide data from the interrupting UART channel via a set of Global pseudo-registers. The interrupt Global pseudo-registers are:

1. Global Interrupting Byte Count
2. Global Interrupting Channel
3. Global Receive Holding Register
4. Global Transmit Holding Register

The first two Global "registers" are provided by Current Interrupt Register fields as shown in Figure 6. The interrupting channel number latched in CIR modifies address decoding so that the Receive or Transmit Holding Register for the interrupting channel is accessed during I/O involving the Global Receive and Transmit Holding Registers. Similarly, for data interrupts from the transmitter and receiver, the number of characters available for transfer to the CPU or the number of transmit FIFO positions open is available by reading the Global Interrupt Byte Count Register. For non-data interrupts, a read of the Global Interrupt Byte Count Register yields a value equal to the highest programmable filed.

In effect, once latched by an IACK or the Update CIR command, the winning interrupt channel number determines the contents of the global registers. All Global registers will provide data from the interrupting UART channel.

Interrupt Threshold Calculation

The state of IRQN is determined by comparison of the winning "bid" value to the Interrupt Threshold field of the Interrupt Control Register.

The logic of the bidding circuit is such that when no interrupt source has a value greater than the interrupt threshold then the interrupt is not asserted and the CIR (Current Interrupt Register) is set to all ones. When one or more of the 18 interrupt sources which are enabled via the IMR (Interrupt Mask Register) exceed the threshold then the interrupt threshold is effectively disconnected from the bidding operation while the 18 sources now bid against each other. The final result is that the highest bidding source will disable all others and its value will be loaded to the CIR and the IRQN pin asserted low. This all occurs during each cycle of the X1,X2 crystal clock.

INTERRUPT NOTE ON 26C94:

For the receivers and transmitters, the bidding of any particular unit may be held off unless one of four FIFO fill levels is attained. This is done by setting the RxINT and TxINT bits in MR0 and MR1 to non-zero values. This may be used to prevent a receiver or transmitter from generating an interrupt even though it is filed above the bid threshold. Although this is not in agreement with the idea that each enabled interrupt source bid with equal authority, it does allow the flexibility of giving particular receiver or transmitters more interrupt importance than others.

This may be used when the Interrupt Threshold is set at or above 100000. Note than in this case the transmitter cannot generate an interrupt. If the interrupt threshold MSBs were set to 011 *and* the 'Receiver Interrupt Bits' on the MR registers set to a value other than 00 then the RxFIFO could not generate and interrupt until it had 4, 6 or 8 bytes. This in effect partially defeats the hardwired characteristic that the receiver interrupts should have more importance than the transmitter. This characteristic has been implemented by setting the MSB of the transmitter bid to zero.

RECEIVER INPUT FILL LEVEL

MR0[6]	MR1[6]	Interrupt Condition
0	0	1 or more bytes in FIFO (Rx RDY) default
0	1	6 or more bytes in FIFO
1	0	4 or more bytes in FIFO
1	1	8 or more bytes in FIFO (Rx FULL)

MR0[5:4] – Tx Interrupt fill level

MR0[5]	MR0[4]	Interrupt Condition
0	0	8 bytes empty (Tx EMPTY) default
0	1	4 or more bytes empty
1	0	6 or more bytes empty
1	1	1 or more bytes empty (Tx RDY)

Vectored Interrupts

The QUART responds to an Interrupt Acknowledge (IACK) initiated by the host MCU by providing an Interrupt Acknowledge Vector on D7:0. The interrupt acknowledge cycle is terminated with a DACKN pulse. The vector provided by the QUART can have one of the three forms under control of the IVC control field (bits 1:0 of the Interrupt Control Register):

With IVC = 00 (IVR only)

IVR7:0
8

With IVC = 01 (channel number)

IVR7:2	Chan #
6	2

With IVC = 10 (type & channel number)

IVR7:5	Type	Chan #
3	3	2

A code of 11 in the Interrupt Vector Control Field of the ICR results in NO interrupt vector being generated. The external data bus will be held in a high impedance state throughout the IACK cycle. A DACKN will be generated normally for the IACK cycle, however.

NOTE: If IACKN is not being used then the command "UPDATE CIR" must be issued for the global and interrupt registers to be updated.

PROGRAMMING UART CONTROL REGISTERS

The operation of the QUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. Addressing of the registers is described in Table 1.

The bit formats of the QUART registers are depicted in Table 2.

Table 2. Register Bit Formats, Duart ab. [duplicated for Duart cd]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

MR0 (Mode Register 0)

Rx Watchdog Timer	RxINT2 bit	TxINT Control	These bits not implemented. They should be considered Reserved.			
0 = off 1 = on	These bits should normally be set to 0		x	x	x	x

MR1 (Mode Register 1)

RxRTS Control	RxINT1 Select	Error Mode	Parity Mode	Parity Type	Bits per Character
0 = No 1 = Yes	Normally set to 0	0 = Char 1 = Block	00 = With parity 01 = Force parity 10 = No parity 11 = Special mode	0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8

MR2 (Mode Register 2)

Channel Mode	TxRTS Control	CTS Enable Tx	Stop Bit Length*
00 = Normal 01 = Auto-echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 4 = 0.813 8 = 1.563 C = 1.813 1 = 0.625 5 = 0.875 9 = 1.625 C = 1.875 2 = 0.688 6 = 0.938 A = 1.688 E = 1.938 3 = 0.750 7 = 1.000 B = 1.750 F = 2.000

NOTE:
13. Add 0.5 to values shown above for 0–7, if channel is programmed for 5 bits/char.

CSR (Clock Select Register)

Receiver Clock Select	Transmitter Clock Select
See text	See text

CR (Command Register)

Miscellaneous Commands	Disable Tx	Enable Tx	Disable Rx	Enable Rx
See text	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
14. Issuing commands contained in the upper four bits of the "Command Register" should be separated in time by at least three (3) X1 clock edges. Allow four (4) edges if the "X1 clock divide by 2" mode is used.

SR (Status Register)

Rec'd. Break	Framing Error	Parity Error	Overrun Error	TxEMT	TxRDY	FFULL	RxRDY
0 = No 1 = Yes *	0 = No 1 = Yes *	0 = No 1 = Yes *	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
15. These status bits are appended to the corresponding data character in the receive FIFO. A read of the status register provides these bits [7:5] from the top of the FIFO together with bits [4:0]. These bits are cleared by a reset error status command. Unless reset with the 'Error Reset' (CR command 40) or receiver reset, these bits will remain active in the Status Register after the RxFIFO is empty.

Table 2. Register Bit Formats, Duart ab. [duplicated for Duart cd] (continued)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

ACR (Auxiliary Control Register)

BRG Set Select	Counter/Timer Mode and Source		Delta I/O1b	Delta I/O0b	Delta I/O1a	Delta I/O0a
0 = set 1 1 = set 2	See text		0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on

IPCR (Input Port Change Register)

Delta I/O1b	Delta I/O0b	Delta I/O1a	Delta I/O0a	I/O1b	I/O0b	I/O1a	I/O0a
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

ISR (Interrupt Status Register)

I/O Port Change	Delta BREAKb	RxRDY/ FFULLb	TxRDYb	Counter Ready	Delta BREAKa	RxRDY/ FFULLa	TxRDYa
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

IMR (Interrupt Mask Register)

I/O Port Change INT	Delta BREAKb INT	RxRDY/ FFULLb INT	TxRDYb INT	Counter Ready INT	Delta BREAKa INT	RxRDY/ FFULLa INT	TxRDYa INT
0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on

CTUR (Counter/Timer Upper Register)

C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]

CTUR (Counter/Timer Lower Register)

C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]

IPR (Input Port Register)

I/O3b	I/O2b	I/O3a	I/O2a	I/O1b	I/O0b	I/O1a	I/O0a
0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

Mode Registers 0, 1 and 2

The addressing of the Mode Registers is controlled by the MR Register pointer. On any access to the Mode Registers this pointer is always incremented. Upon reaching a value of 2 it remains at 2 until changed by a CR command or a hardware reset.

MR0 – Mode Register 0

Mode Register 0 (MR0) is part of the UART configuration registers. It controls the watch dog timer and the encoding of the number of characters received in the RxFIFO. The lower four bits of this register are not implemented in the hardware of the chip. MR0 is normally set to either 80h or 00h. A read of this register will return 1111 (Fh) in the lower four bits.

The MR0 register is accessed by setting the MR Pointer to zero (0) via the command register command 1011 (Bh).

MR0[7]: This bit enables or disables the RxFIFO watch dog timer.

MR0[7] = 1 enable timer

MR0[7] = 0 disable timer

MR0[6:4]: These bits are normally set to 0 except as noted in the "Interrupt Threshold Calculation" description

MR0[3:0]: These bits are not implemented in the chip. These bits should be be considered "reserved."

MR1 – Mode Register 1

MR1 is accessed when the MR pointer points to MR1. The pointer is set to MR1 by RESET, a set pointer command applied via the CR or after an access to MR0. After reading or writing MR1, the pointers are set at MR2.

MR1[7] – Receiver Request-to-Send Flow Control

This bit controls the deactivation of the RTSN output (I/O2x) by the receiver. This output is manually asserted and negated by commands applied via the command register. MR1[7] = 1 causes RTSN to be automatically negated upon receipt of a valid start bit if the

receiver FIFO is full. RTSN is re-asserted when an empty FIFO position is available. This feature can be used to prevent overrun in the receiver by using the RTSN output signal to control the CTS input (the QUART I/O0 pin) of the transmitting device.

Use of this feature requires the I/O2 pin to be programmed as output via the I/OPCR and to be driving a 0 via the OPR. When the RxFIFO is full and the start bit of the ninth character is sensed the receiver logic will drive the I/O2 pin high. This pin will return low when another RxFIFO position is vacant.

MR1[6] – Receiver Interrupt Select 1
This bit is normally set to 0 except as noted in the "Interrupt Threshold Calculation" description. MR1[6] operates with MR0[6] to prevent the receiver from bidding until a particular fill level is attained. For software compatibility this bit is designed to emulate the RxFIFO interrupt function of previous Signetics UARTs.

MR1[5] – Error Mode Select
This bit selects the operating mode of the eight FIFOed status bits (FE, PE, received break). In the character mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO.

In the block mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last reset error command was issued.

In the "Block Error" mode the ORing of the error status bits and the presentation of them to the status register takes place as the bytes enter the RxFIFO. This allows an indication of problem data when the error occurs after the leading bytes have been received. In the character mode the error bits are presented to the status register when the corresponding byte is at the top of the FIFO.

MR1[4:3] – Parity Mode Select
If "with parity" or "force parity" is selected, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR1[4:3] = 11 selects the channel to operate in the special wake-up mode (see page 10).

MR1[2] – Parity Type Select
This bit selects the parity type (odd or even) if the "with parity" mode is programmed by MR1[4:3], and the polarity of the forced parity bit if the "force parity" mode is programmed. It has no effect if the "no parity" mode is programmed. In the special "wake-up" mode, it selects the polarity of the transmitted A/D bit.

MR1[1:0] – Bits per Character Select
This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2 – Mode Register 2

MR2 is accessed when the channel MR pointer points to MR2, which occurs after any access to MR1. Accesses to MR2 do not change the pointer.

MR2[7:6] – Mode Select
The QUART can operate in one of four modes. MR2[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is re-clocked and retransmitted on the TxD output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e., transmitted parity bit is as received.

Two diagnostic modes can also be selected. MR2[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxD output is held high.
4. The RxD input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2[7:6] = 11. In this mode:

1. Received data is re-clocked and retransmitted on the TxD output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., the transmitted parity bit is as received.
5. The receiver must be enabled, but the transmitter need not be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected, the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes; if the deselection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop bit has been retransmitted.

MR2[5] – Transmitter Request-to-Send Control

NOTE: When the transmitter controls the I/O2 pin (usually used for the RTSN signal) the meaning of the pin is not RTSN at all! Rather it signals that the transmitter has finished transmission. (i.e., end of block).

This bit controls the deactivation of the RTSN output (I/O2) by the transmitter. This output is manually asserted and negated by appropriate commands issued via the command register. MR2[5] = 1 causes RTSN to be reset automatically one bit time after the characters in the transmit shift register and in the TxFIFO (if any) are completely transmitted (includes the programmed number of stop bits if the transmitter is not enabled). This feature can be used to automatically terminate the transmission as follows:

1. Program auto-reset mode: MR2[5] = 1.
2. Enable transmitter.
3. Assert RTSN via command.
4. Send message.
5. Verify the next to last character of the message is being sent by waiting until transmitter ready is asserted. Disable transmitter after the last character of the message is loaded in the TxFIFO.
6. The last character will be transmitted and RTSN will be reset one bit time after the last stop bit.

MR2[4] – Transmitter Clear-to-Send Flow Control
The sate of this bit determines if the CTSN input (I/O0) controls the operation of the transmitter. If this bit is 0, CTSN has no effect on the transmitter. If this bit is a 1, the transmitter checks the sate of CTSN each time it is ready to send a character. If it is asserted (Low), the character is transmitted. If it is negated (High), the TxD output remains in the marking state and the transmission is delayed until CTSN goes Low. Changes in CTSN, while a character is being transmitted do not affect the transmission of that character. This feature can be used to prevent overrun of a remote receiver.

MR2[3:0] – Stop Bit Length Select
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1–9/16 to 2 bits, in increments of 1/16 bit, can be programmed

for character lengths of 6, 7, and 8 bits. For a character length of 5 bits, 1–1/16 to 2 stop bits can be programmed in increments of 1/16 bit. If an external 1X clock is used for the transmitter, MR2[3] = 0 selects one stop bit and MR2[3] = 1 selects two stop bits to be transmitted.

RECEIVER NOTE: In all cases, the receiver only checks for a "mark" condition at the center of the stop bit (1/2 to 9/16 bit time into the stop bit position). At this time the receiver has finished processing the present character and is ready to search for the start bit of the next character.

CSR – Clock Select Register

CSR[7:4] – Receiver Clock Select
When using a 3.6864MHz crystal or external clock input, this field selects the baud rate clock for the receiver as shown in Table 3.

The receiver clock is always a 16X clock, except for CSR[7:4] = 1111. I/O2x is external input.

CSR[3:0] – Transmitter Clock Select
This field selects the baud rate clock for the transmitter. The field definition is as shown in Table 3, except as follows:

CSR[3:0]	ACR[7] = 0	ACR[7] = 1
1 1 1 0	I/O3x – 16X	I/O3x – 16X
1 1 1 1	I/O3x – 1X	I/O3x – 1X

Table 3. Baud Rate

	BRG RATE = LOW		BRG RATE = HIGH		TEST 1 = 1	
CSR[7:4]	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0 0 0 0	50	75	50	450	4,800	7,200
0 0 0 1	110	110	110	110	880	880
0 0 1 0	134.5	38.4k	134.5	230.4K	1,076	38.4K
0 0 1 1	200	150	200	900	19.2K	14.4K
0 1 0 0	300	300	1800	1,800	28.8K	28.8K
0 1 0 1	600	600	3,600	3,600	57.6K	57.6K
0 1 1 0	1,200	1,200	7,200	7,200	115.2K	115.2K
0 1 1 1	1,050	2,000	1,050	2,000	1,050	2,000
1 0 0 0	2,400	2,400	14.4K	14.4K	57.6K	57.6K
1 0 0 1	4,800	4,800	28.8K	28.8K	4,800	4,800
1 0 1 0	7,200	1,800	7,200	1,800	57.6K	14.4K
1 0 1 1	9,600	9,600	57.6K	57.6K	9,600	9,600
1 1 0 0	38.4k	19.2k	230.4K	115.2K	38.4K	19.2K
1 1 0 1	Timer	Timer	Timer	Timer	Timer	Timer
1 1 1 0	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X
1 1 1 1	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X

CR – Command Register

CR is used to write commands to the QUART.

CR[7:4] – Miscellaneous Commands
Issuing commands contained in the upper four bits of the "Command Register" should be separated in time by at least three (3) X1 clock edges. Allow four (4) edges if the "X1 clock divide by 2" mode is used. The encoded value of this field can be used to specify a single command as follows:

0000 No command.

0001 Reset MR pointer. Causes the MR pointer to point to MR1.

0010 Reset receiver. Resets the receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO pointer is reset to the first location.

0011 Reset transmitter. Resets the transmitter as if a hardware reset had been applied.

0100 Reset error status. Clears the received break, parity error, framing error, and overrun error bits in the status register (SR[7:4]). Used in character mode to clear OE status (although RB, PE, and FE bits will also be cleared), and in block mode to clear all error status after a block of data has been received.

0101 Reset break change interrupt. Causes the break detect change bit in the interrupt status register (ISR[2 or 6]) to be cleared to zero.

0110 Start break. Forces the TxD output low (spacing). If the transmitter is empty, the start of the break condition will be delayed up to two bit times. If the transmitter is active, the break begins when transmission of the character is completed. If a character is in the TxFIFO, the start of break is delayed until that character or any others loaded after it have been transmitted (TxEMT must be true before break begins). The transmitter must be enabled to start a break

0111 Stop break. The TxD line will go high (marking) within two bit times. TxD will remain high for one bit time before the next character, if any, is transmitted.

1000 Assert RTSN. Causes the RTSN output to be asserted (Low).

1001 Negate RTSN. Causes the RTSN output to be negated (High).

1010 Set Timeout Mode On. The register in this channel will restart the C/T as each receive character is transferred from the shift register to the RxFIFO. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset.

1011 Set MR Pointer to 0.

1100 Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued.

1101 Reserved.

111x Reserved for testing.

CR[3] – Disable Transmitter
This command terminates transmitter operation and resets the TxRDY and TxEMT status bits. However, if a character is being transmitted or if a character is in the TxFIFO

when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CR[2] – Enable Transmitter
Enables operation of the transmitter. The TxRDY and TxEMT status bits will be asserted.

CR[1] – Disable Receiver
This command terminates operation of the receiver immediately – a character being received will be lost. However any unread characters in the RxFIFO area are still available. Disable is not the same as a "receiver reset". With a receiver reset any characters not read are lost. The command has no effect on the receiver status bits or any other control registers. If the special wake–up mode is programmed, the receiver operates even if it is disabled (see Wake-up Mode).

CR[0] – Enable Receiver
Enables operation of the receiver. If not in the special wake-up mode, this also forces the receiver into the search for start bit state.

SR – Channel Status Register

SR[7] – Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received; further entries to the FIFO are inhibited until the RxDA line returns to the marking state for at least one-half bit time (two successive edges of the internal or external 1x clock).

When this bit is set, the change in break bit in the ISR (ISR[6 or 2]) is set. ISR[6 or 2] is also set when the end of the break condition, as defined above, is detected. The break detect circuitry is capable of detecting breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must last until the end of the next character in order for it to be detected.

SR[6] – Framing Error (FE)
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SR[5]– Parity Error (PE)
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity. In special 'wake-up mode', the parity error bit stores the received A/D (Address/Data) bit.

SR[4] – Overrun Error (OE)
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost. This bit is cleared by a reset error status command.

SR[3] – Transmitter Empty (TxEMT)
This bit will be set when the transmitter underruns, i.e., both the TxFIFO and the transmit shift register are empty. This bit and TxRDY are set when the transmitter is first enabled and any time it is re-enabled after either, (a) reset, or (b) the transmitter has assumed the disabled state. It is set after transmission of the last stop bit of a character, if no character is in the TxFIFO awaiting transmission. It is reset when the TxFIFO is loaded by the CPU, a pending transmitter disable is executed, the transmitter is reset, or the transmitter is disabled in the underrun condition.

SR[2] – Transmitter Ready (TxRDY)
This bit, when set, indicates that the TxFIFO has at least one empty location that may be loaded by the CPU. It sets when the transmitter is first enabled. It is cleared when the TxFIFO is full (eight bytes); the transmitter is reset; a pending transmitter disable is executed; the transmitter is disabled when it is in the underrun condition. When this bit is **not** set characters written to the TxFIFO will not be loaded or transmitted; they are lost.

SR[1] – RxFIFO Full (FFULL)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all eight FIFO positions are occupied. It is reset when the CPU reads the FIFO and there is no character in the receive shift register. If a character is waiting in the receive shift register because the FIFO is full, FFULL is not reset after reading the FIFO once.

SR[0] – RxFIFO Ready (RxRDY)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RxFIFO, and no more characters are in the FIFO.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects between two sets of baud rates that are available within each baud rate group generated by the BRG. See Table 3.

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.

Set 2: 75, 110, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, 19.2k, and 38.4k baud.

The selected set of rates is available for use by the receiver and transmitter.

ACR[6:4] – Counter/Timer Mode and Clock Source Select
This field selects the operating mode of the counter/timer and its clock source (see Table 4).

The I/O pins available for counter/timer clock source is I/O1a and I/O1c. The counter/timer clock selection is connected to the I/O1 pin and will accept the signal on this pin regardless of how it is programmed by the I/OPCR. (see Figure 2).

Table 4. ACR[6:4] C/T Clock and Mode Select

[6:4]	Mode	Clock Source
0 0 0	Counter	I/O1 pin
0 0 1	Counter	I/O1 pin divided by 16
0 1 0	Counter	TxC–1X clock of the transmitter
0 1 1	Counter	Crystal or external clock (X1/CLK) divided by 16
1 0 0	Timer	I/O1 pin
1 0 1	Timer	I/O1 pin divided by 16
1 1 0	Timer	Crystal or external clock (X1/CLK)
1 1 1	Timer	Crystal or external clock (X1/CLK) divided by 16

ACR[3:0] – I/O1b, I/O0b, I/O1a, I/O0a Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register, ISR[7], to be set and thus allow the Change of State Detectors to enter the bidding process. If a bit is in the 'on' state, the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which may result in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7:4] – I/O1b, I/O0b, I/O1a, I/O0a Change-of-State
These bits are set when a change of state, as defined in the Input Port section of this data sheet, occurs at the respective pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – I/O1b, I/O0b, I/O1a, I/O0a Change-of-State
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR – Interrupt Status Register

Important: The setting of these bits and those of the IMR are essential to the interrupt bidding process.

This register provides the status of all potential interrupt sources. The contents of this register are masked by the interrupt mask register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', then the interrupt source represented by this bit is allowed to enter the interrupt arbitration process. It will generate an interrupt (the assertion of INTRN low) only if its bid exceeds the interrupt threshold value. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR; the true status is provided regardless of the contents of the IMR.

ISR[7] – I/O Change-of-State
This bit is set when a change-of-state occurs at the I/O1b, I/O0b, I/O1a, I/O0a input pins. It is reset when the CPU reads the IPCR.

ISR[6] – Channel b Change in Break
This bit, when set, indicates that the receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a reset break change interrupt command.

ISR[5] – Receiver Ready or FIFO Full Channel b
Normally the ISR[5] bit being set to one indicates the RxFIFO is filled with one or more bytes and/or the receiver watch dog timer (when enabled) has timed out.

The meaning of ISR[5] is controlled by the MR0[6] and MR1[6] bits which are normally set to 00. The ISR[5] bit setting to one allows the receiver to present its bid to the arbitration logic. This function is explained in the "Interrupt Note On 26C94" and under the "Receiver Interrupt Fill Level".

ISR[5], if set, will reset when the RxFIFO is read. If the reading of the FIFO does not reduce the fill level below that determined by the MR bits, then ISR[5] sets again within two X1 clock times. Further, if the MR fill level is set at 8 bytes AND there is a byte in the receiver shift register waiting for an empty FIFO location, then a read of the RxFIFO will cause ISR[5] to reset. It will immediately set again upon the transfer of the character in the shift register to the FIFO.

ISR[4] – Transmitter Ready Channel b
The function of this bit is programmed by MR0[5:4] (normally set to 00). This bit is set when ever the number of empty TxFIFO positions exceeds or equals the level programmed in the MR0 register. This condition will almost always exist when the transmitter is first enabled. It will reset when the empty TxFIFO positions are reduced to a level less than that programmed in MR0[5:4] or the transmitter is disabled or reset.

The ISR[4] bit will reset with each write to the TxFIFO. If the write to the FIFO does not bring the FIFO above the fill level determined by the MR bits, the ISR[4] bit will set again within 2 X1 clock times.

NOTE: The setting of ISR[4] is necessary for the transmitter to generate an interrupt. It does **not** mean the transmitter **is** generating an interrupt.

ISR[3] – Counter Ready
In the counter mode of operation, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command. It is initialized to '0' when the chip is reset.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time the C/T reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the C/T.

ISR[2] – Channel a Change in Break
This bit, when set, indicates that the receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a reset break change interrupt command.

ISR[1] – Receiver Ready or FIFO Full Channel a
See the description of ISR[5]. The channel 'a' receiver operation is the same as channel 'b'.

ISR[0] – Transmitter Ready Channel a
See the description of ISR[4]. Channel "a" transmitter operates in the same manner as channel "b."

IMR – Interrupt Mask Register

The programming of this register selects which interrupt sources will be allowed to enter the interrupt arbitration process. This register is logically ANDED with the interrupt status register. Its function is to allow the interrupt source it represents to join the bidding process if the corresponding IMR and ISR bits are both 1. It has no effect on the value in the ISR. It does not mask the reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is H'0002'. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half-periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read address at A5–A0 0Eh for C/T ab or read address 1Eh for C/T cd). After this, while in timer mode, the C/T will run continuously. Receipt of a subsequent start counter command causes the C/T to terminate the current timing cycle and to begin a new cycle using the values in the CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a "Stop Counter" command (read address at A5–A0 0Fh for C/T ab or read address 1Fh for C/T cd). The command, however, does not stop the C/T. It only resets the ISR[3] bit; the C/T continues to run. The ISR[3] bit will set again as the counter passes through 0. The generated square wave is output on an I/O pin if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded in CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching the terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set. The counter rolls over to 65535 and continues counting until stopped by the CPU. If I/O is programmed to be the output of the C/T, the output remains High until the terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command. If new values have not been loaded, the previous values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower eight bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower eight bits to the upper eight bits occurs between the times that both halves of the counter is read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

I/O LOGIC

The QUART has four I/O pins for each channel. These pins may be individually programmed as an input or output under control of the I/OPCR (I/O Port Control Register). Functions which may use the I/O pins as inputs (Rx or Tx external clock, for example) are always sensitive to the signal on the I/O pin regardless of it being programmed as an input or an output. For example if I/O1a was programmed to output the RxC1X clock and the Counter/Timer was programmed to use I/O pin as its clock input the result would be the Counter/Timer being clocked by the RxC1X clock.

The 16 I/O ports are accessed and/or controlled by five (5) registers: IPR, ACR, I/OPCR, IPCR, OPR. They are shown in Table 5 of this document. Each UART has four pins. Two of these pins have "Change of State Detectors" (COS). These detectors set whenever the pin to which they are attached changes state. (1 to 0 or 0 to 1) The "Change of State Detectors" are enabled via the ACR. When enabled the COS devices may generate interrupts via the IMR and IPCR registers. Note that when the COS interrupt is enabled that any one or more of the four COS bits in the IPCR will enable the COS bidding. Each of the channel's four I/O lines are configured as inputs on reset.

The Change of State detectors sample the I/O pins at the rate of the 38.4KHz clock. A change on the pin will be required to be stable for at least 26.04µs and as much as 52.08µs for the COS detectors to confirm a change. Note that changes in the X1/clock frequency will effect this stability requirement.

Table 5.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

IPCR (Input Port Change Register ab) The lower four bits replicate the lower four bits of the IPR. The upper four bits reads state of Change detectors. Change detectors are enabled in ACR[3:0]. (DUART ab)

Delta I/O1b	Delta I/O0b	Delta I/O1a	Delta I/O0a	I/O1b	I/O0b	I/O1a	I/O0a
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

IPCR (Input Port Change Register cd) The lower four bits replicate the lower four bits of the IPR. The upper four bits reads state of Change detectors. Change detectors are enabled in ACR[3:0]. (DUART cd)

Delta I/O1d	Delta I/O0d	Delta I/O1c	Delta I/O0c	I/O1d	I/O0d	I/O1c	I/O0c
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

I/OPCR (I/O Port Configuration Register) One register for each UART.

I/O3x CONTROL	I/O2x CONTROL	I/O1x CONTROL	I/O0x CONTROL
Two bits for each I/O pin. See Figure 2.			

This register controls the configuration of the I/O ports. It defines them as inputs or outputs and controls what sources will drive them in the case of outputs or which functions they will drive when used as an input. Each pin has four functions and hence two bits to control it. Each UART has one eight bit register to control its four I/O ports.

OPR (Output Port Register cd) for DUART cd

I/O3d	I/O2d	I/O3c	I/O2c	I/O1d	I/O0d	I/O1c	I/O0c
One bit for each pin. When I/O pins are configured as "General Purpose Outputs" the pins will be driven to the complement value of its associated OPR bit.							

OPR (Output Port Register ab) for DUART ab

I/O3a	I/O2b	I/O3a	I/O2a	I/O1b	I/O0b	I/O1a	I/O0a
One bit for each pin. When I/O pins are configured as "General Purpose Outputs" the pins will be driven to the complement value of its associated OPR bit.							

This register contains the data for the I/O ports when they are used as 'General Purpose Outputs'. The bits of the register are controlled by writing to the hex addresses at 0C and 1C. Ones written to the OPR drive the pins to 0; zeros drive the pins to 1. (The pins drive the value of the complement data written to the OPR)

IPR (Input Port Register cd) Reads I/O pins for DUART cd

I/O3d	I/O2d	I/O3c	I/O2c	I/O1d	I/O0d	I/O1c	I/O0c
0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

IPR (Input Port Register ab) Reads I/O pins for DUART ab

I/O3a	I/O2b	I/O3a	I/O2a	I/O1b	I/O0b	I/O1a	I/O0a
0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

This register reads the state of the 'I/O Ports'. The state of the I/O ports is read regardless of being programmed as inputs or outputs. The IPR can be thought of a just another 8 bit parallel port to the system data bus. The lower four bits of this register are replicated in the lower four bits of the IPCR register.

I/OPCR7	I/OPCR6	I/OPCR5	I/OPCR4	I/OPCR3	I/OPCR2	I/OPCR1	I/OPCR0
I/O3x Control		**I/O2x Control**		**I/O1x Control**		**I/O0x Control**	
00 = GPI or TxC in 01 = OPR3 out 10 = TxC16X out 11 = TxC1X out		00 = GPI or RxC in 01 = OPR2 (Note 1) 10 = RxC1X out 11 = RxC16X out		00 = C/T in (Note 2) 01 = OPR1 out 10 = (Note 3) 11 = RxC1X out		00 = GPI or CTS in 01 = OPR0 out 10 = TxC1X out 11 = TxC16X out	

Note 1: Bit 2 of the OPR is the Request to Send function that is affected by the Assert and Negate RTS commands in CRA or CRB, and by the TxRTS feature if MR2x5 is 1, as well as by writing OPR. The RxRTS function, which is activated if MR1x7 is 1, does not affect OPR2 but merely blocks the output signal whenever the Rx FIFO is full.

Note 2: Similar to the other three pins, a 00 value in this field makes the I/O1 pin an input. I/O1 can always be used as a General Purpose Input (GPI). I/O1a and I/O1c can be used as CTI depending on how ACR6:4 is programmed. If O/PCR[7:6] is not 00, I/O1 can be used as TxC depending on how CSRx[3:0] is programmed.

Note 3: A 10 value in this field makes I/O1b and I/O1d output the C/T signal, and makes I/O1a and I/O1c output RxC16x.

Figure 2. I/OPCR Control of I/O3:0 Pins for Each Channel.

Registers of the Interrupt System

The CIR, and "Global" registers are updated with the IACKN signal or from the "Update CIR" command at hex address 2A. These registers are not updated when IRQN is asserted since there could be a long time between the assertion of IRQN and the start of the interrupt service routine. (See notes following this section).

Current Interrupt Register (CIR)

# Bytes	Type	Chan #
3	3	2

The Channel # field indicates which of the four UARTs has the highest priority interrupt currently outstanding, while the Type field indicates its source within the UART. The Type field is encoded as follows:

000 No Interrupt
001 Change of State
x10 Transmit available
011 Receive available, no error
100 Receiver break change
101 Counter/Timer
111 Receive available, w/errors

With Type = x11, the # Bytes field indicates the count of received bytes available for reading, while with Type = x10 it indicates the number of bytes that can be written to the transmit FIFO.

The CIR is Read only at address 28H.

Global Interrupt Byte Count (GIBC)

00000	# Bytes
5	3

The GIBC is not an actual register but simply outputs the interrupting UART's transmit or receive byte counter value. The count, accurate at the time IACKN asserts, is captured in the CIR. The high order 5 bits are read as '0'. The GIBC is read only at address 2AH.

Global RxFIFO (GRxFIFO)

Received Data
8

Like the GIBC, no physical register implementation exists. The correct receiver's FIFO is popped based on the value of the interrupting channel field of the Current Interrupt Register.

If a receiver is not the cause of the current interrupt, a read of the Global RxFIFO will yield a byte containing all ones and NONE of the UART channels' receive FIFOs will be popped. (IMPORTANT)

The GRxFIFO is Read only at address 2BH.

Global TxFIFO (GTxFIFO)

Data to be Sent
8

Similar to the GRxFIFO, no physical register implementation exists. The byte is pushed into the correct transmitter's FIFO based on the interrupting channel field of the Current Interrupt Register.

If a transmitter is not the cause of the current interrupt, a write to the Global TxFIFO has no effect.

The GTxFIFO is Write only at address 2BH.

Global Interrupting Channel (GICR)

000000	Chan #
6	2

Like the other Global pseudo-registers no hardware register exists. The Channel number field of the Current Interrupt Register padded with leading zeros is output as the GICR. The GICR is Read only at address 29H.

Interrupt Control (ICR)

Threshold	IVC
6	2

The Threshold Field is used by the interrupt comparator to determine if a winning interrupt "bid" should result in interrupting the host MPU. The threshold field resets to 3Fh. The IVC field controls what kind of vector the QUART returns to the host MPU during an Interrupt Acknowledge cycle:

00 Output contents of Interrupt Vector Register
01 Output 6 MSBs of IVR and Channel number as 2 LSBs
10 Output 3 MSBs of IVR, Interrupt Type and Channel number
11 Disable generation of vector during IACK cycle

The IVC field reset to 00. The ICR is read/write at address 2CH.

Bidding Control Registers (BCRs)

Rcv'd Break	State Change	C/T
3	3	2

The 3 MSBs determine the priority of Received Break Interrupts; they are reset to 001.

Bits 4:2 determine the priority of Change of Input State interrupts, and are reset to 00. There is one BCR per UART channel; they can be read or written at addresses 20-23H.

Interrupt Vector (IVR)

Always Used	with IVC = 0x	w/IVC > 00
3	3	2

Holds the constant bits of the interrupt acknowledge vector. As shown, the three MSBs are always used, while the less significant bits can be replaced by the interrupt type code and/or Channel code bits. The IVR is write only at address 29H.

ABSOLUTE MAXIMUM RATINGS[2]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[3]	Note 5	°C
T_{STG}	Storage temperature range	–65 to +150	°C
V_{CC}	Voltage from V_{DD} to GND[4]	–0.5 to +7.0	V
V_S	Voltage from any pin to ground[4]	–0.5 to V_{CC} +0.5	V
P_D	Power dissipation	1	W

DC ELECTRICAL CHARACTERISTICS[5, 6, 7]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL} V_{IH} V_{IH}	Input low voltage Input high voltage (except X1/CLK) Input high voltage (X1/CLK)		 2.0 0.8V_{CC}		0.8	V V V
V_{OL} V_{OH}	Output Low voltage Output High voltage (except OD outputs)	I_{OL} = 4.0mA I_{OH} = –400µA I_{OH} = –100µA	 0.8V_{CC} 0.9V_{CC}		0.4	V V V
I_{IL} I_{IH}	Input current Low, I/O ports Input current High, I/O ports	V_{IN} = 0 V_{IN} = V_{CC}	–10		 1	µA µA
I_I	Input leakage current	V_{IN} = 0 to V_{CC}	–1		1	µA
I_{ILX1} I_{IHX1}	X1/CLK input Low current X1/CLK input High current	V_{IN} = GND, X2 = open V_{IN} = V_{CC}, X2 = open	–100		 100	µA µA
I_{OZH} I_{OZL}	Output off current High, 3–state data bus Output off current Low, 3–state data bus	V_{IN} = V_{CC} V_{IN} = 0	 –1		10 1	 µA
I_{ODL} I_{ODH}	Open–drain output Low current in off state: IRQN Open–drain output Low current in off state: IRQN	V_{IN} = 0 V_{IN} = V_{CC}	–1		 1	 µA
I_{CC}	Power supply current Operating mode	TTL input levels 25°C with X1 = 4MHz			50	mA
	Power down mode				5	mA

* See UART application note for power down currents less than 5µA.

AC ELECTRICAL CHARACTERISTICS[5, 6, 7, 8]

SYMBOL	FIGURE	PARAMETER	LIMITS Min	Typ	Max	UNIT
Reset timing						
t_{RES}	8	Reset pulse width	200			ns
I/O Port timing[9]						
t_{PS}	9	I/O input setup time before RDN Low	0			ns
t_{PH}	9	I/O input hold time after RDN High	0			ns
t_{PD}	9	I/O output valid from WRN High RDN Low			 110 110	 ns ns
Interrupt timing						
t_{IR}	10	INTRN negated or I/O output High from: Read RHR (RxRDY/FFULL interrupt) Write THR (TxRDY interrupt) Reset command (break change interrupt) Reset command (I/O change interrupt) Stop C/T command (counter interrupt) Write IMR (clear of interrupt mask bit) With respect to a 3.6864MHz clock on pin X1/CLK			 100 100 100 100 100 100	 ns ns ns ns ns ns
Clock timing						
t_{CLK}	11	X1/CLK low/high time	125/100			ns
t_{CLK}	11	X1/CLK low/high time (above 4MHz; X1/CLK ÷ 2 active)	56/56			ns
t_{CLK}	11	X1/CLK frequency	0[11]	3.6864	8.0	MHz
t_{CTC}	11	Counter/timer clock high or low time	60			ns
f_{CTC}	11	Counter/timer clock frequency	0[11]		8	MHz
t_{RX}	11	RxC high or low time	30			ns
f_{RX}	11	RxC frequency (16X) RxC frequency (1X)	0[11] 0[11]		16 1.0	MHz MHz
t_{TX}	11	TxC high or low time	30			ns
f_{TX}	11	TxC frequency (16X) TxC frequency (1X)	0[11] 0[11]		16 1.0	MHz MHz
Transmitter timing						
t_{TXD}	12	TxD output delay from TxC low			120	ns
t_{TCS}	12	TxC output delay from TxD output data	–20		+20	ns
Receiver timing						
t_{RXS}	13	RxD data setup time to RxC high	100			ns
t_{RXH}	13	RxD data hold time from RxC high	100			ns

NOTES:

1. Stress above these listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other condition above those indicated in the operation section of the specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range. See ordering information table for applicable temperature range and operating supply range.
5. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of V_{IL} and V_{IH}, as appropriate.
6. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
7. Test condition for interrupt and I/O outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}. Test conditions for rest of outputs: C_L = 150pF.
8. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
9. If CEN is used as the 'strobing' input, the parameter defines the minimum high times between one CEN and the next. The RDN signal must be negated for t_{RWD} guarantee that any status register changes are valid.
10. Consecutive write operations to the command register require at least three rising edges of the X1 clock between writes; four X1/clock edges if the 'X1/clk divide by 2' mode is used.
11. This value is not tested, but is guaranteed by design. For t_{CLK} minimum test rate is 2.0MHz.

AC ELECTRICAL CHARACTERISTICS[1] T_A = 25°C; V_{CC} = 5V ± 10%, unless otherwise specified. Limits shown as nn/nn refer to Commercial/Industrial temperature range. Single numbers apply to both ranges.

NO.	FIGURE	CHARACTERISTIC	LIMITS			UNIT
			Min	Typ	Max	
1	3	A[5:0] Setup time to RDN WRN Low	10			ns
2	3	A[5:0] Hold time from RDN WRN Low	30			ns
3	3	CEN Setup time to RDN WRN Low[2]	0			ns
4	3	CEN Hold time from RDN WRN High[2]	0			ns
5	3	RDN WRN Pulse Width Low	110/115			ns
6	3	D[7:0] Data Valid after CEN and RDN Low			110/115	ns
7	3	D[7:0] Data Bus floating after RDN or CEN High			30	ns
8	3	D[7:0] Data Bus Setup time before WRN or CEN High	40			ns
9	3	D[7:0] Hold time after WRN or CEN High	8			ns
10	3	Time between Reads and/or Writes[3]	50			ns

NOTES:
1. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as a 'strobing' input. CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence the signal asserted last initiates the cycle; the signal negated first terminates the cycle.
2. The RDN signal must be negated for t_{RWD} to guarantee that internal registers update before the next read.
3. Consecutive write operations to the upper four bits of the Command Register (CR) require at least three X1/CLK edges; four X1/CLK edges in the 'X1/CLK divide by 2' mode.

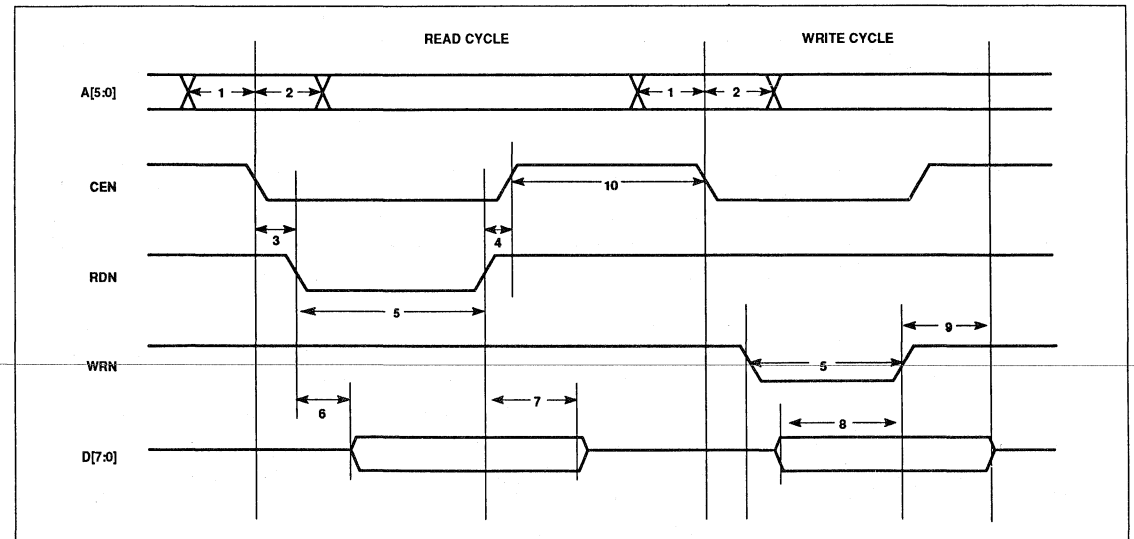


Figure 3. A Read Cycle Followed by a Write Cycle without DACKN

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = 5V \pm 10\%$, unless otherwise specified. Limits shown as nn/nn refer to Commercial/Industrial temperature range. Single numbers apply to both ranges.

NO.	FIGURE	CHARACTERISTIC	LIMITS			UNIT
			Min	Typ	Max	
1	4	D[7:0] Valid after IACKN Low			110/115	ns
2	4	DACKN Low after IACKN Low	10 + 2 X1 edges		90/122 + 3 X1 edges	ns
3	4	D[7:0] floating after IACKN High	0		30	ns
4	4	DACKN High after IACKN High	0		30	ns
5	4	IACKN High after IACKN Low	110/115			ns

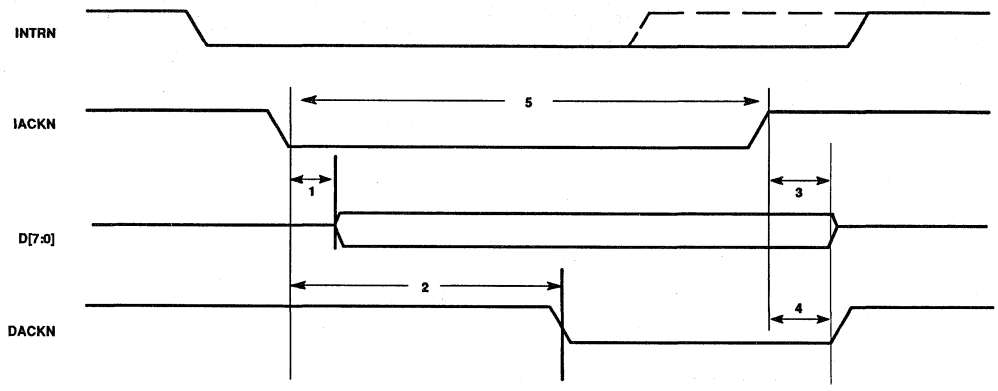


Figure 4. Interrupt Knowledge (IACKN) Timing

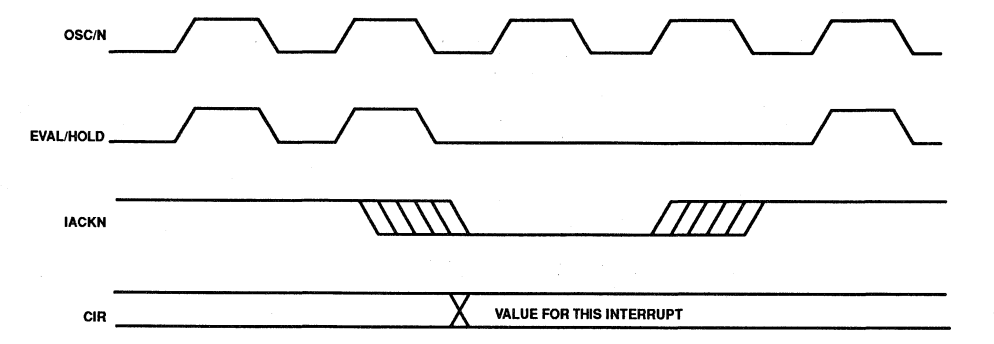


Figure 5. Interrupt Bid Arbitration Timing.

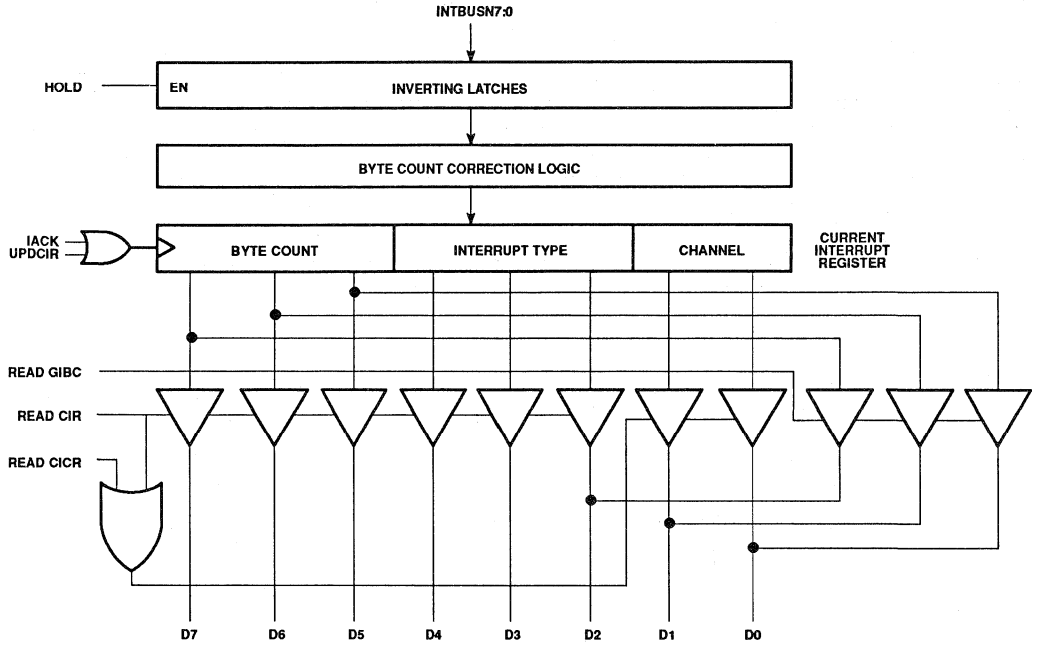


Figure 6. Current Interrupt Register Logic

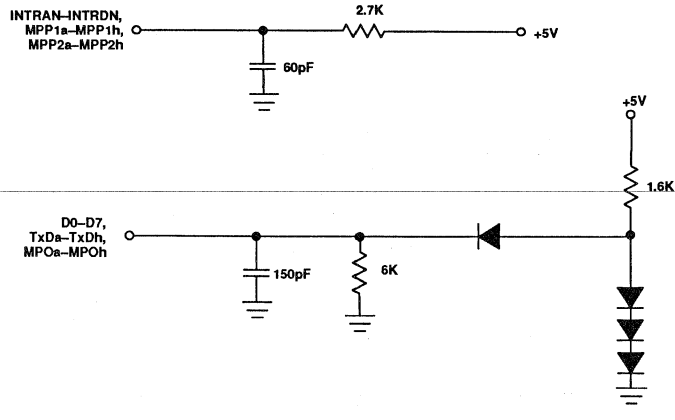


Figure 7. Test Conditions on Outputs

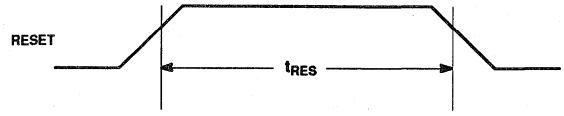


Figure 8. Reset Timing

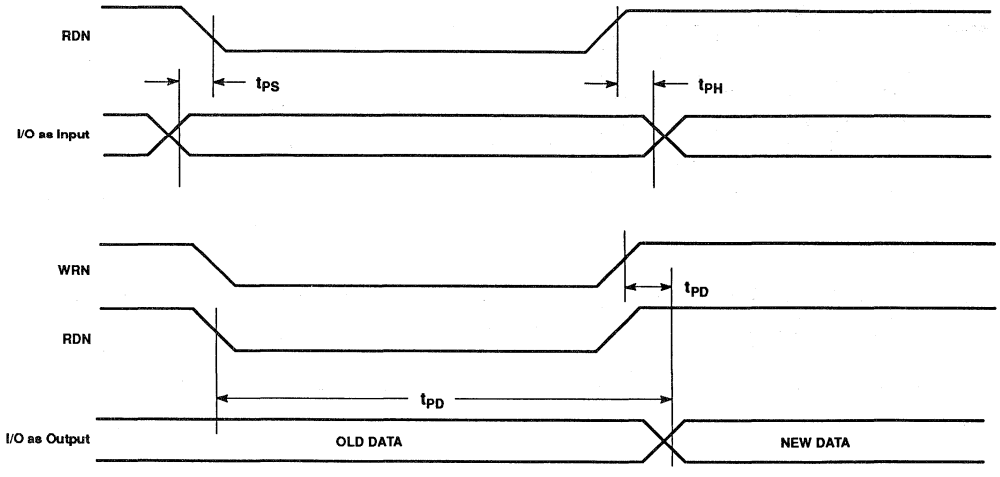
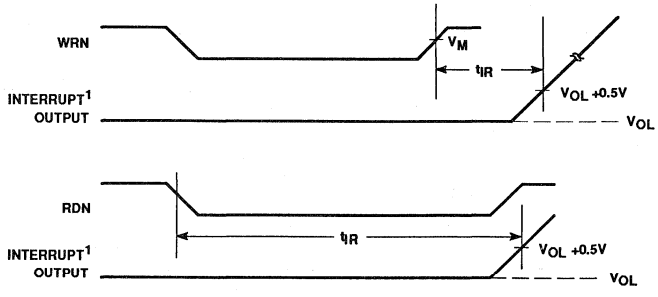
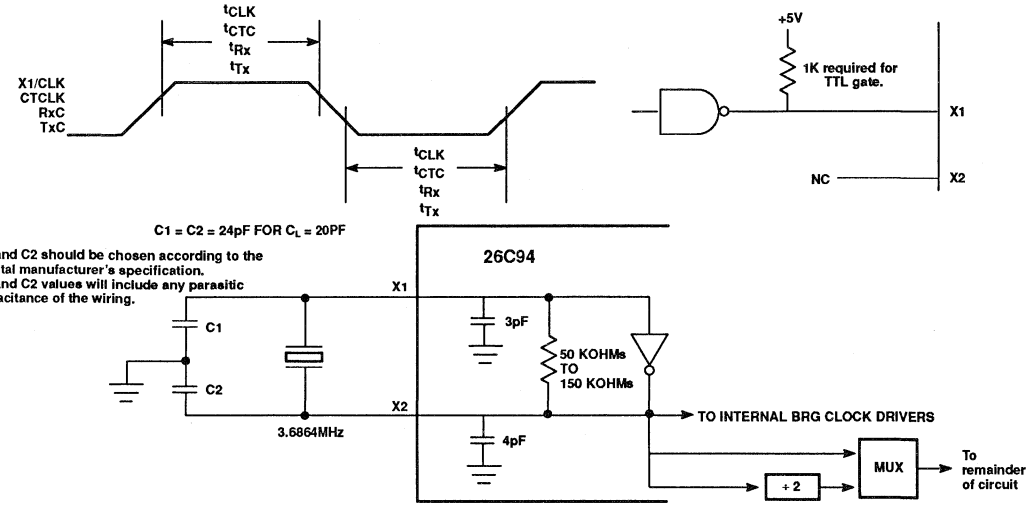


Figure 9. I/O Port Timing



NOTES:
1. INCLUDES I/O WHEN USED AS TxRDY or RxDY/FFULL OUTPUTS AS WELL AS INTRN.
2. THE TEST FOR OPEN DRAIN OUTPUTS IS INTENDED TO GUARANTEE SWITCHING OF THE OUTPUT TRANSISTOR. MEASUREMENT OF THIS RESPONSE IS REFERENCED FROM THE MIDPOINT OF THE SWITCHING SIGNAL, V_M, TO A POINT 0.5V ABOVE V_{OL}. THIS POINT REPRESENTS NOISE MARGIN THAT ASSURES TRUE SWITCHING HAS OCCURRED. BEYOND THIS LEVEL, THE EFFECTS OF EXTERNAL CIRCUITRY AND TEST ENVIRONMENT ARE PRONOUNCED AND CAN GREATLY AFFECT THE RESULTANT MEASUREMENT.

Figure 10. Interrupt Timing



NOTES:
C1 and C2 should be based on manufacturer's specification.
X1 and X2 parasitic capacitance IS 1-2pF AND 3-5pF, respectively.
GAIN: at 4MHz 8 to 14db; at 8MHz 2 to 6db
PHASE: at 4MHz 272° to 276°; at 8MHz 272° to 276°

TYPICAL CRYSTAL SPECIFICATION

FREQUENCY:	2 – 4MHZ
LOAD CAPACITANCE (C_L):	12 – 32pF
TYPE OF OPERATION:	PARALLEL RESONANT, FUNDAMENTAL MODE

Figure 11. Clock Timing

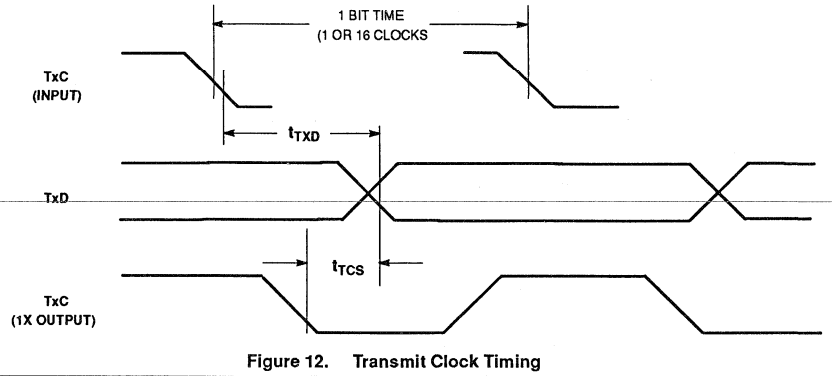


Figure 12. Transmit Clock Timing

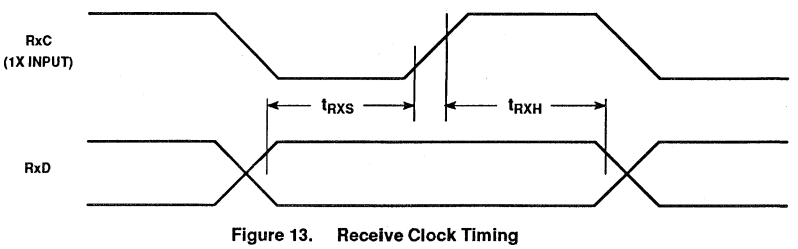
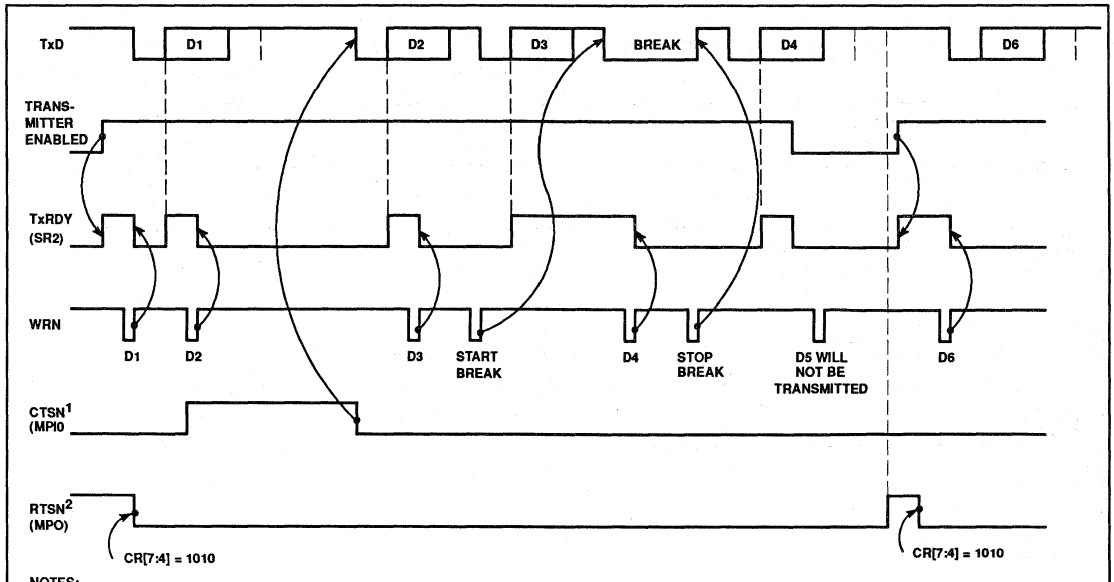
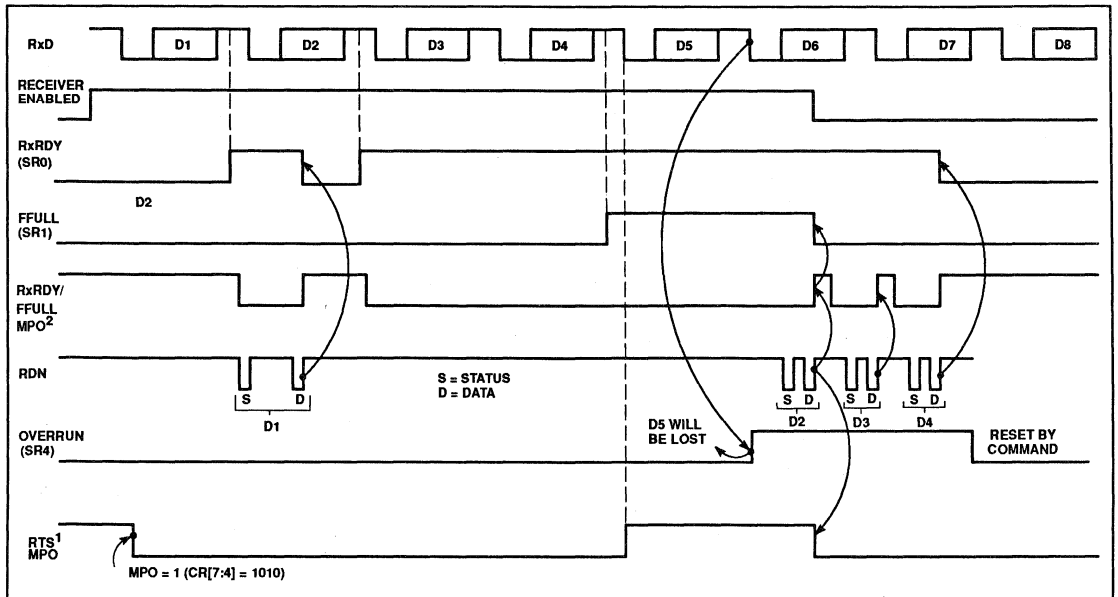


Figure 13. Receive Clock Timing



NOTES:
1. TIMING SHOWN FOR MR2[4] = 1.
2. TIMING SHOWN FOR MR2[5] = 1.

Figure 14. Transmitter Data Timing



NOTES;
1. TIMING SHOWN FOR MR1[7] = 1.
2. SHOWN FOR OPCR [6:4, 2:0] = 111 AND MR1[6] = 0.

Figure 15. Receiver Data Timing

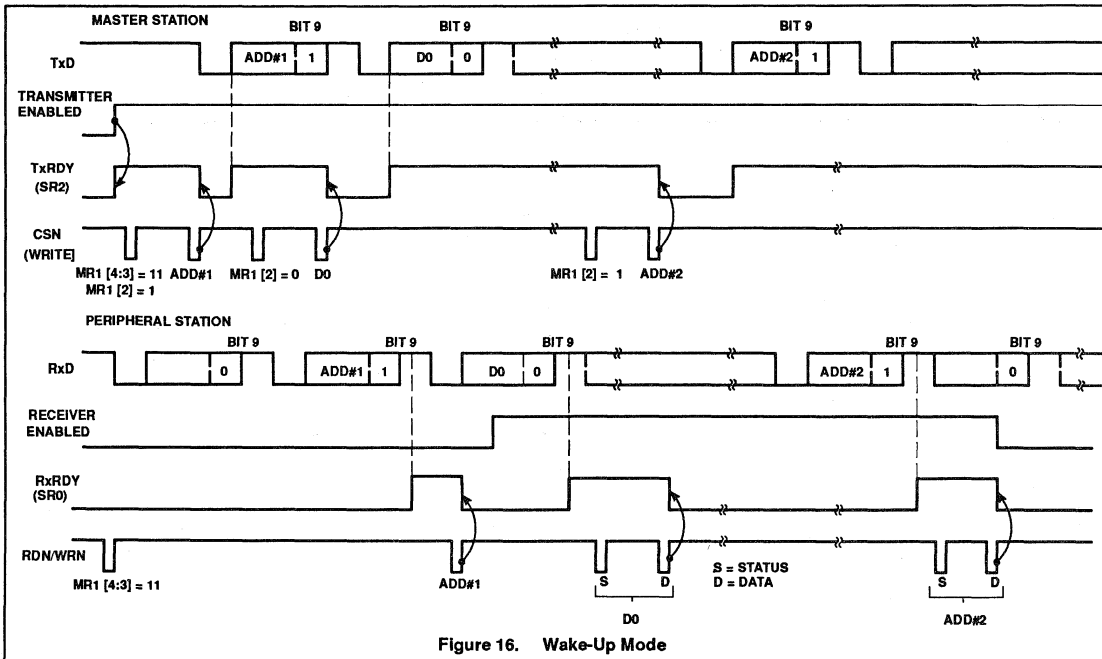


Figure 16. Wake-Up Mode

INTERRUPT NOTES

The following is a brief description of the new QUART "Bidding" interrupt system, interrupt vector and the use of the Global registers.

The new features of the QUARTs have been developed to greatly reduce the microprocessor time required to service uart interrupts. Bus cycle times have also been enhanced. By use of the new Current Interrupt Register (CIR) the speed of a poled system is also improved. For example programming the SCC2692 to interrupt on TxRDY and RxFUL would generate four interrupts for every six characters processed along with at least two additional accesses to the chip for each interrupt. This amounts to two non–data chip accesses per character. In the 26C94 this has been reduced to 0.25 non data accesses per character; an eight fold improvement. In certain conditions use of the global registers will yield a greater improvement.

The QUART has 18 possible sources which can be programmed to generate an interrupt:

- 4 Receiver channels
- 4 Transmitter Channels
- 4 Received "Brake" conditions
- 4 Change of State Detectors (a total of 8 ports)
- 2 Counter/Timers

These sources are encoded in such a way that they generate a unique value. This value is defined by chip hardwire programming, user programming, and the source's present condition. The values the sources generate are compared (at the X1 clock rate) to a user defined Interrupt Threshold value contained in the ICR (Interrupt Control Register). When the source's value exceeds the threshold the interrupt is generated. It is the source's value which is captured in the CIR.

The heart of the interrupt speed enhancement is attained by allowing the interrupting source to encode its channel, interrupt type and, if appropriate, the number of FIFO bytes requiring service. This information is coded and transferred the CIR (Current Interrupt Register) at the time IACKN is asserted or the command 'Update CIR' is executed. Upon an interrupt the processor may read this register and in one access determine the "who, what and how much". This CIR value is used to drive the interrupt vector modification (when used) and the new "Global" registers.

"Global" Registers

The "Global Registers" are effectively pointers which use the contents of the CIR to direct a read or write operation to Rx or Tx or other source which is currently interrupting. There are four global registers defined in the register map:

1. Global Interrupting Byte Count
2. Global Interrupting Channel
3. Global Receive FIFO Register
4. Global Transmit FIFO Register

The global receive and transmit registers operate as an indirect address. The data read from the global receive register will be that of the currently interrupting receiver; the data written to the global transmit register will go to the currently interrupting transmitter. The interesting point here is that under certain circumstances an interrupt can be serviced without an interrogation of the chip.

For completeness it should be noted that the global registers are not physical devices. Reads of the Global Byte and Channel registers give the Byte count or Channel number, respectively, (right justified) of the interrupting channel. The CIR data is mapped to these "registers".

6 "Bidding Format"

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION
Rx Byte count			Error 1	1	1	Channel No.		Receiver bid With error
Rx Byte count			no Error 0	1	1	Channel No.		Receiver bid No error
0	Tx Byte Count			1	0	Channel No.		Transmit bid
Programmable			1	0	0	Channel No.		Receive Brake
Programmable			0	0	1	Channel No.		Change of State
Programmable		0	1	0	1	Channel No.		Counter/Timer

NOTES:

1. The ones and zeros above represent the hardwired positions.
2. Note the format of bits 4:2. They represent the identity of the interrupting source.
3. Bids with the highest number of contiguous MSBs win the bid.

1 1 1	Receiver with error
0 1 1	Receiver without error
x 1 0	Transmitter
1 0 0	Receiver brake detect
0 0 1	Change of State
1 0 1	Counter/Timer
0 0 0	No interrupt

In these identifiers the receivers are biased to have highest priority. The identifier bits and the channel number bits are hardwired on the chip. Normally the non–data interrupts would be programmed to a low value. The programmable fields can, in some cases, make these sources higher than a full receiver.

It would seem that a 11 programmed in the upper counter/timer bits, for example, would cause it to interrupt nearly all the time. This is not true . A counter/timer that has not timed out will not bid. In a similar fashion a receiver FIFO that is empty or a transmitter FIFO that is full will not bid

In general terms the threshold value programmed in the ICR (Interrupt Control Register) will reflect some fill level of the eight character transmit and receive FIFOs that allow processor service without underrun or overrun occurring.

Note that interrupt threshold value in the ICR is 6 bits long. This value is aligned with the bid arbitration logic such that it bids only through the most significant 6 bits. The result of this is that the channel value does not 'bid'. However the logic is such that other parts of the bid being equal the condition of the highest channel will be captured in CIR. The increasing order of the channels is A, B, C, D. Thus channel D is the "strongest" of the four.

It could be that the giving the highest strength to channel D may, from time to time, not be what would be most desired. Further it may

be desired to alter the authority of a channel's bid. This may be done by setting the Rx and/or Tx interrupt bits in MR0 and MR1 to values different than zero. This will have the effect of not allowing the associated receiver or transmitter to bid until its FIFO reaches a particular fill level. Although this compromises the idea of the bidding interrupt scheme, it is entirely safe to use. In fact it is setting of MR0 and MR1 interrupt bits to zero that causes the receiver to stop bidding when it is empty and causes the transmitter to stop bidding when it is full. Altering the MR0 and MR1 interrupt bits only changes the level at which the Rx & Tx bidding is stopped.

See the "Interrupt Note on 26C94" on page 12 which refers to the use of the MR registers in controlling the Rx and Tx bidding.

Table 7. Configuration of Interrupt Vector for the QUART

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Interrupt vector for → ICR(1:0) = 00	INTERRUPT VECTOR FORMATS (Controlled by ICR[1:0])							
	IVR[7:0]							
	Full interrupt vector							
Interrupt vector for → ICR(1:0) = 01								
	IVR[7:2]						ICR[1:0]	
	Interrupt vector 6 MSBs						Channel number	
Interrupt vector for → ICR(1:0) = 10								
	IVR[7:5]			ICR[4:2]			ICR[1:0]	
	Interrupt vector 3 MSBs			Interrupt type			Channel number	
Interrupt vector for → ICR(1:0) = 11 (Inhibit)								
	Inhibit vector output. (Set bus to FFh)							
	CURRENT INTERRUPT REGISTER FORMAT CIR[7:0]							
	Rx or Tx byte count			Interrupt type: R/Tx CT COS BRK			Channel number	
	INTERRUPT CONTROL REGISTER FORMAT ICR[0:7]							
	Interrupt threshold ICR[7:2]						Interrupt vector format ICR[1:0]	

In normal operation the character of an interrupt will be controlled by the above registers in conjunction with the IMR (Interrupt Mask Register (one for each DUART)) . The function of the IMR will be to enable bidding of any particular source.

Recall that the QUART has 18 functions which may generate an interrupt.

The format of the interrupt vector is controlled by the ICR[1:0] bits. The formats are shown in Table 7. The purpose of the vector modification is to allow the interrupting source (either channel or type and channel) to direct the processor to appropriate service routine. We have found that some users wish to use extremely tight loops for the service routines and find the addition of several tests of status bytes to be very 'expensive' in processor time.

NOTE ON QUART INTERFACE TO ITS CONTROLLING PROCESSOR

The QUART, has been designed to interface in either the synchronous interrupt environment (without DACKN) or the asynchronous interrupt environment (with DACKN). The 80xxx devices of Intel design are usually operated in a synchronous interrupt mode while those of Motorola design, 68xxx devices, operate in an asynchronous interrupt mode.

Note: Synchronous and asynchronous interrupt modes are not in any way associated with synchronous or asynchronous data transmission.

The QUART has been designed with the pins required to service either interface. In general then it is probable that in any application some of the interface pins will not be used. This note discusses what is required for the "text book" connections of the two methods. It should be noted that features of either method are not mutually exclusive.

The interface pins are all active low. (at V_{SS} or ground) The pins used for normal reading and writing to the QUART (the generation of a bus cycle) are CEN (Chip Enable), RDN (Read Enable), WRN (Write Enable). The pins used in the interrupt service are IRQN (Interrupt Request), IACKN (Interrupt Acknowledge). The pin used for data transfer is DACKN (Data Acknowledge). IRQN and DACKN are open drain outputs.

DACKN signaling can be enabled or disabled via writing to address 27h or 26h respectively. Note that if DACKN is enabled that writing to the QUART will occur on the falling edge of DACKN. The use of hardware reset (required at power up) enables DACKN.

The Asynchronous Interface

Those familiar with 68xxx I/O will note the use of the two pins RDN and WRN to be in conflict with 68xxx devices use of the one R/WN pin. The R/WN must be inverted such that the R/WN may drive the WRN input while the inversion of R/WN drives the RDN input. It is good practice to condition the inversion of R/WN such that RDN will not become active on the termination of a write to the QUART while CEN is still asserted. These short periods of read could upset FIFO pointers in the chip.

During a read of the QUART DACKN signals that valid data is on the data bus. During a write to the QUART DACKN signals that data placed on the bus by the control processor has been written to the addressed register. The generation of DACKN begins with the start of a bus cycle (Read, Write or Interrupt Acknowledge) and then requires two edges of the X1 clock plus 70ns for its assertion.

In this mode the writing of data to the QUART registers occurs on the falling edge of DACKN or the rising edge of the combination of CEN and WRN which ever occurs first. This requires that the data to be written to the QUART registers be valid with respect to the leading edge of the combination of CEN and WRN. (In the synchronous mode it is the trailing edge)

IACKN updates the CIR (Current Interrupt Register) and places the Interrupt Vector or Modified Interrupt Vector on the bus if the Interrupt Vector is used.

The Synchronous Interface

In this mode the DACKN and IACKN are usually not used. Here data is written to the QUART on the trailing edge of the combination of CEN and WRN. The placing of data on the bus during a read cycle begins with the leading edge of the combination of CEN and RDN.

The read cycle will terminate with the rise of CEN or RDN which ever one occurs first. In this mode bus cycles are usually setup to be the minimum time required by the QUART and hence will be faster than bus cycles that are defined by the DACKN signal. DACKN should be turned off in this mode.

When IACKN is not used or is not available the command at 2Ah should be used to update the CIR (Current Interrupt Register). This register is normally updated by IACKN in response to the IRQN. Note that the CIR is not updated by IRQN since there could be a long time between the assertion of IRQN and the start of the interrupt service routine. During this time it is quite possible that another interrupt with a higher priority occurs. It is the CIR that contains the information that describes the interrupt source and its priority. It is therefor recommended that the first operation upon entering the interrupt service routine is the updating of the CIR. (Recall that the contents of the GLOBAL registers reflect the content of the CIR)

Summary

In the asynchronous mode all of the interface pins are usually used. The synchronous mode usually will not use the IACKN and DACKN. However there is no conflict in the quart if both modes are used in the same application. (i.e. More than one device may control the QUART) The principles to keep in mind are:

1. When IACKN is not used the CIR should be updated via command.
2. If DACKN is not used it should be disabled.
3. When in the asynchronous mode be sure DACKN is enabled.
4. With 68xxx type controllers the RDN signal must be generated.

Quad universal asynchronous receiver/transmitter (QUART) SC68C94

DESCRIPTION

The 68C94 quad universal asynchronous receiver/transmitter (QUART) combines four enhanced Signetics industry-standard UARTs with an innovative interrupt scheme that can vastly minimize host processor overhead. It is implemented using Signetics' high-speed CMOS process that combines small die size and cost with low power consumption.

The operating speed of each receiver and transmitter can be selected independently at one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the QUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

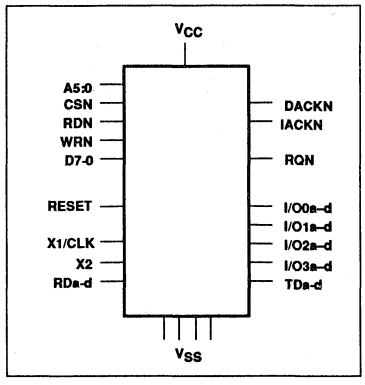
Each receiver is buffered with eight character FIFOs (first-in-first-out memories) and one shift register to minimize the potential for receiver overrun and to reduce interrupt overhead in interrupt driven systems. In addition, a handshaking capability is provided to disable a remote UART transmitter when the receiver buffer is full. (RTS control)

The 68C94 provides a power-down mode in which the oscillator is stopped and the register contents are stored. This results in reduced power consumption on the order of several magnitudes. The QUART is fully TTL compatible and operates from a single +5V power supply.

FEATURES

- New low overhead interrupt control
- Four Signetics industry-standard UARTs
- Eight byte receive FIFO and eight byte transmit FIFO for each UART
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Baud rate for the receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4K baud Non-standard rates to 1.0M baud
  - User-defined rates from the programmable counter/timer associated with each of two blocks
  - External 1x or 16x clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex), automatic echo, local loop back, remote loopback
- Programmable interrupt priorities
- Identification of highest priority interrupt
- Global interrupt register set provides data from interrupting channel
- Vectored interrupts with programmable vector format
- IACKN and DTACKN signals
- Built-in baud rate generator with choice of 18 rates

PIN CONFIGURATIONS



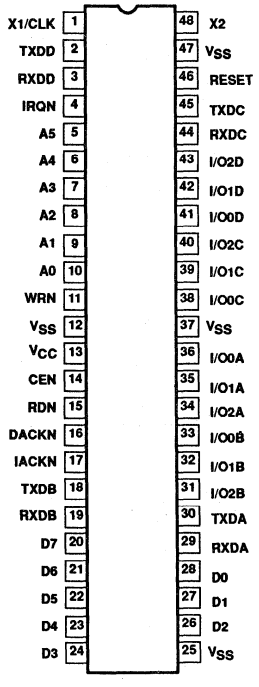
- Four I/O pins per UART for modem controls, clocks, etc.
- Power down mode
- High-speed CMOS technology
- 52-pin PLCC and 48-pin DIP
- Commercial and industrial temperature ranges available
- On-chip crystal oscillator
- TTL compatible
- Single +5V power supply with low power mode
- Two multifunction programmable 16-bit counter/timers
- 1MHz 16x mode operation
- 30ns data bus release time
- "Watch Dog" timer for each receiver

ORDERING INFORMATION

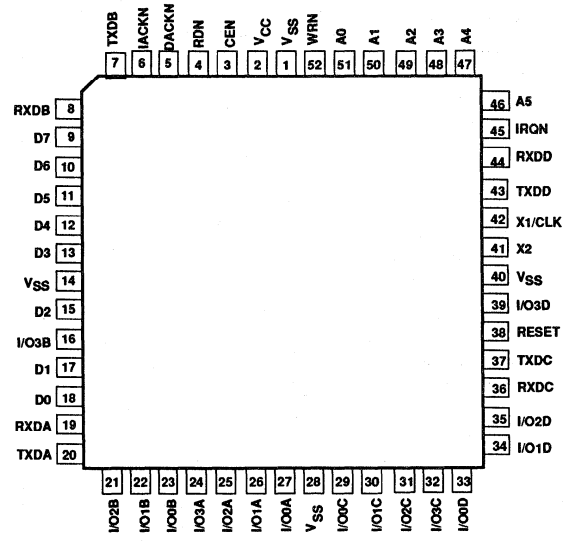
PACKAGES	V_{CC} = +5V ±10%, T_A = 0°C to +70°C	V_{CC} = +5V ±10%, T_A = –40°C to +85°C
48-Pin Plastic DIP	SC68C94C1N	SC68C94A1N
52-Pin PLCC	SC68C94C1A	SC68C94A1A

PIN CONFIGURATIONS

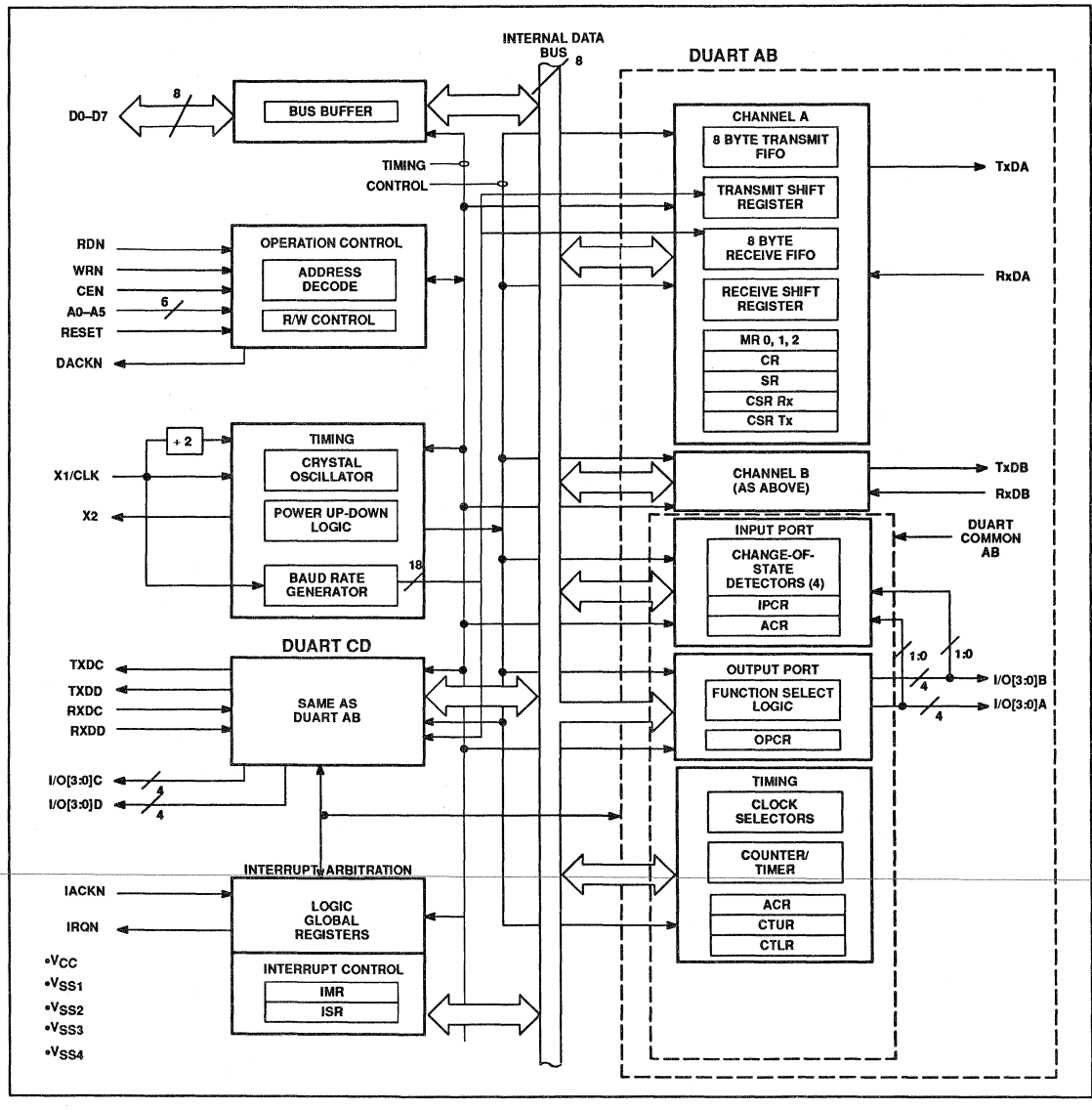
48-Pin Dual-In-Line Package



52-Pin PLCC Package



BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	TYPE	NAME AND FUNCTION
CEN	I	**Chip Select:** Active low input that, in conjunction with RDN or WRN, indicates that the host MPU is trying to access a QUART register. CEN must be inactive when IACKN is asserted.
A5:0	I	**Address Lines:** These inputs select a 68C94 register to be read or written by the host MPU.
D7:0	I/O	**8-bit Bidirectional Data Bus:** Used by the host MPU to read and write 68C94 registers.
RDN	I	**Read Strobe:** Active low input. When this line is asserted simultaneously with CEN, the 68C94 places the contents of the register selected by A5:0 on the D7:0 lines.
WRN	I	**Write Strobe:** Active low input. When this line is asserted simultaneously with CEN, the 68C94 writes the data on D7:0 into the register selected by A5:0.
DACKN	O	**Data ACKnowledge:** Active low, open-drain output to the host MPU, which is asserted subsequent to a read or write operation. For a read operation, assertion of DACKN indicates that register data is valid on D7:0. For a write operation, it indicates that the data on D7:0 has been captured into the indicated register. This signal corresponds to READYN on 80x86 processors and DTACKN on 680x0 processors.
IRQN	O	**Interrupt Request:** This active low open-drain output to the host MPU indicating that one or more of the enabled UART interrupt sources has reached an interrupt value which exceeds that pre-programmed by host software. The IRQN can be used directly as a 680x0 processor input; it must be inverted for use as an 80x86 interrupt input. This signal requires an external pull-up resistor.
IACKN	I	**Interrupt ACKnowledge:** Active low input indicating that the host MPU is acknowledging an interrupt requested by this device. The 68C94 responds to the assertion of this signal by placing an interrupt vector on D7-D0 and asserting DACKN. This signal updates the CIR register in the interrupt logic.
TDa-d	O	**Transmit Data:** Serial outputs from the four UARTs.
RDa-d	I	**Receive Data:** Serial inputs to the four UARTs/
I/O0a-d	I/O	**Input/Output 0:** A multi-use input or output signal for each UART. These pins can be used as general purpose inputs, Clear to Send inputs, 1X or 16X Transmit Clock outputs or general purpose outputs. Change-of-state detection is provided for these pins.
I/O1a-d	I/O	**Input/Output 1:** A multi-use input or output signal for each UART. These pins can be used as general purpose or 1X or 16X transmit clock inputs, or general purpose 1X or 16X receive clock outputs. Change-of-state detection is provided for these pins. In addition, I/O1a and I/O1c can be used as Counter/Timer inputs and I/O1b and I/O1d can be used as Counter/Timer outputs.
I/O2a-d	I/O	**Input/Output 2:** A multi-use input or output signal for each UART. These pins can be used as general purpose inputs, 1X or 16X receive clock inputs, general purpose outputs, RTS output or 1X or 16X receive clock outputs.
I/O3a-d	I/O	**Input/Output 3:** A multi-use input or output signal for each UART. These pins can be used as general purpose inputs, 1X or 16X transmit clock inputs, general purpose outputs, or 1X or 16X transmit clock outputs.
RESET	I	**Master Reset:** Active high reset for the 68C94 logic. Must be asserted at power-up, may be asserted at other times that the system is to be reset and restarted. OSC set to divide by 1, MR pointer set to 1, DACKN enabled, I/O pins to input. Registers reset: OMR, CIR. IRQN, DTACKN, IVR Interrupt Vector, Power Down, Test registers, FIFO pointers, Baud rate generator, Error Status, Watch Dog Timers, IMR, Change of State detectors, counter/timer to timer, Transmitter and Receiver controllers.
X1/CLK	I	**Crystal 1 or Communication Clock:** This pin is normally connected to one side of a 3.6864MHz or a 7.3728MHz crystal, or can be connected to an external clock up to 8MHz.
X2	O	**Crystal 2:** If a crystal is used, this pin should be connected to its other terminal. If an external clock is applied to X1, this pin should be left unconnected.
V_{CC}, V_{SS1}, V_{SS2}, V_{SS3}, V_{SS4}		**Power and grounds:** respectively.

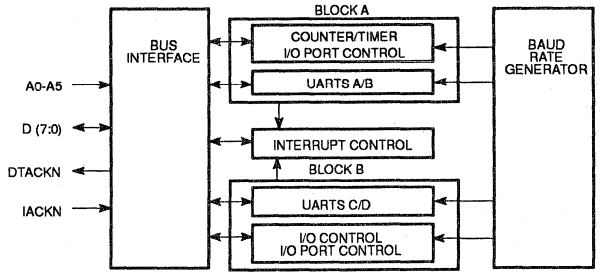


Figure 1. Channel Architecture

Table 1. QUART Registers

A5:0	READ (RDN = Low)	WRITE (WRN = Low)
000000	Mode Register a (MR0a, MR1a, MR2a)	Mode Register a (MR0a, MR1a, MR2a)
000001	Status Register a (SRa)	Clock Select Register a (CSRa)
000010	Reserved	Command Register a (CRa)
000011	Receive Holding Register a (RxFIFOa)	Transmit Holding Register a (TxFIFOa)
000100	Input Port Change Reg ab (IPCRab)	Auxiliary Control Reg ab (ACRab)
000101	Interrupt Status Reg ab (ISRab)	Interrupt Mask Reg ab (IMRab)
000110	Counter/Timer Upper ab (CTUab)	Counter/Timer Upper Reg ab (CTURab)
000111	Counter/Timer Lower ab (CTLab)	Counter/Timer Lower Reg ab (CTLRab)
001000	Mode Register b (MR0b, MR1b, MR2b)	Mode Register b (MR0b, MR1b, MR2b)
001001	Status Register b (SRb)	Clock Select Register b (CSRb)
001010	Reserved	Command Register b (CRb)
001011	Receive Holding Register b (RxFIFOb)	Transmit Holding Register b (TxFIFOb)
001100	Output Port Register ab (OPRab)	Output Port Register ab (OPRab)
001101	Input Port Register ab (IPRab)	I/OPCRa (I/O Port Control Reg a)
001110	Start Counter ab	I/OPCRb (I/O Port Control Reg b)
001111	Stop Counter ab	Reserved
010000	Mode Register c (MR0c, MR1c, MR2c)	Mode Register c (MR0c, MR1c, MR2c)
010001	Status Register c (SRc)	Clock Select Register c (CSRc)
010010	Reserved	Command Register c (CRc)
010011	Receive Holding Register c (RxFIFOc)	Transmit Holding Register c (TxFIFOc)
010100	Input Port Change Reg cd (IPCRcd)	Auxiliary Control Reg cd (ACRcd)
010101	Interrupt Status Reg cd (ISRcd)	Interrupt Mask Reg cd (IMRcd)
010110	Counter/Timer Upper cd (CTUcd)	Counter/Timer Upper Reg cd (CTURcd)
010111	Counter/Timer Lower cd (CTLcd)	Counter/Timer Lower Reg cd (CTLRcd)
011000	Mode Register d (MR0d, MR1d, MR2d)	Mode Register d (MR0d, MR1d, MR2d)
011001	Status Register d (SRd)	Clock Select Register d (CSRd)
011010	Reserved	Command Register d (CRd)
011011	Receive Holding Register d (RxFIFOd)	Transmit Holding Register d (TxFIFOd)
011100	Output Port Register cd (OPRcd)	Output Port Register cd (OPRcd)
011101	Input Port Register cd (IPRcd)	I/OPCRc (I/O Port Control Reg c)
011110	Start Counter cd	I/OPCRd (I/O Port Control Reg d)
011111	Stop Counter cd	Reserved
100000	Bidding Control Register a (BCRa)	Bidding Control Register a (BCRa)
100001	Bidding Control Register b (BCRb)	Bidding Control Register b (BCRb)
100010	Bidding Control Register c (BCRc)	Bidding Control Register c (BCRc)
100011	Bidding Control Register d (BCRd)	Bidding Control Register d (BCRd)
100100	Reserved	Power Down
100101	Reserved	Power Up
100110	Reserved	Disable DACKN
100111	Reserved	Enable DACKN
101000	Current Interrupt Register (CIR)	Reserved
101001	Global Interrupt Channel Reg (GICR)	Interrupt Vector Register (IVR)
101010	Global Int Byte Count Reg (GIBCR)	Update CIR
101011	Global Receive Holding Reg (GRxFIFO)	Global Transmit Holding Reg (GTxFIFO)
101100	Interrupt Control Register (ICR)	Interrupt Control Register (ICR)
101101	Reserved	BRG Rate. 00 = low; 01 = high
101110	Reserved	Set X1/CLK divide by two
101111	Reserved	Set X1/CLK Normal
110000–111000	Reserved	Reserved
111001	Test Mode	Test Mode
111010–111111	Reserved	Reserved

FUNCTIONAL BLOCKS

The QUART is composed of four Signetics industry–standard UARTs, each having a separate transmit and receive channel.

The Basic UART cells in the QUART are configured with 8-byte Receive FIFOs and 8-byte Transmit FIFOs. Hardware supports interrupt priority arbitration based on the number of bytes available in the transmit and receive FIFOs, counter/timers, change of state detectors, break detect or receiver error. Attempts to push a full FIFO or pop an empty FIFO do not affect the count.

Baud Rate Generator

The baud rate generator used in the QUART is the same as that used in other Signetics industry standard UARTs. It provides 18 basic Baud rates from 50 baud to 38,400 baud. It has been enhanced to provide to provide other baud rates up to 230,400 baud based on a 3.6364MHz clock. With an 8.0MHz clock rates to 500K baud. Other rates are available by setting the BRG rate to high at address 2D hex or setting Test 1 on at address 39 hex. See Table 3. These two modes are controlled by writing 00 or 01 to the addresses above. They are both set to 00 on reset. External Rx and Tx clocks yield rates to 1MHz in the 16X mode.

BLOCK DIAGRAM

As shown in the block diagram, the QUART consists of: data bus buffer, interrupt control, operation control, timing, and four receiver and transmitter channels. The four channels are divided into two different blocks, each block independent of the other.

Channel Blocks

There are two blocks (Block Diagram), each containing two sets of receiver/transmitters. In the following discussion, the description applies to Block A which contains channels a and b. However, the same information applies to all channel blocks.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the QUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The functions performed by the CPU read and write operations are shown in Table 1.

Mode registers (MR) 0, 1 and 2 are accessed via an address counter. This counter is set to one (1) by reset or a command 1x to the Command Register for compatibility with other Signetics software. It is set to 0 via a command Bx to the Command Register (CR). The address counter is incremented with each access to the MR until it reaches 2 at which time it remains at 2. All subsequent accesses to the MR will be to MR2 until the MR counter is changed by a reset or an MR counter command.

The Mode Registers control the basic configuration of the UART channels. There is one for each UART. (Transmitter/receiver pair)

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, power up/down logic and a divide by 2 selector. Closely associated with the timing block are two 16-bit counter/timers; one for each DUART.

Oscillator

The crystal oscillator operates directly from a 3.6864MHz crystal connected across the X1/CLK and X2 inputs with a minimum of external components. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. If an external clock is used instead of a crystal, X1 must be driven and X2 left floating as shown in Figure 11. The clock serves as the basic timing reference for the baud rate generator (BRG), the counter/timer, and other internal circuits. A clock frequency, within the limits specified in the electrical specifications, must be supplied even if the internal BRG is not used.

Baud Rate Generator

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. The eighteen BRG rates are grouped in two groups. Eight of the 18 are common to each group. The group selection is controlled by ACR[7]. See the Baud Rate Table 3. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The clock selectors allow the independent selection, by the receiver and transmitter, of any of these baud rates or an external timing signal.

Counter/Timer

The counter timer is a 16-bit programmable divider that operates in one of three modes: counter, timer, time out. In the timer mode it generates a square wave. In the counter mode it generates a time delay. In the time out mode it monitors the time between received characters. The C/T uses the numbers loaded into the Counter/Timer Lower Register (CTLR) and the Counter/Timer Upper Register (CTUR) as its divisor.

There are two counter/timers in the QUART; one for each block. The counter/timer clock source and mode of operation (counter or timer) is selected by the Auxiliary Control Register bits 6 to 4 (ACR[6:4]). The output of the counter/timer may be used for a baud rate and/or may be output to the I/O pins for some external function that may be totally unrelated to data transmission. The counter/timer also sets the counter/timer ready bit in the Interrupt Status Register (ISR) when its output transitions from 1 to 0.

A register read address (see Table 1) is reserved to issue a start counter/timer command and a second register read address is reserved to issue a stop command. The value of D(7:0) is ignored. The START command always loads the contents of CTUR, CTLR to the counting registers. The STOP command always resets the ISR(3) bit in the interrupt status register.

Timer Mode

In the timer mode a symmetrical square wave is generated whose half period is equal in time to division of the selected counter/timer clock frequency by the 16-bit number loaded in the CTLR CTUR. Thus, the frequency of the counter/timer output will be equal to the counter/timer clock frequency divided by twice the value of the CTUR CTLR. While in the timer mode the ISR bit 3 (ISR[3]) will be set each time the counter/timer transitions from 1 to 0. (High to low) This continues regardless of issuance of the stop counter command. ISR[3] is reset by the stop counter command. NOTE: Reading of the CTU and CTL registers in the timer mode is not meaningful.

When the C/T is used to generate a baud rate *and* the C/T is selected through the CSR then the receivers and/or transmitter will be operating in the 16x mode. Calculation for the number 'n' to program the counter timer upper and lower registers is shown below.

$$n = \frac{\text{C/T Clock Frequency}}{2 * 16 * \text{Baud rate desired}}$$

Often this division will result in a non-integer number; 26.3 for example. One can only program integer numbers to a digital divider. Therefore 26 would be chosen. This gives a baud rate error of 0.3/26.3 which is 1.14%; well within the ability of the asynchronous mode of operation.

Counter Mode

In the counter mode the counter/timer counts the value of the CTLR CTUR down to zero and then sets the ISR[3] bit and sets the counter/timer output from 1 to 0. It then rolls over to 65,365 and continues counting with no further observable effect.

Reading the C/T in the counter mode outputs the present state of the C/T. If the C/T is not

stopped, a read of the C/T may result in changing data on the data bus.

Timeout Mode

The timeout mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RxFIFO, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. If the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU will not be interrupted for the remaining characters in the RxFIFO.

By programming the C/T such that it would time out in just over one character time, the above situation could be avoided. The processor would be interrupted any time the data stream had stopped for more than one character time. NOTE: This is very similar to the watch dog time of MR0. The difference is in the programmability of the delay time and that the watchdog timer is restarted by either a receiver load to the RxFIFO or a system read from it.

This mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the timeout mode for that channel. Writing a 'Cx' to CRA or CRB will disable the timeout mode. The timeout mode should only be used by one channel at a time.

The timeout mode disables the regular START/STOP counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RxFIFO, the C/T is stopped after one C/T clock, reloaded with the value in CTUR and CTLR and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Since receiving a character restarts the C/T, the receipt of a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Timeout Mode On' command, CRx='Ax', will also clear the counter ready bit and stop the counter until the next character is received.

The counter timer is controlled with six commands: Start/Stop C/T, Read/Write Counter/Timer lower register and Read/Write Counter/Timer upper register. These commands have slight differences depending on the mode of operation. Please see the detail of the commands under the CTLR CTUR Register descriptions.

Receiver and Transmitter

The QUART has four full-duplex asynchronous receiver/transmitters. The operating frequency for the receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input.

Registers associated with the communications channel are the mode registers (MR0, MR1 and MR2) Clock Select Register (CSR), Command Register (CR), Status Register (SR), Transmit FIFO (TxFIFO), and the Receive FIFO (RxFIFO). The transmit and receive FIFOs are each eight characters deep. The receive FIFO also stores three status bits with each character.

Transmitter

The transmitter accepts parallel data from the CPU and converts it to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the TxFIFO, the TxD output remains high and the TxEMT bit in the SR will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character in the TxFIFO. In the 16X clock mode, this also re-synchronizes the internal 1X transmitter clock so that transmission of the new character begins with minimum delay.

If the transmitter is disabled it continues operating until the character currently being transmitted and any characters in the TxFIFO, including parity and stop bits, have been transmitted. New data cannot be loaded to the TxFIFO when the transmitter is disabled.

The transmitter can be forced to send a break (a continuous low condition) by issuing a START BREAK command via the CR register. The break is terminated by a STOP BREAK command or a transmitter reset..

The TxFIFO empty positions are encoded as a three bit number for presentation to the bidding logic. The coding will equal the number of bytes that remain to be filled. That is, a binary number of 101 will mean five bytes may be loaded; 111 means 7, etc. Eight positions will be indicated by a binary 111 *and* the FIFO empty bit will be set.

Receiver

The receiver accepts serial data on the RxD pin, converts the serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition, and presents the assembled character to the CPU via the receiver FIFO.

The receiver operates in two modes: the 1X and 16X. The 16X mode is the more robust of the two. It allows the receiver to establish a phase relation to the remote transmitter clock within 1/16 of a bit time and also allows validation of the start bit. The 1X mode does not validate the start bit and assumes that the receiver clock rising edge is centered in the data bit cell. The use of the 1X mode implies that the transmitter clock is available to the receiver.

When operating in the 16X mode and after the receiver has been enabled the receiver state machine will look for a high to low transition on the RxD input. The detection of this transition will cause the divider being driven by the 16X clock to be reset to zero and continue counting. When the counter reaches 7 the RxD input is sampled again and if still low a valid START BIT will be detected. If the RxD input is high at count 7 then an invalid start bit will have been sensed and the receiver will then look for another high to low transition and begin validating again.

When a valid start bit is detected the receiver state machine allows the 16X divider circuit to continue counting 0 to 15. Each time the receiver passes count 7 (the theoretical center of the bit time) another data bit is clocked into the receiver shift register until the proper number of bits have been received including the parity bit, if used, and 1/2 stop bit. After the STOP BIT is detected the receiver state machine will wait until the next falling edge of the X1 clock and then clock the assembled character and its status bits into the receiver FIFO on the next rising edge of the X1 clock. The delay from the detection of the STOP BIT to the loading of the character to the RxFIFO will be from one half to one and one half X1 clock periods. Receiver Status Register bits for FIFO READY, FIFO FULL, parity error, framing error, break detect will also set at this time. The most significant bits for data characters less than eight bits will be set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (i.e. framing error) and RxD remains low for one-half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled). The parity error, framing error and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set.

If a break condition is detected (RxD is low for the entire character including the stop bit), only one character consisting of all zeros will be loaded in the FIFO and the received break

bit in the SR is set to 1. The "Change of Break" bit in the ISR at position 2 or 6 is also set at this time. Note that the "Change of Break" bit will set again when the break condition terminates. The RxD input must return to a high condition for two successive clock edges of the 1X clock (internal or external) before a search for the next start bit begins.

NOTE: If the RxD input is low when the receiver is enabled and remains low for at least 9/16 of a bit time a valid start bit will be seen and data (probably random) will be clocked into the receiver FIFO. If the line remains low for a full character time plus a stop bit then a break will be detected.

Each receiver is equipped with a watchdog timer. This timer is enabled by MR0[7] and counts 64 RxC1X clocks. Its purpose is to alert the controlling CPU that data is in the FIFO which has not been read. This situation may occur at the end of a message when the last group of characters was not long enough to cause an interrupt.

RECEIVER FIFO

The RxFIFO consists of a first-in-first-out (FIFO) with a capacity of eight characters. Data is loaded from the receive shift register into the top-most empty position of the FIFO. The RxRDY bit in the status register (SR) is set whenever one or more characters are available to be read; a FFULL status bit is set if all eight stack positions are filled with data. The number of filled positions is encoded into a 3-bit value. This value is sent to the interrupt bidding logic where it is used to generate an interrupt. A read of the RxFIFO, outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits are 'popped' thus emptying a FIFO position for new data.
NOTE: The number of filled positions in the RxFIFO is coded as actual number filled positions. Seven filled will be coded as 7. Eight filled positions will be coded as 7 *and* the RxFIFO full status bit will be set.

In addition to the data word, three status bits (parity error, framing error, and received break) are appended to each data character in the FIFO. Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical OR of the status for all characters coming to the top of the FIFO since the last reset error command was issued. In either mode, reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RxFIFO is read. Therefore, the SR should be read prior to reading the corresponding data character.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exists, the contents of the FIFO are not affected: the character previously in the shift register is lost and the overrun error status bit, SR[4], will be set upon receipt of the start bit of the new (overrunning) character.

A "watchdog" timer is associated with each receiver. Its interrupt is enabled by MR0[7]. The purpose of this timer is alerting the control processor that characters are in the RxFIFO which have not been read and/or the datastream has stopped. This situation may occur at the end of a transmission when the last few characters received are not sufficient to cause an interrupt.

This counter times out after 64 bit times. It is reset each time a character is transferred from the Receive shift register to the RxFIFO or a read of the RxFIFO is executed.

WAKE-UP MODE

In addition to the normal transmitter and receiver operation described above, the QUART incorporates a special mode which provides automatic "wakeup" of a receiver through address frame (or character) recognition for multi-processor or multi-station communications. This mode is selected by programming MR1[4:3] to '11'.

In this mode of operation a 'master' station transmits an address character to the several 'slave' stations on the line. The address character is identified by setting its parity bit to 1. The slave stations will usually have their receivers partially enabled as a result of setting MR1[4:3] to 11. When the receivers see a parity bit set to one they will load that character to the RxFIFO and set the RxRDY bit in the status register. The user would usually set the receiver interrupt to occur on RxRDY as well. (All characters whose parity bits are set to 0 will be ignored). The local processor at the slave station will read the 'address' character just received. The local processor will test for an address match for this station and if match occurs it will enable the local receiver and receive the following data characters. The master will normally follow an address character(s) with data characters. Since the data characters transmitted by the master will have their parity bits set to zero, stations other than the addressed one(s) will ignore the data.

NOTE: The time between address and data fields must be enough for the local processor to test the address character and enable the receiver. At bit times approaching 10µs this may begin to be a point of concern.

A transmitted character consists of a start bit, the programmed number of data and stop bits and an "address/data" bit. The parity bit is used as the address or data indicator. The polarity of the A/D bit is selected by setting MR1[2] to zero or one; zero indicates that the current byte is data, while one indicates that the current byte is addresses. The desired polarity of the A/D bit (parity) should be programmed before the TxFIFO is loaded.

While in this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character in the RxFIFO if the received A/D bit is a one, but discards the received character if the received A/D bit is a zero. If enabled, all received characters are then transferred to the CPU via the RxFIFO. In either case, the data bits are loaded in the data FIFO while the A/D bit is loaded in the status FIFO position normally used for parity error (SR[5]). Framing error, overrun error, and break detect operate normally whether or not the receiver is enabled.

INPUT OUTPUT (I/O) PINS

There are 16 multi-use pins; four for each UART. These pins are accessed and controlled via the Input Port Register (IPR), I/O Port Control Register (I/OPCR), Input Port Change Register (IPCR), and Output Port Register (OPR). They may be individually programmed to be inputs or outputs. See Table 5.

I/O0x and I/O1x pins have change of state detectors. The change of state detectors sample the input ports every 26.04µs (with the X1 clock at 3.686400MHz) and set the change bit in the IPCR if the pin has changed since it was last read. Whether the pins are programmed as inputs or outputs the change detectors still operate and report changes accordingly. See the register descriptions of the I/O ports for the detailed use of these features.

Interrupt Priority System

The interrupt control for the QUART has been designed to provide very low interrupt service overhead for the controlling processor while maintaining a high degree of flexibility in setting the importance of interrupts generated in different functional blocks of the device.

This is accomplished by allowing each function of the QUART (18 total) which may cause an interrupt to generate a variable numeric code which contains the identity of the source, channel number and severity level. This code is compared (at the X1 clock rate or the X1 clock rate divided by 2) to an interrupt threshold. When the interrupting source generates a code that is numerically greater than the interrupt threshold the IRQN is asserted

This is referred to as the bidding process. The winning bid contains, in different fields, all the characteristics of the winning bidder.

This data may be used in several ways to steer the controlling processor to the proper type and amount of service required (usually the amount of service refers to the number of bytes written to the transmitter or read from the receiver). Access to the winning bid is provided via the CIR (Current Interrupt Register), interrupt vectors, modified interrupt vectors and Global registers.

Functional Description of the Interrupt Arbitration

The QUART contains eighteen sources which may cause an interrupt:

1. Four receiver data FIFO filled functions.
2. Four receiver BREAK detect functions.
3. Four transmitter FIFO space available functions.
4. Four "Change of State" detectors.
5. Two counter/timers.

The interrupt logic at each source produces a numeric code that identifies its interrupt priority condition currently pending. This code is compared to a programmable Interrupt Threshold via the arbitration logic which determines if the IRQN should be asserted. The arbitration logic only judges those possible interrupt sources which have been allowed to bid via the IMR (Interrupt Mask Register).

The arbitration logic produces a value which is the concatenation of the channel number, interrupt type, FIFO fill level and user-defined fields. The channel number and interrupt type fields are hardwired. During the "bid arbitration" process all bids from enabled sources are presented, simultaneously, to an internal interrupt bus. The bidding system and formats are discussed in more detail in following sections.

The interrupt arbitration logic insures that the interrupt with the numerically largest bid value will be the only source driving the interrupt bus at the end of the arbitration period. The arbitration period follows the period of the X1 clock. The maximum speed is 4.0MHz. If a higher speed X1 clock is used then the X1 clock "divide by 2" feature must be used.

The value of the winning bid determined during the arbitration cycle is compared to the "Interrupt Threshold" contained in the ICR (Interrupt Control Register). If the winning bid exceeds the value of the ICR the IRQN is asserted.

Priority Arbitration and Bidding

Each of the five "types" of interrupts has slightly different "bid" value, as follows:

Receivers

# rcv'd	rEr	1	1	Chan #
3	1	1	1	2

Transmitters

0	# avail	1	0	Chan #
1	3	1	1	2

Break Detect

Programmable	1	0	0	Chan #
3	1	1	1	2

Change of State

Programmable	0	0	1	Chan #
3	1	1	1	2

Counter/Timer

Programmable	0	1	0	1	Chan #
2	1	1	1	1	2

Bits shown above as '0' or '1' are hard-wired inputs to the arbitration logic. Their presence allows determination of the interrupt type and they insure that no bid will have a value of all zeros (a condition that is indistinguishable from not bidding at all). They also serve to set a default priority among the non-receive/transmit types when the programmable fields are all zeros.

The channel number always occupies the two LSBs. Inclusion of the channel number insures that a bid value generated will be unique and that a single "winner" will drive the Interrupt Bus at the end of the arbitration interval. The channel number portion of each UARTs bid is hard-wired with UARTa being channel number 0 and so forth.

As can be seen above, bits 4:2 of the winning bid value can be used to identify the type of interrupt, including whether data was received correctly or not. Like the Channel number field, these bits are hard-wired for each interrupt source.

The "# rcv'd" and "# avail" fields indicate the number of bytes present in the receiver FIFO and the number of empty bytes in the transmitter FIFO, respectively.

NOTE: When there are zero bytes in the receiver's FIFO, it does NOT bid. Similarly, a full transmitter FIFO makes NO bid. In the case where all bids have been disabled by the Interrupt Mask Register or as a result of their byte counts, the active-low Interrupt Bus will return FFh. This value always indicates no interrupt source is active and IRQN will be negated.

The high order bit of the transmitter "bid" is always zero. An empty transmit FIFO is, therefore, fixed at a lower interrupt priority than a 1/2 full receive FIFO. Bit 4 of a receiver bid is the Receiver Error Bit (RER). The RER is the OR of the parity, framing and overrun error conditions. The RER does little to modify the priority of receiver interrupts vs. transmitter interrupts. It is output to the Interrupt Bus to allow inclusion of good data vs. problem data information in the Current Interrupt Register.

The high order bits of bids for received break, CoS (Change of State) and Counter/Timer events are all programmable. By programming ones in these fields, the associated interrupt source can be made more significant than most receiver and all transmitter interrupts. Values near zero in these fields makes them lower priority classes of interrupt.

As shown in Figure 5, the bid arbitration process is controlled by the EVAL/HOLDN signal derived from the oscillator clock.

Receipt of an IACKN signal from the host MPU latches the latest "winning bid" from the latched Interrupt Bus into the Current Interrupt Register (CIR). This logic is diagrammed in Figure 6.

If the IACKN falling edge of Figure 5 occurs during EVAL time, the result from the last arbitration (captured by the Interrupt Bus latches) is stored in CIR. Otherwise, the next EVAL pulse is inhibited and the value in the Interrupt Bus Latches is stored in CIR.

Clearing the Interrupt

Activities which change the state of the ISR will cause the IRQN to assert or negate. In addition, the accessing of a global or local RxFIFO or TxFIFO reduces the associated byte count for transmitter and receiver data interrupts. If the byte count falls below the threshold value, the interrupt request is withdrawn. Other interrupt conditions are cleared when the interrupting source is cleared.

Once the interrupt is cleared, the programmable value lowered or its byte count value reduced by one of the methods listed above, a different bidder (or no bidder at all) will win the on-going arbitration. When the winning bid drops below the Interrupt Threshold Register's value, the IRQN pin will negate.

Arbitration - Aftermath

At the end of the arbitration, i.e., the falling edge of EVAL, the winning interrupt source is driving its Channel number, number of bytes (if applicable) and interrupt type onto the Interrupt Bus. These values are captured into a latch by the trailing edge of EVAL. The output of this latch is used by the Interrupt Threshold comparator; the winning value is

captured into another set of latches called the Current Interrupt Register (CIR) at the time of an Interrupt Acknowledge cycle or execution of the "Update CIR" command.

The Current Interrupt Register and associated read logic is shown in Figure 6. Interrupting channel number and the three bit interrupt type code and FIFO fill level are readable via the Internal Data Bus.

The contents of the appropriate receiver or transmitter byte "counter", as captured at the time of IACKN assertion, make up bits 7:5 of the CIR. If the interrupt type stored in the Current Interrupt Register is not a receiver or transmitter data transfer type, the CIR7:5 field will read as the programmable fields of their respective bid formats.

The buffers driving the CIR to the DBUS also provide the means of implementing the Global Interrupting Channel and Global Byte Count Registers, described in a later section.

The winning bid channel number and interrupt type fields can also be used to generate part of the Interrupt Vector, as defined by the Interrupt Control Register.

Interrupt Context

The channel number of the winning "bid" is used by the address decoders to provide data from the interrupting UART channel via a set of Global pseudo-registers. The interrupt Global pseudo-registers are:

1. Global Interrupting Byte Count
2. Global Interrupting Channel
3. Global Receive Holding Register
4. Global Transmit Holding Register

The first two Global "registers" are provided by Current Interrupt Register fields as shown in Figure 6. The interrupting channel number latched in CIR modifies address decoding so that the Receive or Transmit Holding Register for the interrupting channel is accessed during I/O involving the Global Receive and Transmit Holding Registers. Similarly, for data interrupts from the transmitter and receiver, the number of characters available for transfer to the CPU or the number of transmit FIFO positions open is available by reading the Global Interrupt Byte Count Register. For non-data interrupts, a read of the Global Interrupt Byte Count Register yields a value equal to the highest programmable filed.

In effect, once latched by an IACK or the Update CIR command, the winning interrupt channel number determines the contents of the global registers. All Global registers will provide data from the interrupting UART channel.

Interrupt Threshold Calculation

The state of IRQN is determined by comparison of the winning "bid" value to the Interrupt Threshold field of the Interrupt Control Register.

The logic of the bidding circuit is such that when no interrupt source has a value greater than the interrupt threshold then the interrupt is not asserted and the CIR (Current Interrupt Register) is set to all ones. When one or more of the 18 interrupt sources which are enabled via the IMR (Interrupt Mask Register) exceed the threshold then the interrupt threshold is effectively disconnected from the bidding operation while the 18 sources now bid against each other. The final result is that the highest bidding source will disable all others and its value will be loaded to the CIR and the IRQN pin asserted low. This all occurs during each cycle of the X1,X2 crystal clock.

INTERRUPT NOTE ON 68C94:

For the receivers and transmitters, the bidding of any particular unit may be held off unless one of four FIFO fill levels is attained. This is done by setting the RxINT and TxINT bits in MR0 and MR1 to non-zero values. This may be used to prevent a receiver or transmitter from generating an interrupt even though it is filed above the bid threshold. Although this is not in agreement with the idea that each enabled interrupt source bid with equal authority, it does allow the flexibility of giving particular receiver or transmitters more interrupt importance than others.

This may be used when the Interrupt Threshold is set at or above 100000. Note than in this case the transmitter cannot generate an interrupt. If the Interrupt threshold MSBs were set to 011 *and* the 'Receiver Interrupt Bits' on the MR registers set to a value other than 00 then the RxFIFO could not generate and interrupt until it had 4, 6 or 8 bytes. This in effect partially defeats the hardwired characteristic that the receiver interrupts should have more importance than the transmitter. This characteristic has been implemented by setting the MSB of the transmitter bid to zero.

RECEIVER INPUT FILL LEVEL

MR0[6]	MR1[6]	Interrupt Condition
0	0	1 or more bytes in FIFO (Rx RDY) default
0	1	6 or more bytes in FIFO
1	0	4 or more bytes in FIFO
1	1	8 or more bytes in FIFO (Rx FULL)

MR0[5:4] – Tx Interrupt fill level

MR0[5]	MR0[4]	Interrupt Condition
0	0	8 bytes empty (Tx EMPTY) default
0	1	4 or more bytes empty
1	0	6 or more bytes empty
1	1	1 or more bytes empty (Tx RDY)

Vectored Interrupts

The QUART responds to an Interrupt Acknowledge (IACK) initiated by the host MCU by providing an Interrupt Acknowledge Vector on D7:0. The interrupt acknowledge cycle is terminated with a DACKN pulse. The vector provided by the QUART can have one of the three forms under control of the IVC control field (bits 1:0 of the Interrupt Control Register):

With IVC = 00 (IVR only)

IVR7:0
8

With IVC = 01 (channel number)

IVR7:2	Chan #
6	2

With IVC = 10 (type & channel number)

IVR7:5	Type	Chan #
3	3	2

A code of 11 in the Interrupt Vector Control Field of the ICR results in NO interrupt vector being generated. The external data bus will be held in a high impedance state throughout the IACK cycle. A DACKN will be generated normally for the IACK cycle, however.

NOTE: If IACKN is not being used then the command "UPDATE CIR" must be issued for the global and interrupt registers to be updated.

PROGRAMMING UART CONTROL REGISTERS

The operation of the QUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. Addressing of the registers is described in Table 1.

The bit formats of the QUART registers are depicted in Table 2.

Table 2. Register Bit Formats, DUART AB. [duplicated for DUART CD]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

MR0 (Mode Register 0)

Rx Watchdog Timer	RxINT2 bit	TxINT Control	These bits not implemented. They should be considered Reserved.			
0 = off 1 = on	These bits should normally be set to 0		x	x	x	x

MR1 (Mode Register 1)

RxRTS Control	RxINT1 Select	Error Mode	Parity Mode	Parity Type	Bits per Character
0 = No 1 = Yes	Normally set to 0	0 = Char 1 = Block	00 = With parity 01 = Force parity 10 = No parity 11 = Special mode	0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8

MR2 (Mode Register 2)

Channel Mode	TxRTS Control	CTS Enable Tx	Stop Bit Length*
00 = Normal 01 = Auto-echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 4 = 0.813 8 = 1.563 C = 1.813 1 = 0.625 5 = 0.875 9 = 1.625 C = 1.875 2 = 0.688 6 = 0.938 A = 1.688 E = 1.938 3 = 0.750 7 = 1.000 B = 1.750 F = 2.000

NOTE:
Add 0.5 to values shown above for 0–7, if channel is programmed for 5 bits/char.

CSR (Clock Select Register)

Receiver Clock Select	Transmitter Clock Select
See text	See text

CR (Command Register)

Miscellaneous Commands	Disable Tx	Enable Tx	Disable Rx	Enable Rx
See text	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
Issuing commands contained in the upper four bits of the "Command Register" should be separated in time by at least three (3) X1 clock edges. Allow four (4) edges if the "X1 clock divide by 2" mode is used.

SR (Status Register)

Rec'd. Break	Framing Error	Parity Error	Overrun Error	TxEMT	TxRDY	FFULL	RxRDY
0 = No 1 = Yes *	0 = No 1 = Yes *	0 = No 1 = Yes *	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
These status bits are appended to the corresponding data character in the receive FIFO. A read of the status register provides these bits [7:5] from the top of the FIFO together with bits [4:0]. These bits are cleared by a reset error status command. Unless reset with the 'Error Reset' (CR command 40) or receiver reset, these bits will remain active in the Status Register after the RxFIFO is empty.

Table 2. Register Bit Formats, Duart ab. [duplicated for Duart cd] (continued)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

ACR (Auxiliary Control Register)

BRG Set Select	Counter/Timer Mode and Source	Delta I/O1b	Delta I/O0b	Delta I/O1a	Delta I/O0a
0 = set 1 1 = set 2	See text	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on

IPCR (Input Port Change Register)

Delta I/O1b	Delta I/O0b	Delta I/O1a	Delta I/O0a	I/O1b	I/O0b	I/O1a	I/O0a
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

ISR (Interrupt Status Register)

I/O Port Change	Delta BREAKb	RxRDY/ FFULLb	TxRDYb	Counter Ready	Delta BREAKa	RxRDY/ FFULLa	TxRDYa
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

IMR (Interrupt Mask Register)

I/O Port Change INT	Delta BREAKb INT	RxRDY/ FFULLb INT	TxRDYb INT	Counter Ready INT	Delta BREAKa INT	RxRDY/ FFULLa INT	TxRDYa INT
0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on

CTUR (Counter/Timer Upper Register)

C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]

CTUR (Counter/Timer Lower Register)

C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]

IPR (Input Port Register)

I/O3b	I/O2b	I/O3a	I/O2a	I/O1b	I/O0b	I/O1a	I/O0a
0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

Mode Registers 0, 1 and 2

The addressing of the Mode Registers is controlled by the MR Register pointer. On any access to the Mode Registers this pointer is always incremented. Upon reaching a value of 2 it remains at 2 until changed by a CR command or a hardware reset.

MR0 – Mode Register 0

Mode Register 0 (MR0) is part of the UART configuration registers. It controls the watch dog timer and the encoding of the number of characters received in the RxFIFO. The lower four bits of this register are not implemented in the hardware of the chip. MR0 is normally set to either 80h or 00h. A read of this register will return 1111 (Fh) in the lower four bits.

The MR0 register is accessed by setting the MR Pointer to zero (0) via the command register command 1011 (Bh).

MR0[7]: This bit enables or disables the RxFIFO watch dog timer.

MR0[7] = 1 enable timer

MR0[7] = 0 disable timer

MR0[6:4]: These bits are normally set to 0 except as noted in the "Interrupt Threshold Calculation" description

MR0[3:0]: These bits are not implemented in the chip. These bits should be be considered "reserved."

MR1 – Mode Register 1

MR1 is accessed when the MR pointer points to MR1. The pointer is set to MR1 by RESET, a set pointer command applied via the CR or after an access to MR0. After reading or writing MR1, the pointers are set at MR2.

MR1[7] – Receiver Request-to-Send Flow Control

This bit controls the deactivation of the RTSN output (I/O2x) by the receiver. This output is manually asserted and negated by commands applied via the command register. MR1[7] = 1 causes RTSN to be automatically negated upon receipt of a valid start bit if the

receiver FIFO is full. RTSN is re-asserted when an empty FIFO position is available. This feature can be used to prevent overrun in the receiver by using the RTSN output signal to control the CTS input (the QUART I/O0 pin) of the transmitting device.

Use of this feature requires the I/O2 pin to be programmed as output via the I/OPCR and to be driving a 0 via the OPR. When the RxFIFO is full and the start bit of the ninth character is sensed the receiver logic will drive the I/O2 pin high. This pin will return low when another RxFIFO position is vacant.

MR1[6] – Receiver Interrupt Select 1
This bit is normally set to 0 except as noted in the "Interrupt Threshold Calculation" description. MR1[6] operates with MR0[6] to prevent the receiver from bidding until a particular fill level is attained. For software compatibility this bit is designed to emulate the RxFIFO interrupt function of previous Signetics UARTs.

MR1[5] – Error Mode Select
This bit selects the operating mode of the eight FIFOed status bits (FE, PE, received break). In the character mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO.

In the block mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last reset error command was issued.

In the "Block Error" mode the ORing of the error status bits and the presentation of them to the status register takes place as the bytes enter the RxFIFO. This allows an indication of problem data when the error occurs after the leading bytes have been received. In the character mode the error bits are presented to the status register when the corresponding byte is at the top of the FIFO.

MR1[4:3] – Parity Mode Select
If "with parity" or "force parity" is selected, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR1[4:3] = 11 selects the channel to operate in the special wake-up mode (see page 10).

MR1[2] – Parity Type Select
This bit selects the parity type (odd or even) if the "with parity" mode is programmed by MR1[4:3], and the polarity of the forced parity bit if the "force parity" mode is programmed. It has no effect if the "no parity" mode is programmed. In the special "wake-up" mode, it selects the polarity of the transmitted A/D bit.

MR1[1:0] – Bits per Character Select
This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2 – Mode Register 2

MR2 is accessed when the channel MR pointer points to MR2, which occurs after any access to MR1. Accesses to MR2 do not change the pointer.

MR2[7:6] – Mode Select
The QUART can operate in one of four modes. MR2[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is re-clocked and retransmitted on the TxD output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e., transmitted parity bit is as received.

Two diagnostic modes can also be selected. MR2[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxD output is held high.
4. The RxD input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2[7:6] = 11. In this mode:

1. Received data is re-clocked and retransmitted on the TxD output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., the transmitted parity bit is as received.
5. The receiver must be enabled, but the transmitter need not be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected, the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes; if the deselection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop bit has been retransmitted.

MR2[5] – Transmitter Request-to-Send Control

NOTE: When the transmitter controls the I/O2 pin (usually used for the RTSN signal) the meaning of the pin is not RTSN at all! Rather it signals that the transmitter has finished transmission. (i.e., end of block).

This bit controls the deactivation of the RTSN output (I/O2) by the transmitter. This output is manually asserted and negated by appropriate commands issued via the command register. MR2[5] = 1 causes RTSN to be reset automatically one bit time after the characters in the transmit shift register and in the TxFIFO (if any) are completely transmitted (includes the programmed number of stop bits if the transmitter is not enabled). This feature can be used to automatically terminate the transmission as follows:

1. Program auto-reset mode: MR2[5] = 1.
2. Enable transmitter.
3. Assert RTSN via command.
4. Send message.
5. Verify the next to last character of the message is being sent by waiting until transmitter ready is asserted. Disable transmitter after the last character of the message is loaded in the TxFIFO.
6. The last character will be transmitted and RTSN will be reset one bit time after the last stop bit.

MR2[4] – Transmitter Clear-to-Send Flow Control
The sate of this bit determines if the CTSN input (I/O0) controls the operation of the transmitter. If this bit is 0, CTSN has no effect on the transmitter. If this bit is a 1, the transmitter checks the sate of CTSN each time it is ready to send a character. If it is asserted (Low), the character is transmitted. If it is negated (High), the TxD output remains in the marking state and the transmission is delayed until CTSN goes Low. Changes in CTSN, while a character is being transmitted do not affect the transmission of that character. This feature can be used to prevent overrun of a remote receiver.

MR2[3:0] – Stop Bit Length Select
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1–9/16 to 2 bits, in increments of 1/16 bit, can be programmed

for character lengths of 6, 7, and 8 bits. For a character length of 5 bits, 1–1/16 to 2 stop bits can be programmed in increments of 1/16 bit. If an external 1X clock is used for the transmitter, MR2[3] = 0 selects one stop bit and MR2[3] = 1 selects two stop bits to be transmitted.

RECEIVER NOTE: In all cases, the receiver only checks for a "mark" condition at the center of the stop bit (1/2 to 9/16 bit time into the stop bit position). At this time the receiver has finished processing the present character and is ready to search for the start bit of the next character.

CSR – Clock Select Register

CSR[7:4] – Receiver Clock Select
When using a 3.6864MHz crystal or external clock input, this field selects the baud rate clock for the receiver as shown in Table 3.

The receiver clock is always a 16X clock, except for CSR[7:4] = 1111. I/O2x is external input.

CSR[3:0] – Transmitter Clock Select
This field selects the baud rate clock for the transmitter. The field definition is as shown in Table 3, except as follows:

CSR[3:0]	ACR[7] = 0	ACR[7] = 1
1 1 1 0	I/O3x – 16X	I/O3x – 16X
1 1 1 1	I/O3x – 1X	I/O3x – 1X

Table 3. Baud Rate

	BRG RATE = LOW		BRG RATE = HIGH		TEST 1 = 1	
CSR[7:4]	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0 0 0 0	50	75	50	450	4,800	7,200
0 0 0 1	110	110	110	110	880	880
0 0 1 0	134.5	38.4k	134.5	230.4K	1,076	38.4K
0 0 1 1	200	150	200	900	19.2K	14.4K
0 1 0 0	300	300	1800	1,800	28.8K	28.8K
0 1 0 1	600	600	3,600	3,600	57.6K	57.6K
0 1 1 0	1,200	1,200	7,200	7,200	115.2K	115.2K
0 1 1 1	1,050	2,000	1,050	2,000	1,050	2,000
1 0 0 0	2,400	2,400	14.4K	14.4K	57.6K	57.6K
1 0 0 1	4,800	4,800	28.8K	28.8K	4,800	4,800
1 0 1 0	7,200	1,800	7,200	1,800	57.6K	14.4K
1 0 1 1	9,600	9,600	57.6K	57.6K	9,600	9,600
1 1 0 0	38.4k	19.2k	230.4K	115.2K	38.4K	19.2K
1 1 0 1	Timer	Timer	Timer	Timer	Timer	Timer
1 1 1 0	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X
1 1 1 1	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X

CR – Command Register

CR is used to write commands to the QUART.

CR[7:4] – Miscellaneous Commands
Issuing commands contained in the upper four bits of the "Command Register" should be separated in time by at least three (3) X1 clock edges. Allow four (4) edges if the "X1 clock divide by 2" mode is used. The encoded value of this field can be used to specify a single command as follows:

0000 No command.

0001 Reset MR pointer. Causes the MR pointer to point to MR1.

0010 Reset receiver. Resets the receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO pointer is reset to the first location.

0011 Reset transmitter. Resets the transmitter as if a hardware reset had been applied.

0100 Reset error status. Clears the received break, parity error, framing error, and overrun error bits in the status register (SR[7:4]). Used in character mode to clear OE status (although RB, PE, and FE bits will also be cleared), and in block mode to clear all error status after a block of data has been received.

0101 Reset break change interrupt. Causes the break detect change bit in the interrupt status register (ISR[2 or 6]) to be cleared to zero.

0110 Start break. Forces the TxD output low (spacing). If the transmitter is empty, the start of the break condition will be delayed up to two bit times. If the transmitter is active, the break begins when transmission of the character is completed. If a character is in the TxFIFO, the start of break is delayed until that character or any others loaded after it have been transmitted (TxEMT must be true before break begins). The transmitter must be enabled to start a break

0111 Stop break. The TxD line will go high (marking) within two bit times. TxD will remain high for one bit time before the next character, if any, is transmitted.

1000 Assert RTSN. Causes the RTSN output to be asserted (Low).

1001 Negate RTSN. Causes the RTSN output to be negated (High).

1010 Set Timeout Mode On. The register in this channel will restart the C/T as each receive character is transferred from the shift register to the RxFIFO. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset.

1011 Set MR Pointer to 0.

1100 Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued.

1101 Reserved.

111x Reserved for testing.

CR[3] – Disable Transmitter
This command terminates transmitter operation and resets the TxRDY and TxEMT status bits. However, if a character is being transmitted or if a character is in the TxFIFO

when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CR[2] – Enable Transmitter
Enables operation of the transmitter. The TxRDY and TxEMT status bits will be asserted.

CR[1] – Disable Receiver
This command terminates operation of the receiver immediately – a character being received will be lost. However any unread characters in the RxFIFO area are still available. Disable is not the same as a "receiver reset". With a receiver reset any characters not read are lost. The command has no effect on the receiver status bits or any other control registers. If the special wake–up mode is programmed, the receiver operates even if it is disabled (see Wake-up Mode).

CR[0] – Enable Receiver
Enables operation of the receiver. If not in the special wake-up mode, this also forces the receiver into the search for start bit state.

SR – Channel Status Register

SR[7] – Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received; further entries to the FIFO are inhibited until the RxDA line returns to the marking state for at least one-half bit time (two successive edges of the internal or external 1x clock).

When this bit is set, the change in break bit in the ISR (ISR[6 or 2]) is set. ISR[6 or 2] is also set when the end of the break condition, as defined above, is detected. The break detect circuitry is capable of detecting breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must last until the end of the next character in order for it to be detected.

SR[6] – Framing Error (FE)
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SR[5]– Parity Error (PE)
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity. In special 'wake-up mode', the parity error bit stores the received A/D (Address/Data) bit.

SR[4] – Overrun Error (OE)
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost. This bit is cleared by a reset error status command.

SR[3] – Transmitter Empty (TxEMT)
This bit will be set when the transmitter underruns, i.e., both the TxFIFO and the transmit shift register are empty. This bit and TxRDY are set when the transmitter is first enabled and any time it is re-enabled after either, (a) reset, or (b) the transmitter has assumed the disabled state. It is set after transmission of the last stop bit of a character, if no character is in the TxFIFO awaiting transmission. It is reset when the TxFIFO is loaded by the CPU, a pending transmitter disable is executed, the transmitter is reset, or the transmitter is disabled in the underrun condition.

SR[2] – Transmitter Ready (TxRDY)
This bit, when set, indicates that the TxFIFO has at least one empty location that may be loaded by the CPU. It sets when the transmitter is first enabled. It is cleared when the TxFIFO is full (eight bytes); the transmitter is reset; a pending transmitter disable is executed; the transmitter is disabled when it is in the underrun condition. When this bit is **not** set characters written to the TxFIFO will not be loaded or transmitted; they are lost.

SR[1] – RxFIFO Full (FFULL)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all eight FIFO positions are occupied. It is reset when the CPU reads the FIFO and there is no character in the receive shift register. If a character is waiting in the receive shift register because the FIFO is full, FFULL is not reset after reading the FIFO once.

SR[0] – RxFIFO Ready (RxRDY)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RxFIFO, and no more characters are in the FIFO.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects between two sets of baud rates that are available within each baud rate group generated by the BRG. See Table 3.

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.

Set 2: 75, 110, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, 19.2k, and 38.4k baud.

The selected set of rates is available for use by the receiver and transmitter.

ACR[6:4] – Counter/Timer Mode and Clock Source Select
This field selects the operating mode of the counter/timer and its clock source (see Table 4).

The I/O pins available for counter/timer clock source is I/O1a and I/O1c. The counter/timer clock selection is connected to the I/O1 pin and will accept the signal on this pin regardless of how it is programmed by the I/OPCR. (see Figure 2).

Table 4. ACR[6:4] C/T Clock and Mode Select

[6:4]	Mode	Clock Source
0 0 0	Counter	I/O1 pin
0 0 1	Counter	I/O1 pin divided by 16
0 1 0	Counter	TxC–1X clock of the transmitter
0 1 1	Counter	Crystal or external clock (X1/CLK) divided by 16
1 0 0	Timer	I/O1 pin
1 0 1	Timer	I/O1 pin divided by 16
1 1 0	Timer	Crystal or external clock (X1/CLK)
1 1 1	Timer	Crystal or external clock (X1/CLK) divided by 16

ACR[3:0] – I/O1b, I/O0b, I/O1a, I/O0a Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register, ISR[7], to be set and thus allow the Change of State Detectors to enter the bidding process. If a bit is in the 'on' state, the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which may result in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7:4] – I/O1b, I/O0b, I/O1a, I/O0a Change-of-State
These bits are set when a change of state, as defined in the Input Port section of this data sheet, occurs at the respective pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – I/O1b, I/O0b, I/O1a, I/O0a Change-of-State
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR – Interrupt Status Register

Important: The setting of these bits and those of the IMR are essential to the interrupt bidding process.

This register provides the status of all potential interrupt sources. The contents of this register are masked by the interrupt mask register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', then the interrupt source represented by this bit is allowed to enter the interrupt arbitration process. It will generate an interrupt (the assertion of INTRN low) only if its bid exceeds the interrupt threshold value. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR; the true status is provided regardless of the contents of the IMR.

ISR[7] – I/O Change-of-State
This bit is set when a change-of-state occurs at the I/O1b, I/O0b, I/O1a, I/O0a input pins. It is reset when the CPU reads the IPCR.

ISR[6] – Channel b Change in Break
This bit, when set, indicates that the receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a reset break change interrupt command.

ISR[5] – Receiver Ready or FIFO Full Channel b
Normally the ISR[5] bit being set to one indicates the RxFIFO is filled with one or more bytes and/or the receiver watch dog timer (when enabled) has timed out.

The meaning of ISR[5] is controlled by the MR0[6] and MR1[6] bits which are normally set to 00. The ISR[5] bit setting to one allows the receiver to present its bid to the arbitration logic. This function is explained in the "Interrupt Note On 68C94" and under the "Receiver Interrupt Fill Level".

ISR[5], if set, will reset when the RxFIFO is read. If the reading of the FIFO does not reduce the fill level below that determined by the MR bits, then ISR[5] sets again within two X1 clock times. Further, if the MR fill level is set at 8 bytes AND there is a byte in the receiver shift register waiting for an empty FIFO location, then a read of the RxFIFO will cause ISR[5] to reset. It will immediately set again upon the transfer of the character in the shift register to the FIFO.

ISR[4] – Transmitter Ready Channel b
The function of this bit is programmed by MR0[5:4] (normally set to 00). This bit is set when ever the number of empty TxFIFO positions exceeds or equals the level programmed in the MR0 register. This condition will almost always exist when the transmitter is first enabled. It will reset when the empty TxFIFO positions are reduced to a level less than that programmed in MR0[5:4] or the transmitter is disabled or reset.

The ISR[4] bit will reset with each write to the TxFIFO. If the write to the FIFO does not bring the FIFO above the fill level determined by the MR bits, the ISR[4] bit will set again within 2 X1 clock times.

NOTE: The setting of ISR[4] is necessary for the transmitter to generate an interrupt. It does **not** mean the transmitter **is** generating an interrupt.

ISR[3] – Counter Ready
In the counter mode of operation, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command. It is initialized to '0' when the chip is reset.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time the C/T reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the C/T.

ISR[2] – Channel a Change in Break
This bit, when set, indicates that the receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a reset break change interrupt command.

ISR[1] – Receiver Ready or FIFO Full Channel a
See the description of ISR[5]. The channel 'a' receiver operation is the same as channel 'b'.

ISR[0] – Transmitter Ready Channel a
See the description of ISR[4]. Channel "a" transmitter operates in the same manner as channel "b."

IMR – Interrupt Mask Register

The programming of this register selects which interrupt sources will be allowed to enter the interrupt arbitration process. This register is logically ANDED with the interrupt status register. Its function is to allow the interrupt source it represents to join the bidding process if the corresponding IMR and ISR bits are both 1. It has no effect on the value in the ISR. It does not mask the reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is H'0002'. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half-periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read address at A5–A0 0Eh for C/T ab or read address 1Eh for C/T cd). After this, while in timer mode, the C/T will run continuously. Receipt of a subsequent start counter command causes the C/T to terminate the current timing cycle and to begin a new cycle using the values in the CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a "Stop Counter" command (read address at A5–A0 0Fh for C/T ab or read address 1Fh for C/T cd). The command, however, does not stop the C/T. It only resets the ISR[3] bit; the C/T continues to run. The ISR[3] bit will set again as the counter passes through 0. The generated square wave is output on an I/O pin if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded in CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching the terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set. The counter rolls over to 65535 and continues counting until stopped by the CPU. If I/O is programmed to be the output of the C/T, the output remains High until the terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command. If new values have not been loaded, the previous values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower eight bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower eight bits to the upper eight bits occurs between the times that both halves of the counter is read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

I/O LOGIC

The QUART has four I/O pins for each channel. These pins may be individually programmed as an input or output under control of the I/OPCR (I/O Port Control Register). Functions which may use the I/O pins as inputs (Rx or Tx external clock, for example) are always sensitive to the signal on the I/O pin regardless of it being programmed as an input or an output. For example if I/O1a was programmed to output the RxC1X clock and the Counter/Timer was programmed to use I/O pin as its clock input the result would be the Counter/Timer being clocked by the RxC1X clock.

The 16 I/O ports are accessed and/or controlled by five (5) registers: IPR, ACR, I/OPCR, IPCR, OPR. They are shown in Table 5 of this document. Each UART has four pins. Two of these pins have "Change of State Detectors" (COS). These detectors set whenever the pin to which they are attached changes state. (1 to 0 or 0 to 1) The "Change of State Detectors" are enabled via the ACR. When enabled the COS devices may generate interrupts via the IMR and IPCR registers. Note that when the COS interrupt is enabled that any one or more of the four COS bits in the IPCR will enable the COS bidding. Each of the channel's four I/O lines are configured as inputs on reset.

The Change of State detectors sample the I/O pins at the rate of the 38.4KHz clock. A change on the pin will be required to be stable for at least 26.04µs and as much as 52.08µs for the COS detectors to confirm a change. Note that changes in the X1/clock frequency will effect this stability requirement.

Table 5.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

IPCR (Input Port Change Register ab) The lower four bits replicate the lower four bits of the IPR. The upper four bits reads state of Change detectors. Change detectors are enabled in ACR[3:0]. (DUART ab)

Delta I/O1b	Delta I/O0b	Delta I/O1a	Delta I/O0a	I/O1b	I/O0b	I/O1a	I/O0a
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

IPCR (Input Port Change Register cd) The lower four bits replicate the lower four bits of the IPR. The upper four bits reads state of Change detectors. Change detectors are enabled in ACR[3:0]. (DUART cd)

Delta I/O1d	Delta I/O0d	Delta I/O1c	Delta I/O0c	I/O1d	I/O0d	I/O1c	I/O0c
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

I/OPCR (I/O Port Configuration Register) One register for each UART.

I/O3x CONTROL	I/O2x CONTROL	I/O1x CONTROL	I/O0x CONTROL
Two bits for each I/O pin. See Figure 2.			

This register controls the configuration of the I/O ports. It defines them as inputs or outputs and controls what sources will drive them in the case of outputs or which functions they will drive when used as an input. Each pin has four functions and hence two bits to control it. Each UART has one eight bit register to control its four I/O ports.

OPR (Output Port Register cd) for DUART cd

I/O3d	I/O2d	I/O3c	I/O2c	I/O1d	I/O0d	I/O1c	I/O0c
One bit for each pin. When I/O pins are configured as "General Purpose Outputs" the pins will be driven to the complement value of its associated OPR bit.							

OPR (Output Port Register ab) for DUART ab

I/O3a	I/O2b	I/O3a	I/O2a	I/O1b	I/O0b	I/O1a	I/O0a
One bit for each pin. When I/O pins are configured as "General Purpose Outputs" the pins will be driven to the complement value of its associated OPR bit.							

This register contains the data for the I/O ports when they are used as 'General Purpose Outputs'. The bits of the register are controlled by writing to the hex addresses at 0C and 1C. Ones written to the OPR drive the pins to 0; zeros drive the pins to 1. (The pins drive the value of the complement data written to the OPR)

IPR (Input Port Register cd) Reads I/O pins for DUART cd

I/O3d	I/O2d	I/O3c	I/O2c	I/O1d	I/O0d	I/O1c	I/O0c
0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

IPR (Input Port Register ab) Reads I/O pins for DUART ab

I/O3a	I/O2b	I/O3a	I/O2a	I/O1b	I/O0b	I/O1a	I/O0a
0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

This register reads the state of the 'I/O Ports'. The state of the I/O ports is read regardless of being programmed as inputs or outputs. The IPR can be thought of a just another 8 bit parallel port to the system data bus. The lower four bits of this register are replicated in the lower four bits of the IPCR register.

I/OPCR7 I/OPCR6	I/OPCR5 I/OPCR4	I/OPCR3 I/OPCR2	I/OPCR1 I/OPCR0
I/O3x Control 00 = GPI or TxC in 01 = OPR3 out 10 = TxC16X out 11 = TxC1X out	**I/O2x Control** 00 = GPI or RxC in 01 = OPR2 (Note 1) 10 = RxC1X out 11 = RxC16X out	**I/O1x Control** 00 = C/T in (Note 2) 01 = OPR1 out 10 = (Note 3) 11 = RxC1X out	**I/O0x Control** 00 = GPI or CTS in 01 = OPR0 out 10 = TxC1X out 11 = TxC16X out

Note 1: Bit 2 of the OPR is the Request to Send function that is affected by the Assert and Negate RTS commands in CRA or CRB, and by the TxRTS feature if MR2x5 is 1, as well as by writing OPR. The RxRTS function, which is activated if MR1x7 is 1, does not affect OPR2 but merely blocks the output signal whenever the Rx FIFO is full.

Note 2: Similar to the other three pins, a 00 value in this field makes the I/O1 pin an input. I/O1 can always be used as a General Purpose Input (GPI). I/O1a and I/O1c can be used as CTI depending on how ACR6:4 is programmed. If O/PCR[7:6] is not 00, I/O1 can be used as TxC depending on how CSRx[3:0] is programmed.

Note 3: A 10 value in this field makes I/O1b and I/O1d output the C/T signal, and makes I/O1a and I/O1c output RxC16x.

Figure 2. I/OPCR Control of I/O3:0 Pins for Each Channel.

Registers of the Interrupt System

The CIR, and "Global" registers are updated with the IACKN signal or from the "Update CIR" command at hex address 2A. These registers are not updated when IRQN is asserted since there could be a long time between the assertion of IRQN and the start of the interrupt service routine. (See notes following this section).

Current Interrupt Register (CIR)

# Bytes	Type	Chan #
3	3	2

The Channel # field indicates which of the four UARTs has the highest priority interrupt currently outstanding, while the Type field indicates its source within the UART. The Type field is encoded as follows:

000 No Interrupt
001 Change of State
x10 Transmit available
011 Receive available, no error
100 Receiver break change
101 Counter/Timer
111 Receive available, w/errors

With Type = x11, the # Bytes field indicates the count of received bytes available for reading, while with Type = x10 it indicates the number of bytes that can be written to the transmit FIFO.

The CIR is Read only at address 28H.

Global Interrupt Byte Count (GIBC)

00000	# Bytes
5	3

The GIBC is not an actual register but simply outputs the interrupting UART's transmit or receive byte counter value. The count, accurate at the time IACKN asserts, is captured in the CIR. The high order 5 bits are read as '0'. The GIBC is read only at address 2AH.

Global RxFIFO (GRxFIFO)

Received Data
8

Like the GIBC, no physical register implementation exists. The correct receiver's FIFO is popped based on the value of the interrupting channel field of the Current Interrupt Register.

If a receiver is not the cause of the current interrupt, a read of the Global RxFIFO will yield a byte containing all ones and NONE of the UART channels' receive FIFOs will be popped. (IMPORTANT)

The GRxFIFO is Read only at address 2BH.

Global TxFIFO (GTxFIFO)

Data to be Sent
8

Similar to the GRxFIFO, no physical register implementation exists. The byte is pushed into the correct transmitter's FIFO based on the interrupting channel field of the Current Interrupt Register.

If a transmitter is not the cause of the current interrupt, a write to the Global TxFIFO has no effect.

The GTxFIFO is Write only at address 2BH.

Global Interrupting Channel (GICR)

000000	Chan #
6	2

Like the other Global pseudo-registers no hardware register exists. The Channel number field of the Current Interrupt Register padded with leading zeros is output as the GICR. The GICR is Read only at address 29H.

Interrupt Control (ICR)

Threshold	IVC
6	2

The Threshold Field is used by the interrupt comparator to determine if a winning interrupt "bid" should result in interrupting the host MPU. The threshold field resets to 3Fh. The IVC field controls what kind of vector the QUART returns to the host MPU during an Interrupt Acknowledge cycle:

00 Output contents of Interrupt Vector Register
01 Output 6 MSBs of IVR and Channel number as 2 LSBs
10 Output 3 MSBs of IVR, Interrupt Type and Channel number
11 Disable generation of vector during IACK cycle

The IVC field reset to 00. The ICR is read/write at address 2CH.

Bidding Control Registers (BCRs)

Rcv'd Break	State Change	C/T
3	3	2

The 3 MSBs determine the priority of Received Break Interrupts; they are reset to 001.

Bits 4:2 determine the priority of Change of Input State interrupts, and are reset to 00. There is one BCR per UART channel; they can be read or written at addresses 20-23H.

Interrupt Vector (IVR)

Always Used	with IVC = 0x	w/IVC > 00
3	3	2

Holds the constant bits of the interrupt acknowledge vector. As shown, the three MSBs are always used, while the less significant bits can be replaced by the interrupt type code and/or Channel code bits. The IVR is write only at address 29H.

ABSOLUTE MAXIMUM RATINGS[2]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[3]	Note 5	°C
T_{STG}	Storage temperature range	–65 to +150	°C
V_{CC}	Voltage from V_{DD} to GND[4]	–0.5 to +7.0	V
V_S	Voltage from any pin to ground[4]	–0.5 to V_{CC} +0.5	V
P_D	Power dissipation	1	W

DC ELECTRICAL CHARACTERISTICS[5, 6, 7]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL} V_{IH} V_{IH}	Input low voltage Input high voltage (except X1/CLK) Input high voltage (X1/CLK)		 2.0 $0.8V_{CC}$		0.8	V V V
V_{OL} V_{OH}	Output Low voltage Output High voltage (except OD outputs)	I_{OL} = 4.0mA I_{OH} = –400µA I_{OH} = –100µA	 $0.8V_{CC}$ $0.9V_{CC}$		0.4	V V V
I_{IL} I_{IH}	Input current Low, I/O ports Input current High, I/O ports	V_{IN} = 0 V_{IN} = V_{CC}	–10		 1	µA µA
I_I	Input leakage current	V_{IN} = 0 to V_{CC}	–1		1	µA
I_{ILX1} I_{IHX1}	X1/CLK input Low current X1/CLK input High current	V_{IN} = GND, X2 = open V_{IN} = V_{CC}, X2 = open	–100		 100	µA µA
I_{OZH} I_{OZL}	Output off current High, 3–state data bus Output off current Low, 3–state data bus	V_{IN} = V_{CC} V_{IN} = 0	 –1		10 1	 µA
I_{ODL} I_{ODH}	Open–drain output Low current in off state: IRQN Open–drain output Low current in off state: IRQN	V_{IN} = 0 V_{IN} = V_{CC}	–1		 1	 µA
I_{CC}	Power supply current Operating mode	TTL input levels 25°C with X1 = 4MHz			50	mA
	Power down mode*				5	mA

* See UART application note for power down currents less than 5µA.

AC ELECTRICAL CHARACTERISTICS[5, 6, 7, 8]

SYMBOL	FIGURE	PARAMETER	LIMITS Min	Typ	Max	UNIT
Reset timing						
t_{RES}	8	Reset pulse width	200			ns
I/O Port timing[9]						
t_{PS}	9	I/O input setup time before RDN Low	0			ns
t_{PH}	9	I/O input hold time after RDN High	0			ns
t_{PD}	9	I/O output valid from WRN High RDN Low			 110 110	 ns ns
Interrupt timing						
t_{IR}	10	INTRN negated or I/O output High from: (With respect to a 3.6864MHz clock on pin X1/CLK) Read RHR (RxRDY/FFULL interrupt) Write THR (TxRDY interrupt) Reset command (break change interrupt) Reset command (I/O change interrupt) Stop C/T command (counter interrupt) Write IMR (clear of interrupt mask bit)			 100 100 100 100 100 100	 ns ns ns ns ns ns
Clock timing						
t_{CLK}	11	X1/CLK low/high time	125/100			ns
t_{CLK}	11	X1/CLK low/high time (above 4MHz; X1/CLK + 2 active)	56/56			ns
t_{CLK}	11	X1/CLK frequency	0[11]	3.6864	8.0	MHz
t_{CTC}	11	Counter/timer clock high or low time	60			ns
f_{CTC}	11	Counter/timer clock frequency	0[11]		8	MHz
t_{RX}	11	RxC high or low time	30			ns
f_{RX}	11	RxC frequency (16X) RxC frequency (1X)	0[11] 0[11]		16 1.0	MHz MHz
t_{TX}	11	TxC high or low time	30			ns
f_{TX}	11	TxC frequency (16X) TxC frequency (1X)	0[11] 0[11]		16 1.0	MHz MHz
Transmitter timing						
t_{TXD}	12	TxD output delay from TxC low			120	ns
t_{TCS}	12	TxC output delay from TxD output data	–20		+20	ns
Receiver timing						
t_{RXS}	13	RxD data setup time to RxC high	100			ns
t_{RXH}	13	RxD data hold time from RxC high	100			ns

NOTES:

1. Stress above these listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other condition above those indicated in the operation section of the specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range. See ordering information table for applicable temperature range and operating supply range.
5. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of V_{IL} and V_{IH}, as appropriate.
6. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
7. Test condition for interrupt and I/O outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}. Test conditions for rest of outputs: C_L = 150pF.
8. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
9. If CEN is used as the 'strobing' input, the parameter defines the minimum high times between one CEN and the next. The RDN signal must be negated for t_{RWD} guarantee that any status register changes are valid.
10. Consecutive write operations to the command register require at least three rising edges of the X1 clock between writes; four X1/clock edges if the 'X1/clk divide by 2' mode is used.
11. This value is not tested, but is guaranteed by design. For t_{CLK} minimum test rate is 2.0MHz.

AC ELECTRICAL CHARACTERISTICS[4]

T_A = 25°C; V_{CC} = 5V ± 10%, unless otherwise specified. Limits shown as nn/nn refer to Commercial/Industrial temperature range. Single numbers apply to both ranges.

NO.	FIGURE	CHARACTERISTIC	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
1	3	Setup: A[5:0] valid to CEN Low	10			ns
2	3	Hold: A[5:0] valid after CEN Low	30			ns
3	3	Access: Later of CEN Low and RDN Low, to Dnn valid (read)			110/115	ns
4	3	Later of CEN Low and (RDN or WRN as applicable) Low, to DACKN Low Normal Operation: From Power Down:	10 + 2 X1 edges		90/122 + 3 X1 edges 150	ns
5	3	Earlier of CEN High or RDN High, to Dnn released (read)[1]	0		30	ns
6	3	Earlier of CEN High or (RDN or WRN as applicable) High, to DACKN released	0		30	ns
7	3	Earlier of CEN High or (RDN or WRN as applicable) High, in one cycle, to later of CEN Low and (RDN or WRN as applicable) Low, for the next cycle	50			ns
8	3	Setup, Dnn valid (write) to later of CEN Low and WRN Low[2]	–30			ns
9	3	Later of CEN Low and WRN Low, to earlier of CEN High or WRN High	110/115			ns
10	3	Hold: Dnn valid (write) after DACKN Low, CEN High or WRN High[3]	0			ns

NOTES:
1. The minimum time indicates that read data will remain valid until the bus master drives CEN and/or RDN to High.
2. The fact that this parameter is negative means that the Dnn line may actually become valid after CEN and WRN are both Low.
3. In a Write operation, the bus master must hold the write data valid either until drives CEN and/or WRN to High, or until the QUART drives DACKN to Low, whichever comes first.
4. Test condition for interrupt and I/O outputs: C_L = 50pF, forced current for V_{OL} = 5.3mA; forced current for V_{OH} = 400µA, RL = 2.7kΩ to V_{CC}. Test condition for rest of outputs: C_L = 150pF

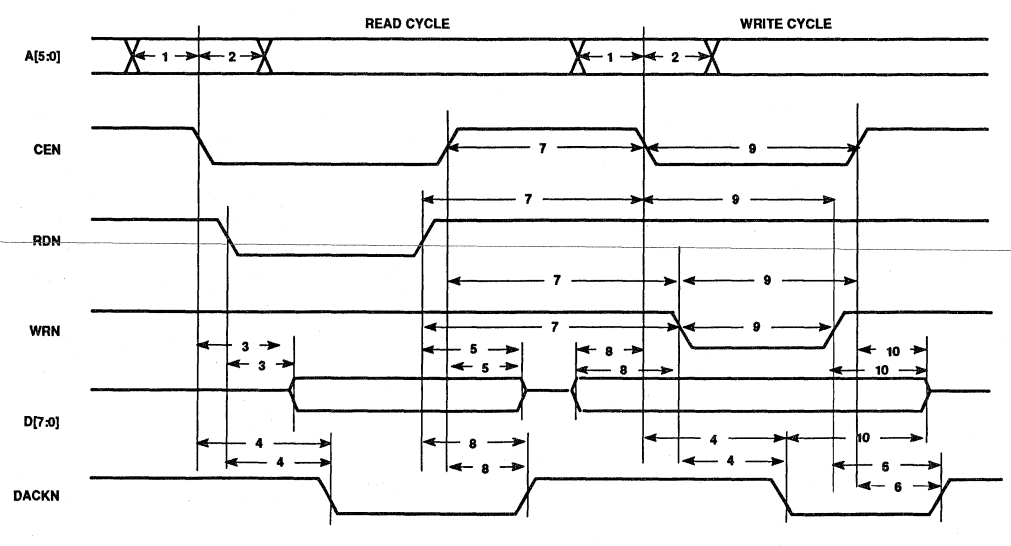


Figure 3. A Read Cycle Followed by a Write Cycle with DACKN

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = 5V \pm 10\%$, unless otherwise specified. Limits shown as nn/nn refer to Commercial/Industrial temperature range. Single numbers apply to both ranges.

NO.	FIGURE	CHARACTERISTIC	LIMITS			UNIT
			Min	Typ	Max	
1	4	D[7:0] Valid after IACKN Low			110/115	ns
2	4	DACKN Low after IACKN Low	10 + 2 X1 edges		90/122 + 3 X1 edges	ns
3	4	D[7:0] floating after IACKN High	0		30	ns
4	4	DACKN High after IACKN High	0		30	ns
5	4	IACKN High after IACKN Low	110/115			ns

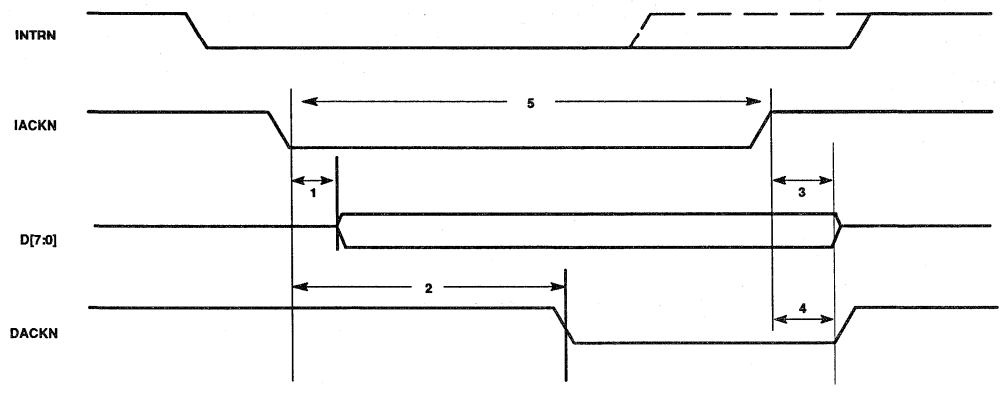


Figure 4. Interrupt Knowledge (IACKN) Timing

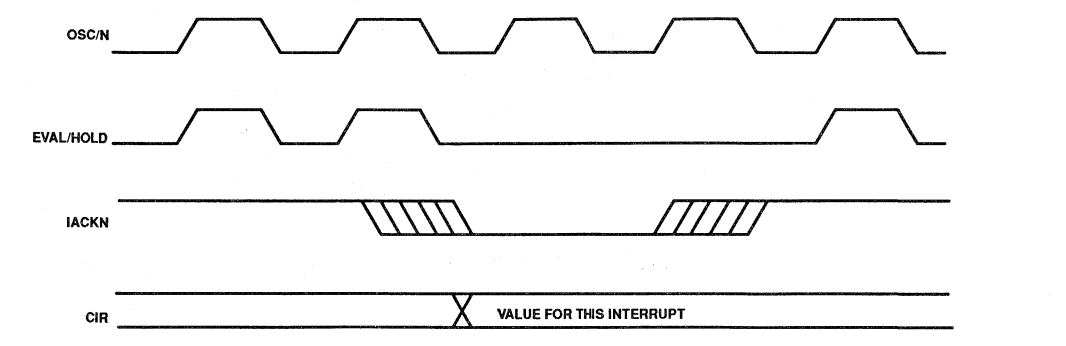


Figure 5. Interrupt Bid Arbitration Timing.

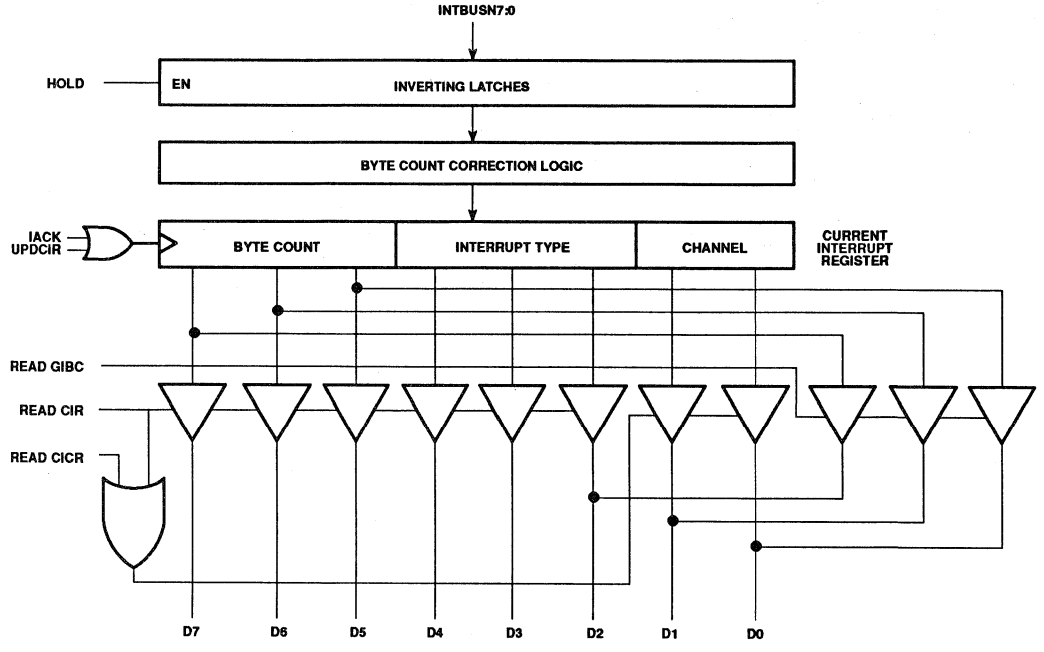


Figure 6. Current Interrupt Register Logic

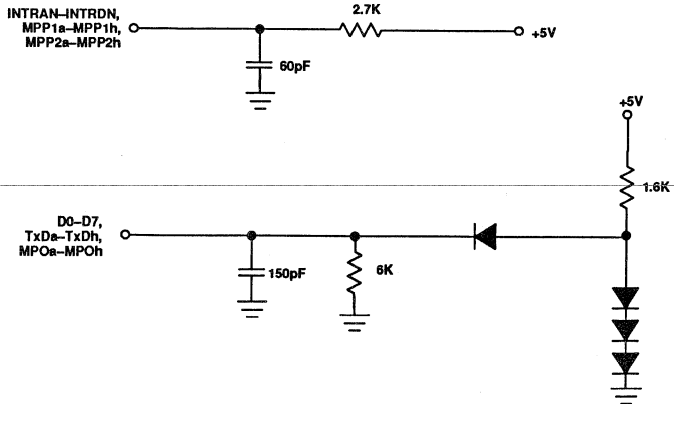


Figure 7. Test Conditions on Outputs

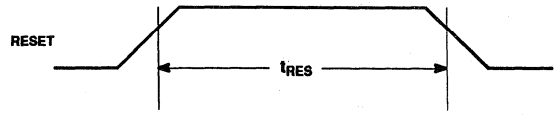


Figure 8. Reset Timing

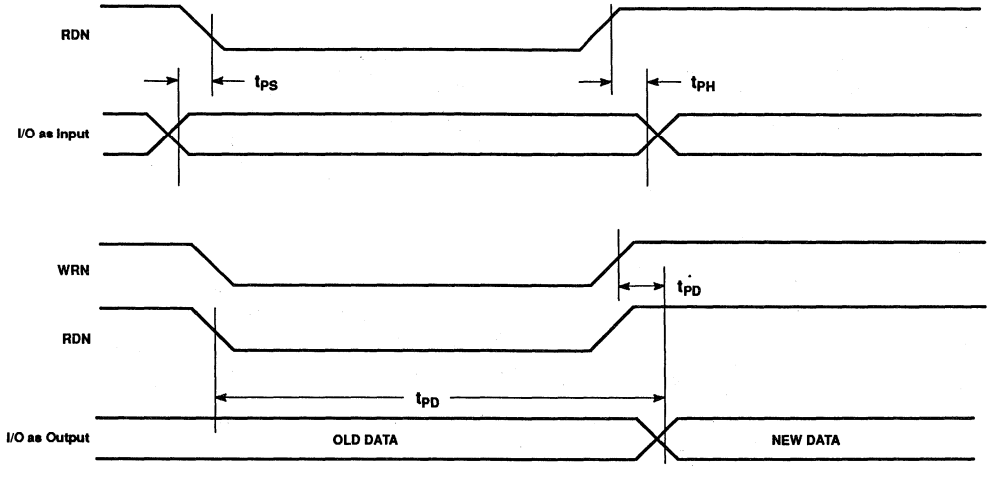
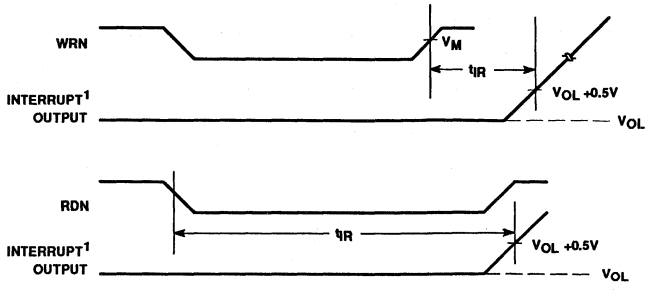
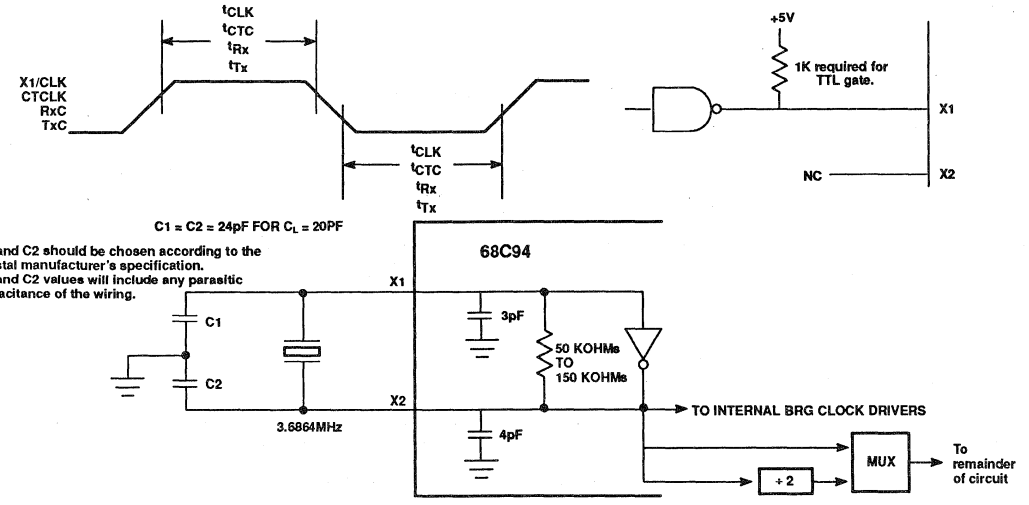


Figure 9. I/O Port Timing



NOTES:
1. INCLUDES I/O WHEN USED AS TxRDY or RxDY/FFULL OUTPUTS AS WELL AS INTRN.
2. THE TEST FOR OPEN DRAIN OUTPUTS IS INTENDED TO GUARANTEE SWITCHING OF THE OUTPUT TRANSISTOR. MEASUREMENT OF THIS RESPONSE IS REFERENCED FROM THE MIDPOINT OF THE SWITCHING SIGNAL, V_M, TO A POINT 0.5V ABOVE V_{OL}. THIS POINT REPRESENTS NOISE MARGIN THAT ASSURES TRUE SWITCHING HAS OCCURRED. BEYOND THIS LEVEL, THE EFFECTS OF EXTERNAL CIRCUITRY AND TEST ENVIRONMENT ARE PRONOUNCED AND CAN GREATLY AFFECT THE RESULTANT MEASUREMENT.

Figure 10. Interrupt Timing



NOTES:
C1 and C2 should be based on manufacturer's specification.
X1 and X2 parasitic capacitance IS 1-2pF AND 3-5pF, respectively.
GAIN: at 4MHz 8 to 14db; at 8MHz 2 to 6db
PHASE: at 4MHz 272° to 276°; at 8MHz 272° to 276°

TYPICAL CRYSTAL SPECIFICATION

FREQUENCY:	2 – 4MHZ
LOAD CAPACITANCE (C_L):	12 – 32pF
TYPE OF OPERATION:	PARALLEL RESONANT, FUNDAMENTAL MODE

Figure 11. Clock Timing

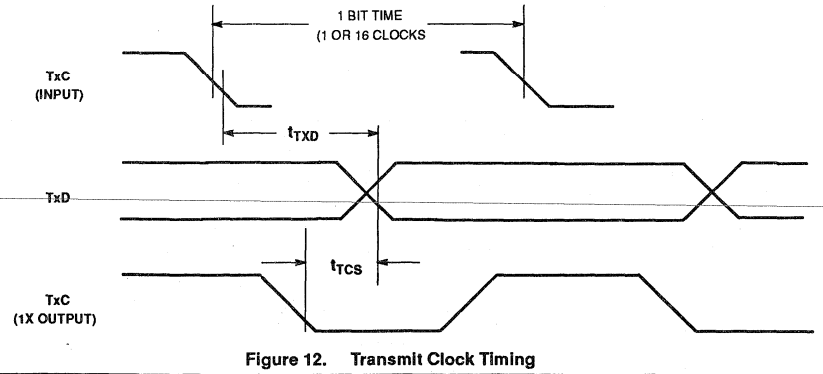


Figure 12. Transmit Clock Timing

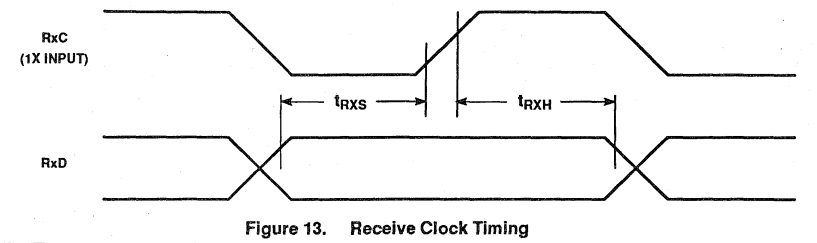
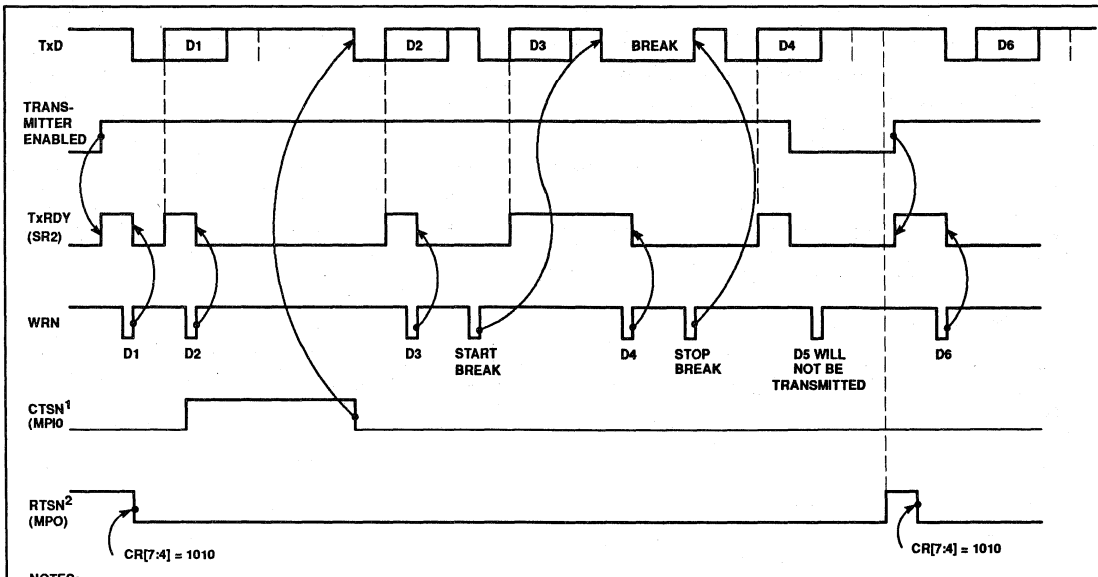
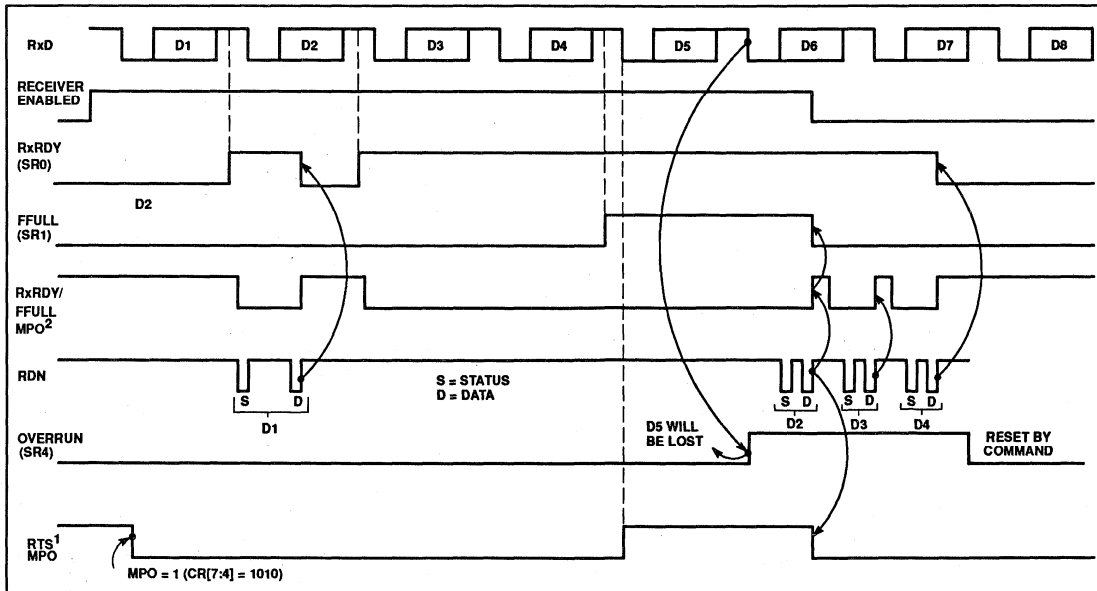


Figure 13. Receive Clock Timing



NOTES:
1. TIMING SHOWN FOR MR2[4] = 1.
2. TIMING SHOWN FOR MR2[5] = 1.

Figure 14. Transmitter Data Timing



NOTES;
1. TIMING SHOWN FOR MR1[7] = 1.
2. SHOWN FOR OPCR [6:4, 2:0] = 111 AND MR1[6] = 0.

Figure 15. Receiver Data Timing

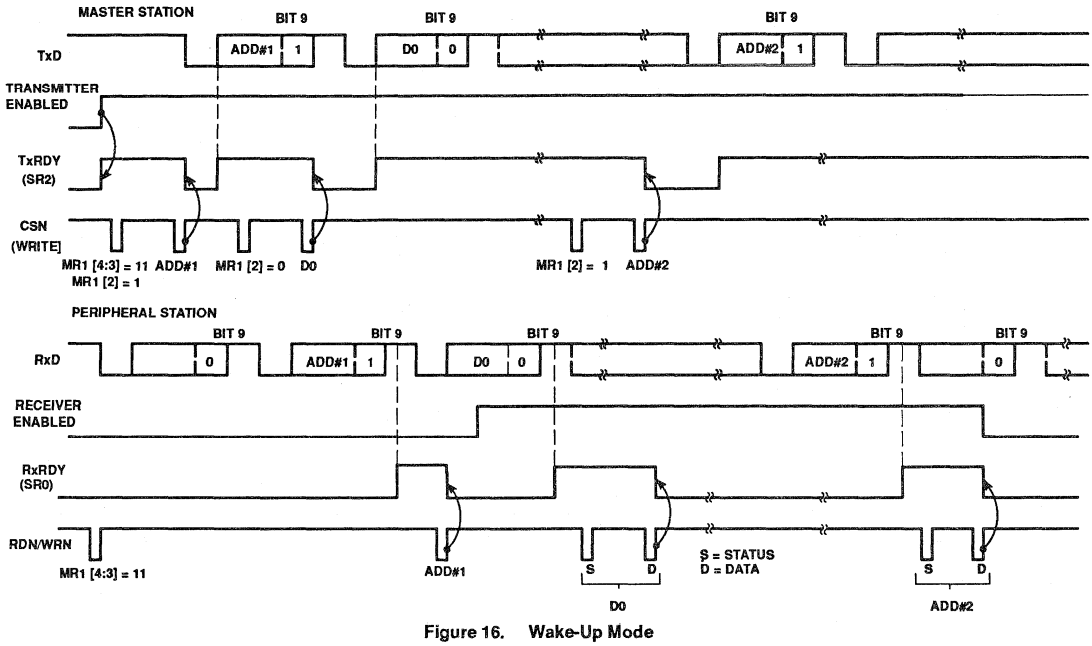


Figure 16. Wake-Up Mode

INTERRUPT NOTES

The following is a brief description of the new QUART "Bidding" interrupt system, interrupt vector and the use of the Global registers.

The new features of the QUARTs have been developed to greatly reduce the microprocessor time required to service uart interrupts. Bus cycle times have also been enhanced. By use of the new Current Interrupt Register (CIR) the speed of a poled system is also improved. For example programming the SCC2692 to interrupt on TxRDY and RxFUL would generate four interrupts for every six characters processed along with at least two additional accesses to the chip for each interrupt. This amounts to two non–data chip accesses per character. In the 68C94 this has been reduced to 0.25 non data accesses per character; an eight fold improvement. In certain conditions use of the global registers will yield a greater improvement.

The QUART has 18 possible sources which can be programmed to generate an interrupt:

- 4 Receiver channels
- 4 Transmitter Channels
- 4 Received "Brake" conditions
- 4 Change of State Detectors (a total of 8 ports)
- 2 Counter/Timers

These sources are encoded in such a way that they generate a unique value. This value is defined by chip hardwire programming, user programming, and the source's present condition. The values the sources generate are compared (at the X1 clock rate) to a user defined Interrupt Threshold value contained in the ICR (Interrupt Control Register). When the source's value exceeds the threshold the interrupt is generated. It is the source's value which is captured in the CIR.

The heart of the interrupt speed enhancement is attained by allowing the interrupting source to encode its channel, interrupt type and, if appropriate, the number of FIFO bytes requiring service. This information is coded and transferred the CIR (Current Interrupt Register) at the time IACKN is asserted or the command 'Update CIR' is executed. Upon an interrupt the processor may read this register and in one access determine the "who, what and how much". This CIR value is used to drive the interrupt vector modification (when used) and the new "Global" registers.

"Global" Registers

The "Global Registers" are effectively pointers which use the contents of the CIR to direct a read or write operation to Rx or Tx or other source which is currently interrupting. There are four global registers defined in the register map:

1. Global Interrupting Byte Count
2. Global Interrupting Channel
3. Global Receive FIFO Register
4. Global Transmit FIFO Register

The global receive and transmit registers operate as an indirect address. The data read from the global receive register will be that of the currently interrupting receiver; the data written to the global transmit register will go to the currently interrupting transmitter. The interesting point here is that under certain circumstances an interrupt can be serviced without an interrogation of the chip.

For completeness it should be noted that the global registers are not physical devices. Reads of the Global Byte and Channel registers give the Byte count or Channel number, respectively, (right justified) of the interrupting channel. The CIR data is mapped to these "registers".

Table 6. "Bidding Format"

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION
Rx Byte count			Error 1	1	1	Channel No.		Receiver bid With error
Rx Byte count			no Error 0	1	1	Channel No.		Receiver bid No error
0	Tx Byte Count			1	0	Channel No.		Transmit bid
Programmable			1	0	0	Channel No.		Receive Brake
Programmable			0	0	1	Channel No.		Change of State
Programmable		0	1	0	1	Channel No.		Counter/Timer

NOTES:

1. The ones and zeros above represent the hardwired positions.
2. Note the format of bits 4:2. They represent the identity of the interrupting source.
3. Bids with the highest number of contiguous MSBs win the bid.

1 1 1	Receiver with error
0 1 1	Receiver without error
x 1 0	Transmitter
1 0 0	Receiver brake detect
0 0 1	Change of State
1 0 1	Counter/Timer
0 0 0	No interrupt

In these identifiers the receivers are biased to have highest priority. The identifier bits and the channel number bits are hardwired on the chip. Normally the non–data interrupts would be programmed to a low value. The programmable fields can, in some cases, make these sources higher than a full receiver.

It would seem that a 11 programmed in the upper counter/timer bits, for example, would cause it to interrupt nearly all the time. This is not true . A counter/timer that has not timed out will not bid. In a similar fashion a receiver FIFO that is empty or a transmitter FIFO that is full will not bid

In general terms the threshold value programmed in the ICR (Interrupt Control Register) will reflect some fill level of the eight character transmit and receive FIFOs that allow processor service without underrun or overrun occurring.

Note that interrupt threshold value in the ICR is 6 bits long. This value is aligned with the bid arbitration logic such that it bids only through the most significant 6 bits. The result of this is that the channel value does not 'bid'. However the logic is such that other parts of the bid being equal the condition of the highest channel will be captured in CIR. The increasing order of the channels is A, B, C, D. Thus channel D is the "strongest" of the four.

It could be that the giving the highest strength to channel D may, from time to time, not be what would be most desired. Further it may

be desired to alter the authority of a channel's bid. This may be done by setting the Rx and/or Tx interrupt bits in MR0 and MR1 to values different than zero. This will have the effect of not allowing the associated receiver or transmitter to bid until its FIFO reaches a particular fill level. Although this compromises the idea of the bidding interrupt scheme, it is entirely safe to use. In fact it is setting of MR0 and MR1 interrupt bits to zero that causes the receiver to stop bidding when it is empty and causes the transmitter to stop bidding when it is full. Altering the MR0 and MR1 interrupt bits only changes the level at which the Rx & Tx bidding is stopped.

See the "Interrupt Note on 68C94" on page 12 which refers to the use of the MR registers in controlling the Rx and Tx bidding.

Table 7. Configuration of Interrupt Vector for the QUART

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Interrupt vector for → ICR(1:0) = 00	INTERRUPT VECTOR FORMATS (Controlled by ICR[1:0])							
	IVR[7:0]							
	Full interrupt vector							
Interrupt vector for → ICR(1:0) = 01								
	IVR[7:2]						ICR[1:0]	
	Interrupt vector 6 MSBs						Channel number	
Interrupt vector for → ICR(1:0) = 10								
	IVR[7:5]			ICR[4:2]			ICR[1:0]	
	Interrupt vector 3 MSBs			Interrupt type			Channel number	
Interrupt vector for → ICR(1:0) = 11 (Inhibit)								
	Inhibit vector output. (Set bus to FFh)							
	CURRENT INTERRUPT REGISTER FORMAT CIR[7:0]							
	Rx or Tx byte count			Interrupt type: R/Tx CT COS BRK			Channel number	
	INTERRUPT CONTROL REGISTER FORMAT ICR[0:7]							
	Interrupt threshold ICR[7:2]						Interrupt vector format ICR[1:0]	

In normal operation the character of an interrupt will be controlled by the above registers in conjunction with the IMR (Interrupt Mask Register (one for each DUART)) . The function of the IMR will be to enable bidding of any particular source.

Recall that the QUART has 18 functions which may generate an interrupt.

The format of the interrupt vector is controlled by the ICR[1:0] bits. The formats are shown in Table 7. The purpose of the vector modification is to allow the interrupting source (either channel or type and channel) to direct the processor to appropriate service routine. We have found that some users wish to use extremely tight loops for the service routines and find the addition of several tests of status bytes to be very 'expensive' in processor time.

NOTE ON QUART INTERFACE TO ITS CONTROLLING PROCESSOR

The QUART, has been designed to interface in either the synchronous interrupt environment (without DACKN) or the asynchronous interrupt environment (with DACKN). The 80xxx devices of Intel design are usually operated in a synchronous interrupt mode while those of Motorola design, 68xxx devices, operate in an asynchronous interrupt mode.

Note: Synchronous and asynchronous interrupt modes are not in any way associated with synchronous or asynchronous data transmission.

The QUART has been designed with the pins required to service either interface. In general then it is probable that in any application some of the interface pins will not be used. This note discusses what is required for the "text book" connections of the two methods. It should be noted that features of either method are not mutually exclusive.

The interface pins are all active low. (at V_{SS} or ground) The pins used for normal reading and writing to the QUART (the generation of a bus cycle) are CEN (Chip Enable), RDN (Read Enable), WRN (Write Enable). The pins used in the interrupt service are IRQN (Interrupt Request), IACKN (Interrupt Acknowledge). The pin used for data transfer is DACKN (Data Acknowledge). IRQN and DACKN are open drain outputs.

DACKN signaling can be enabled or disabled via writing to address 27h or 26h respectively. Note that if DACKN is enabled that writing to the QUART will occur on the falling edge of DACKN. The use of hardware reset (required at power up) enables DACKN.

The Asynchronous Interface

Those familiar with 68xxx I/O will note the use of the two pins RDN and WRN to be in conflict with 68xxx devices use of the one R/WN pin. The R/WN must be inverted such that the R/WN may drive the WRN input while the inversion of R/WN drives the RDN input. It is good practice to condition the inversion of R/WN such that RDN will not become active on the termination of a write to the QUART while CEN is still asserted. These short periods of read could upset FIFO pointers in the chip.

During a read of the QUART DACKN signals that valid data is on the data bus. During a write to the QUART DACKN signals that data placed on the bus by the control processor has been written to the addressed register. The generation of DACKN begins with the start of a bus cycle (Read, Write or Interrupt Acknowledge) and then requires two edges of the X1 clock plus 70ns for its assertion.

In this mode the writing of data to the QUART registers occurs on the falling edge of DACKN or the rising edge of the combination of CEN and WRN which ever occurs first. This requires that the data to be written to the QUART registers be valid with respect to the leading edge of the combination of CEN and WRN. (In the synchronous mode it is the trailing edge)

IACKN updates the CIR (Current Interrupt Register) and places the Interrupt Vector or Modified Interrupt Vector on the bus if the Interrupt Vector is used.

The Synchronous Interface

In this mode the DACKN and IACKN are usually not used. Here data is written to the QUART on the trailing edge of the combination of CEN and WRN. The placing of data on the bus during a read cycle begins with the leading edge of the combination of CEN and RDN.

The read cycle will terminate with the rise of CEN or RDN which ever one occurs first. In this mode bus cycles are usually setup to be the minimum time required by the QUART and hence will be faster than bus cycles that are defined by the DACKN signal. DACKN should be turned off in this mode.

When IACKN is not used or is not available the command at 2Ah should be used to update the CIR (Current Interrupt Register). This register is normally updated by IACKN in response to the IRQN. Note that the CIR is not updated by IRQN since there could be a long time between the assertion of IRQN and the start of the interrupt service routine. During this time it is quite possible that another interrupt with a higher priority occurs. It is the CIR that contains the information that describes the interrupt source and its priority. It is therefor recommended that the first operation upon entering the interrupt service routine is the updating of the CIR. (Recall that the contents of the GLOBAL registers reflect the content of the CIR)

Summary

In the asynchronous mode all of the interface pins are usually used. The synchronous mode usually will not use the IACKN and DACKN. However there is no conflict in the quart if both modes are used in the same application. (i.e. More than one device may control the QUART) The principles to keep in mind are:

1. When IACKN is not used the CIR should be updated via command.
2. If DACKN is not used it should be disabled.
3. When in the asynchronous mode be sure DACKN is enabled.
4. With 68xxx type controllers the RDN signal must be generated.

Enhanced octal universal asynchronous receiver/transmitter (Octal UART)

SCC2698B

DESCRIPTION

The SCC2698B Enhanced Octal Universal Asynchronous Receiver/Transmitter (Octal UART) is a single chip MOS-LSI communications device that provides eight full-duplex asynchronous receiver/transmitter channels in a single package. It is fabricated with CMOS technology which combines the benefits of high density and low power consumption.

The operating speed of each receiver and transmitter can be selected independently as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the Octal UART particularly attractive for dual-speed channel applications such as clustered terminal systems.

The receiver is quadruple buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a handshaking capability is provided to disable a remote UART transmitter when the receiver buffer is full.

The UART provides a power-down mode in which the oscillator is frozen but the register contents are stored. This results in reduced power consumption on the order of several magnitudes. The Octal UART is fully TTL compatible and operates from a single +5V power supply.

The SCC2698B is an upwardly compatible version of the 2698A Octal UART. In PLCC packaging, it is enhanced by the addition of receiver ready or FIFO full status outputs, and transmitter empty status outputs for each channel on 16 multipurpose I/O pins. The multipurpose I/O pins of the SCC2698B were inputs only on the SCC2698A.

FEATURES

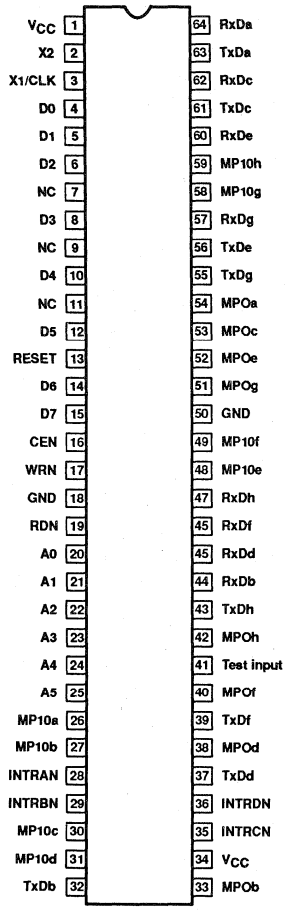
- Eight full-duplex asynchronous receiver/transmitters
- Quadruple buffered receiver data register
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Baud rate for the receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4K baud
    Non-standard rates to 115.2K baud
  - User-defined rates from the programmable counter/timer associated with each of four blocks
  - External 1x or 16x clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex), automatic echo, local loop back, remote loopback
- Four multi-function programmable 16-bit counter/timers
- Four interrupt outputs with eight maskable interrupting conditions for each output
- Receiver ready/FIFO full and transmitter ready status available on 16 multi-function pins in PLCC package
- On-chip crystal oscillator
- TTL compatible
- Single +5V power supply with low power mode

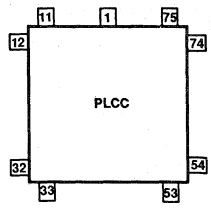
ORDERING INFORMATION

PACKAGES	V_{CC} = +5V ±5%, T_A = 0°C to +70°C	V_{CC} = +5V ±5%, T_A = –40°C to +85°C
Plastic DIP	SCC2698BC1N64	SCC2698BE1N64
Plastic Leaded Chip Carrier	SCC2698BC1A84	SCC2698BE1A84

NOTE:
Pin Grid Array (PGA) package version is available from Philips Components Military Division.

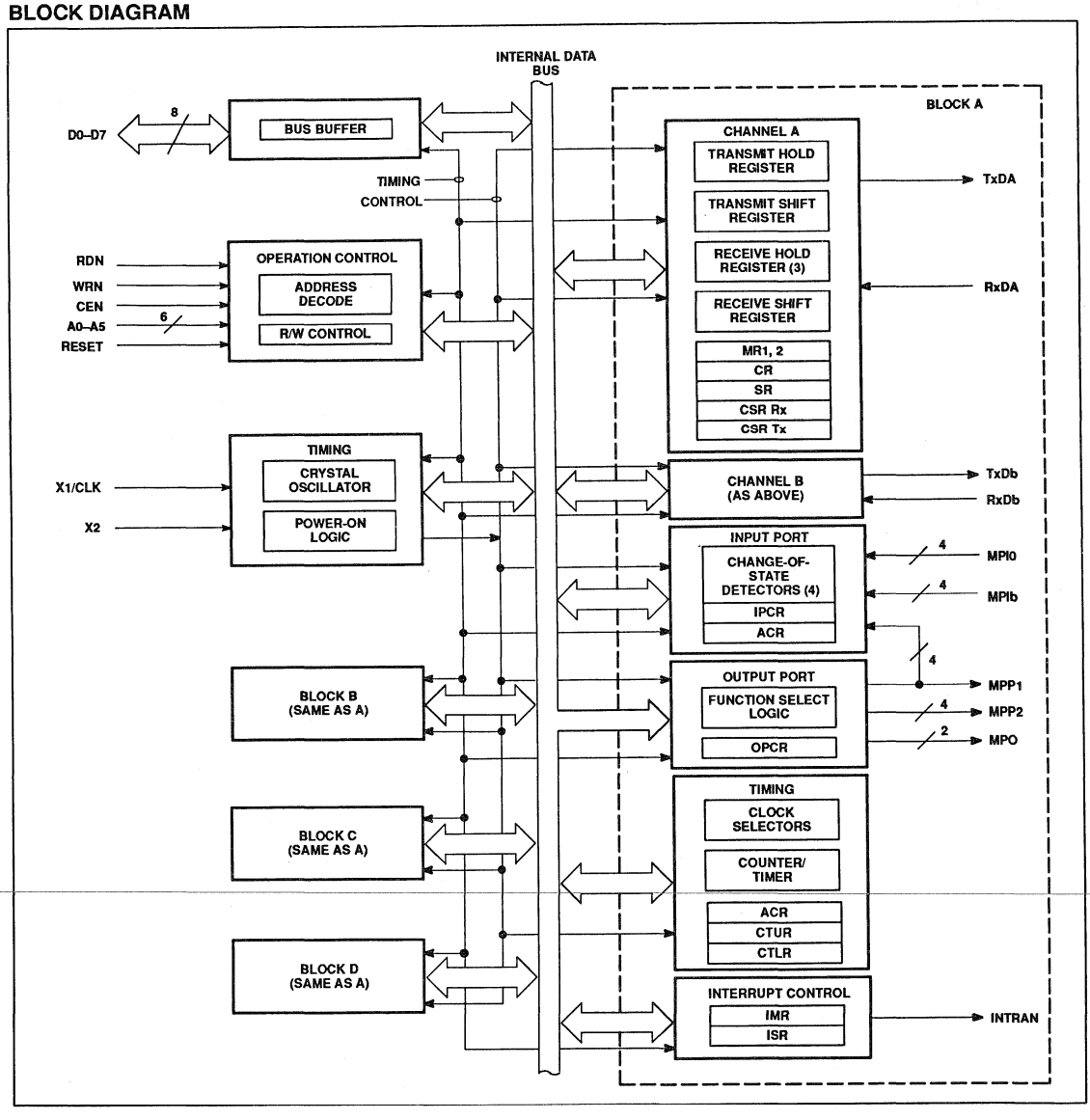
PIN CONFIGURATIONS





Pin	Function	Pin	Function	Pin	Function
1	TxDa	29	A3	57	RxDd
2	MPP2g	30	MPP2b	58	RxDf
3	RxDa	31	A4	59	RxDh
4	MPP2h	32	A5	60	MPI1e
5	V_{cc}	33	MPI0a	61	MPI0e
6	X2	34	MPI0b	62	MPI1f
7	X1/CLK	35	INTRAN	63	MPI0f
8	D0	36	INTRBN	64	MPP1e
9	D1	37	MPI0c	65	GND
10	D2	38	MPI1c	66	MPP1f
11	D3	39	MPI0d	67	MPOg
12	D4	40	MPI1d	68	MPP2e
13	D5	41	TxDb	69	MPOe
14	MPI1a	42	MPP1c	70	MPP2f
15	RESET	43	MPOb	71	MPOc
16	D6	44	MPP1d	72	MPOa
17	D7	45	V_{cc}	73	TxDg
18	CEN	46	INTRCN	74	TxDe
19	WRN	47	INTRDN	75	RxDg
20	GND	48	MPP2c	76	MPI0g
21	MPI1b	49	TxDd	77	MPI0h
22	RDN	50	MPP2d	78	MPI1g
23	A0	51	MPOd	79	RxDe
24	MPP1a	52	TxDf	80	MPIh
25	A1	53	MPOf	81	TxDc
26	MPP1b	54	MPOh	82	MPP1g
27	A2	55	TxDh	83	RxDc
28	MPP2a	56	RxDb	84	MPP1h

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
D0–D7	4–6, 8, 10, 12, 14, 15	8–13, 16, 17	I/O	**Data Bus:** Active–High 8-bit bidirectional 3-State data bus. Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the Octal UART take place over this bus. The direction of the transfer is controlled by the WRN and RDN inputs when the CEN input is low. When the CEN input is High, the data bus is in the 3-State condition.
CEN	16	18	I	**Chip Enable:** Active-Low input. When Low, data transfers between the CPU and the Octal UART are enabled on D0–D7 as controlled by the WRN, RDN and A0–A5 inputs. When CEN is High, the Octal UART is effectively isolated from the data bus and D0–D7 are placed in the 3-State condition.
WRN	17	19	I	**Write Strobe:** Active-Low input. A Low on this pin while CEN is Low causes the contents of the data bus to be transferred to the register selected by A0–A5. The transfer occurs on the trailing (rising) edge of the signal.
RDN	19	22	I	**Read Strobe:** Active-Low input. A Low on this pin while CEN is Low causes the contents of the register selected by A0–A5 to be placed on the data bus. The read cycle begins on the leading (falling) edge of RDN.
A0–A5	20–25	23, 25, 27, 29, 31, 32	I	**Address Inputs:** Active-High address inputs to select the Octal UART registers for read/write operations.
RESET	13	15	I	**Reset:** Master reset. A High on this pin clears the status register (SR), clears the interrupt mask register (IMR), clears the interrupt status register (ISR), clears the output port configuration register (OPCR), places the receiver and transmitter in the inactive state causing the TxD output to go to the marking (High) state, and stops the counter/timer. Clears power-down mode and interrupts. Clears Test Modes.
INTRAN–INTRDN	28, 29, 35, 36	35, 36, 46, 47	O	**Interrupt Request:** This active-Low open drain output is asserted on occurrence of one or more of eight maskable interrupting conditions. The CPU can read the interrupt status register to determine the interrupting condition(s).
X1/CLK	3	7	I	**Crystal 1:** Crystal or external clock input. When using the crystal oscillator, this pin serves as the connection for one side of the crystal. If a crystal is not used, an external clock is supplied at this input. An external clock (or crystal) is required even if the internal baud rate generator is not utilized. This clock is used to drive the internal baud rate generator, as an optional input to the timer/counter, and to provide other clocking signals required by the chip.
X2	2	6	I	**Crystal 2:** Connection for other side of crystal. If an external source is used instead of a crystal, this connection should be left open (see Figure 7).
RxDa–RxDh	64, 44, 62, 45, 60, 46, 57, 47	3, 56, 83, 57, 79, 58, 75, 59	I	**Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified, this input is sampled on the rising edge of the clock. If internal clock is used, the RxD input is sampled on the rising edge of the RxC1x signal as seen on the MPO pin.
TxDa–TxDh	63, 32, 61, 37, 56, 39, 55, 43	1, 41, 81, 49, 74, 52, 73, 55	O	**Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the marking (High) condition when the transmitter is idle or disabled and when the Octal UART is operating in local loopback mode. If external transmitter is specified, the data is shifted on the falling edge of the transmitter clock. If internal clock is used, the TxD output changes on the falling edge of the TxC1x signal as seen on the MPO pin.
MPOa–MPOh	54, 33, 53, 38, 52, 40, 51, 42	72, 43, 71, 51, 69, 53, 67, 54	O	**Multi-Purpose Output:** Each of the four DUARTS has two MPO pins. One of the following eight functions can be selected for this output pin by programming the OPCR (output port configuration register). Note that reset conditions MPO pins to RTSN. **RTSN** – Request to send active-Low output. This output is asserted and negated via the command register. By appropriate programming of the mode registers, (MR1[7])=1 RTSN can be programmed to be automatically reset after the character in the transmitter is completely shifted or when the receiver FIFO and shift register are full. RTSN is an internal signal which normally represents the condition of the receiver FIFO not full, i.e., the receiver can request more data to be sent. However, it can also be controlled by the transmitter empty and the commands 8h and 9h written to the CR (command register). **C/TO** – The counter/timer output. **TxC1X** – The 1X clock for the transmitter. **TxC16X** – The 16X clock for the transmitter. **RxC1X** – The 1X clock for the receiver. **RxC16X** – The 16X clock for the receiver. **TxRDY** – Transmitter holding register empty signal. **RxRDY/FFULL** – Receiver FIFO not empty/full signal.
MPI0a–MPI0h	26, 27, 30, 31, 48, 49, 58, 59	33, 34, 37, 39, 61, 63, 76, 77	I	**Multi-Purpose Input 0:** This pin (one in each UART) is programmable. Its state can always be read through the IPCR bit 0, or the IPR bit 0. **CTSN:** By programming MR2[4] to a 1, this input controls the clear-to-send function for the transmitter. It is active low. This pin is provided with a change-of-state detector.

PIN DESCRIPTION (CONTINUED)

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
MPI1a–MPI1h	NC	14, 21, 38, 40, 60, 62, 78, 80	I	**Multi-Purpose Input 1:** This pin (one for each unit) is programmable. Its state can always be determined by reading the IPCR bit 1 or IPR bit 1. **C/TCLK** – This input will serve as the external clock for the counter/timer when ACR[5] is set to 0. This occurs only for channels a, c, e, and g since there is one counter/timer for each DUART block. This pin is provided with a change-of-state detector.
MPP1a–MPP1h	NC	24, 26, 42, 44, 64, 66, 82, 84	I/O	**Multi-Purpose Pin 1:** This pin (one for each UART) is programmed to be an input or an output according to the state of OPCR[7]. (0 = input, 1 = output). The state of the multi-purpose pin can always be determined by reading the IPR. When programmed as an input, it will be the transmitter clock (TxCLK). It will be 1x or 16x according to the clock select registers (CSR[3.0]). When programmed as an output, it will be the status register TxRDY bit. As an output, it will be an open drain, and thus requires a pull-up device.
MPP2a–MPP2h	NC	28, 30, 48, 50, 68, 70, 2, 4	I/O	**Multi-Purpose Pin 2:** This pin (one for each UART) is programmed to be an input or an output according to the state of OPCR[7]. (0 = input, 1 = output). The state of the multi-purpose pin can always be determined by reading the IPR. When programmed as an input, it will be the receiver clock (RxCLK). It will be 1x or 16x according to the clock select registers (CSR[7:4). When programmed as an output, it will be the ISR status register RxRDY/FIFO full bit. As an output, it will be an open drain, and thus requires a pull-up device.
Test Input	41	–	I	**Test Input:** This pin is used as an input for test purposes at the factory while in test mode. This pin can be treated as 'N/C' by the user. It can be tied high, or left open.
V_{CC}	1, 34	5, 45	I	**Power Supply:** +5V supply input.
GND	18, 50	20, 65	I	**Ground**

BLOCK DIAGRAM

As shown in the block diagram, the Octal UART consists of: data bus buffer, interrupt control, operation control, timing, and eight receiver and transmitter channels. The eight channels are divided into four different blocks, each block independent of each other (see Figure 1).

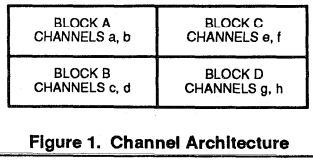


Figure 1. Channel Architecture

Channel Blocks

There are four blocks (Figure 1), each containing two sets of receiver/transmitters. In the following discussion, the description applies to Block A which contains channels a and b. However, the same information applies to all channel blocks.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the Octal UART.

Interrupt Control

A single interrupt output per block (INTRN) is provided which is asserted on occurrence of any of the following internal events:

- –Transmit holding register ready for each channel
- –Receive holding register ready or FIFO full for each channel
- –Change in break received status for each channel
- –Counter reached terminal count
- –Change in MPI input

Associated with the interrupt system are the interrupt mask register (IMR) and the interrupt status register (ISR). The IMR can be programmed to select only certain conditions, of the above, to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. However, the bits of the ISR are not masked by the IMR. The transmitter ready status and the receiver ready or FIFO full status can be provided on MPP1a, MPP1b, MPP2a, and MPP2b by setting OPCR[7]. these outputs are not masked by IMR.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The functions performed by the CPU read and write operations are shown in Table 1.

Mode registers 1 and 2 are accessed via an auxiliary pointer. The pointer is set to MR1 by RESET or by issuing a reset pointer command via the command register. Any read or write of the mode register while the pointer is at MR1 switches the pointer to MR2. The pointer then remains at MR2 so that subsequent accesses are to MR2, unless the pointer is reset to MR1 as already described.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer for each block, and two clock selectors.

The crystal oscillator operates directly from a 3.6864MHz crystal connected across the X1/CLK and X2 inputs with a minimum of external components. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. If an external clock is used instead of a crystal, X1 must be driven and X2 left floating as shown in Figure 7. The clock serves as the basic timing reference for the baud rate generator (BRG), the counter/timer, and other internal circuits. A clock frequency, within the limits specified in the electrical specifications, must be supplied even if the internal BRG is not used.

Table 1. Register Addressing

Units A and B								Units E and F							
A5	A4	A3	A2	A1	A0	READ (RDN=0)	WRITE (WRN=0)	A5	A4	A3	A2	A1	A0	READ (RDN=0)	WRITE (WRN=0)
0	0	0	0	0	0	MR1a, MR2a	MR1a, MR2a	1	0	0	0	0	0	MR1e, MR2e	MR1e, MR2e
0	0	0	0	0	1	SRa	CSRa	1	0	0	0	0	1	SRe	CSRe
0	0	0	0	1	0	BRG Test	CRa	1	0	0	0	1	0	Reserved*	CRe
0	0	0	0	1	1	RHRa	THRa	1	0	0	0	1	1	RHRe	THRe
0	0	0	1	0	0	IPCRA	ACRA	1	0	0	1	0	0	IPCRC	ACRC
0	0	0	1	0	1	ISRA	IMRA	1	0	0	1	0	1	ISRC	IMRC
0	0	0	1	1	0	CTUA	CTURA	1	0	0	1	1	0	CTUC	CTURC
0	0	0	1	1	1	CTLA	CTLRA	1	0	0	1	1	1	CTLC	CTLRC
0	0	1	0	0	0	MR1b, MR2b	MR1b, MR2b	1	0	1	0	0	0	MR1f, MR2f	MR1f, MR2f
0	0	1	0	0	1	SRb	CSRb	1	0	1	0	0	1	SRf	CSRf
0	0	1	0	1	0	1X/16X Test	CRb	1	0	1	0	1	0	Reserved*	CRf
0	0	1	0	1	1	RHRb	THRb	1	0	1	0	1	1	RHRf	THRf
0	0	1	1	0	0	Reserved*	Reserved*	1	0	1	1	0	0	Reserved*	Reserved*
0	0	1	1	0	1	Input port A	OPCRA	1	0	1	1	0	1	Input port C	OPCRC
0	0	1	1	1	0	Start C/T A	Reserved*	1	0	1	1	1	0	Start C/T C	Reserved*
0	0	1	1	1	1	Stop C/T A	Reserved*	1	0	1	1	1	1	Stop C/T C	Reserved*
Units C and D								**Units G and H**							
0	1	0	0	0	0	MR1c, MR2c	MR1c, MR2c	1	1	0	0	0	0	MR1g, MR2g	MR1g, MR2g
0	1	0	0	0	1	SRc	CSRc	1	1	0	0	0	1	SRg	CSRg
0	1	0	0	1	0	Reserved*	CRc	1	1	0	0	1	0	Reserved*	CRg
0	1	0	0	1	1	RHRc	THRc	1	1	0	0	1	1	RHRg	THRg
0	1	0	1	0	0	IPCRB	ACRB	1	1	0	1	0	0	IPCRD	ACRD
0	1	0	1	0	1	ISRB	IMRB	1	1	0	1	0	1	ISRD	IMRD
0	1	0	1	1	0	CTUB	CTURB	1	1	0	1	1	0	CTUD	CTURD
0	1	0	1	1	1	CTLB	CTLRB	1	1	0	1	1	1	CTLD	CTLRD
0	1	1	0	0	0	MR1d, MR2d	MR1d, MR2d	1	1	1	0	0	0	MR1h, MR2h	MR1h, MR2h
0	1	1	0	0	1	SRd	CSRd	1	1	1	0	0	1	SRh	CSRh
0	1	1	0	1	0	Reserved*	CRd	1	1	1	0	1	0	Reserved*	CRh
0	1	1	0	1	1	RHRd	THRd	1	1	1	0	1	1	RHRh	THRh
0	1	1	1	0	0	Reserved*	Reserved*	1	1	1	1	0	0	Reserved*	Reserved*
0	1	1	1	0	1	Input port B	OPCRB	1	1	1	1	0	1	Input port D	OPCRD
0	1	1	1	1	0	Start C/T B	Reserved*	1	1	1	1	1	0	Start C/T D	Reserved*
0	1	1	1	1	1	Stop C/T B	Reserved*	1	1	1	1	1	1	Stop C/T D	Reserved*

NOTE:

4. Reserved registers should never be read during normal operation since they are reserved for internal diagnostics.

ACR = Auxiliary control register
CR = Command register
CSR = Clock select register
CTL = Counter/timer lower
CTLR = Counter/timer lower register
CTU = Counter/timer upper
CTUR = Counter/timer upper register
MR = Mode register
SR = Status Register
THR = Tx holding register
RHR = Rx holding register
IPCR = Input port change register
ISR = Interrupt status register
IMR = Interrupt mask register
OPCR = Output port configuration registerr

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. Thirteen of these are available simultaneously for use by the receiver and transmitter. Eight are fixed, and one of two sets of five can be selected by programming ACR[7]. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The clock selectors allow the independent selection, by the receiver and transmitter, of any of these baud rates or an external timing signal.

There are four C/Ts in the Octal UART, one for each block. The C/T operation is programmed by ACR[6:4]. One of eight timing sources can be used as the input to the C/T. The output of the C/T is available to the clock selectors and can also be programmed by OPCR[2:0] for channel a and OPCR[6:4] for channel b, to be output on the MPOa or MPOb pin respectively.

A register read address is reserved to issue a start counter/timer command and a second register read address is reserved to issue a stop counter/timer command for each timer. For example, to issue a stop counter command for the counter-timer in block B, a read of address '1F' must be performed. See Table 1 for register addressing.

In the timer mode, the C/T generates a square wave whose period is twice the number of clock periods loaded into the C/T upper and lower registers. The counter ready bit in the ISR is set once each cycle of the square wave. If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half-periods will be affected. In this mode the C/T runs continuously and does not recognize the stop C/T command (the command only resets the counter ready bit in the ISR). Receipt of a start C/T command causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR. Counting begins upon receipt of a start counter command. Upon reaching terminal count, the counter ready bit in the ISR is set. The counter continues counting past the terminal count until stopped by the CPU. If MPO is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and the counter ready bit is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command following a stop counter command. If new values have not been loaded, the previous count values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower eight bits of the counter may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower eight bits to the upper eight bits occurs between the times that both halves of the counter are read. However, a subsequent start counter command causes the counter to begin a new count cycle using the values in CTUR and CTLR.

Receiver and Transmitter

The Octal UART has eight full-duplex asynchronous receiver/transmitters. The operating frequency for the receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input.

Registers associated with the communications channel are the mode registers (MR1 and MR2), the clock select register (CSR), the command register (CR), the status register (SR), the transmit holding register (THR), and the receive holding register (RHR).

Transmitter

The transmitter accepts parallel data from the CPU and converts it to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains high and the TxEMT bit in the SR will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character in the THR. In the 16X clock mode, this also resynchronizes the internal 1X transmitter clock so that transmission of the new character begins with minimum delay.

The transmitter can be forced to send a break (continuous Low condition) by issuing a start break command via the CR. The break is terminated by a stop break command. If the transmitter is disabled, it continues operating until the characters currently being transmitted and the character in the THR, if any, are completely sent out. Characters cannot be loaded in the THR while the transmitter is disabled.

Receiver

The receiver accepts serial data on the RxD pin, converts the serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition, and presents the assembled character to the CPU. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled again each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode).

If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver samples the input. This continues at one bit time intervals, at the theoretical center of the bit, until the proper number of data bits and the parity bit (if any) have been assembled, and one stop bit has been detected. The data is then transferred to the RHR and the RxRDY bit in the SR is set to a one. If the character length is less than eight bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (i.e. framing error) and RxD remains low for one-half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled). The parity error, framing error and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set.

If a break condition is detected (RxD is low for the entire character including the stop bit), only one character consisting of all zeros will be loaded in the FIFO and the received break bit in the SR is set to 1. The RxD input must return to a high condition for two successive clock edges of the 1X clock (internal or external) before a search for the next start bit begins.

TIMEOUT MODE

The timeout mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RHR, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU may not know when there is data left in the FIFO, The CTU and CTL value would be programmed for just over one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all of the characters from the FIFO, but the last character received has started the count. If there is no new data during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

This mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the timeout mode for that channel. Writing a 'Cx' to CRA or CRB will disable the timeout mode. The timeout mode should only be used by one channel at once, since it uses the C/T. CTU and CTL must be loaded with a value greater than the normal receive character period. The timeout mode disables the regular START/STOP counter commands and puts the C/T into counter mode under the

control of the received data stream. Each time a received character is transferred from the shift register to the RHR, the C/T is stopped after one C/T clock, reloaded with the value in CTU and CTL and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Since receiving a character restarts the C/T, the receipt of a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Timeout Mode On' command, CRx='Ax', will also clear the counter ready bit and stop the counter until the next character is received.

RECEIVER FIFO

The RHR consists of a first-in-first-out (FIFO) with a capacity of three characters. Data is loaded from the receive shift register into the top-most empty position of the FIFO. The RxRDY bit in the status register (SR) is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR, outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are appended to each data character in the FIFO. Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical OR of the status for all characters coming to the top of the FIFO since the last reset error command was issued. In either mode, reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore, the SR should be read prior to reading the corresponding data character.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exists, the contents of the FIFO are not affected: the character previously in the shift register is lost and the overrun error status bit, SR[4], will be set upon receipt of the start bit of the new (overrunning) character.

WAKE-UP MODE

In addition to the normal transmitter and receiver operation described above, the Octal UART incorporates a special mode which provides automatic wake-up of the receiver through address frame recognition for multiprocessor communications. This mode is selected by programming bits MR1[4:3] to '11'.

In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, whose receivers are normally disabled, examine the received data stream and 'wake-up' the CPU [by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, an address/data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1[2]; MR1[2] = 0 transmits a zero in the A/D bit position which identifies the corresponding data bits as data; MR1[2] = 1 transmits a one in the A/D bit position which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits in the THR.

While in this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character in the RHR FIFO if the received A/D bit is a one, but discards the received character if the received A/D bit is a zero. If enabled, all received characters are then transferred to the CPU via the RHR. In either case, the data bits are loaded in the data FIFO while the A/D bit is loaded in the status FIFO position normally used for parity error (SR[5]). Framing error, overrun error, and break detect operate normally whether or not the receiver is enabled.

MULTI-PURPOSE INPUT PIN AND MULTI-PURPOSE I/O PINS

The inputs to this unlatched 8-bit port for each block can be read by the CPU, by performing a read operation as shown in Table 1. A High input results in a logic one, while a Low input results in a logic zero. When the input port pins are read on the 84-pin LLCC, they will appear on the data bus in alternating pairs (i.e., DB0 = MP10a, DB1 = MPI1a, DB2 = MPI0b, DB3 = MPI1b, DB4 = MPP1a, DB5 = MPP2a, DB6 = MPP1b, DB7 = MPP2b. Although this example is shown for input port 'A', all ports will have a similar order).

The MPI pin can be programmed as an input to one of several Octal UART circuits. The function of the pin is selected by programming the appropriate control register. Change-of-state detectors are provided for MPI0 and MPI1 for each channel in each block. A High-to-Low or Low-to-High transition of the inputs lasting longer than 25 to 50µs sets the MPI change-of-state bit in the interrupt status register. The bit is cleared via a command. The change-of-state can be programmed to generate an interrupt to the CPU by setting the corresponding bit in the interrupt mask register.

The input port pulse detection circuitry uses a 38.4KHz sampling clock, derived from one of the baud rate generator taps. This produces a sampling period of slightly more than 25µs (assuming a 3.6864MHz oscillator input). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples be observed at the new logic level. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs coincident with the first sample pulse. (The 50µs time refers to the condition where the change-of-state is just missed and the first change of state is not detected until after an additional 25µs.)

The multi-purpose pins can be programmed as inputs or outputs using OPCR[7]. When programmed as inputs, the functions of the pins are selected by programming the appropriate control registers. When programmed as outputs, the two MPP1 pins (per block) will provide the transmitter ready (TxRDY) status for each channel and the MPP2 pins will provide the receiver ready or FIFO full (RxRDY/FFULL) status for each channel.

MULTI-PURPOSE OUTPUT PIN

This pin can be programmed to serve as a request-to-send output, the counter/timer output, the output for the 1X or 16X transmitter or receiver clocks, the TxRDY output or the RxRDY/FFULL output (see OPCR [2:0] and OPCR [6:4] – MPO Output Select).

REGISTERS

The operation of the Octal UART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. Addressing of the registers is described in Table 1.

The bit formats of the Octal UART registers are depicted in Table 2. These are shown for block A. The bit format for the other blocks is the same.

MR1 – Mode Register 1

MR1 is accessed when the MR pointer points to MR1. The pointer is set to MR1 by RESET or by a set pointer command applied via the CR. After reading or writing MR1, the pointers are set at MR2.

MR1[7] – Receiver Request-to-Send Control

This bit controls the deactivation of the RTSN output (MPO) by the receiver. This output is manually asserted and negated by commands applied via the command register. MR1[7] = 1 causes RTSN to be automatically negated upon receipt of a valid start bit if the receiver FIFO is full. RTSN is reasserted when an empty FIFO position is available. This feature can be used to prevent overrun in the receiver by using the RTSN output signal to control the CTS input of the transmitting device.

MR1[6] – Receiver Interrupt Select

This bit selects either the receiver ready status (RxRDY) or the FIFO full status (FFULL) to be used for CPU interrupts.

MR1[5] – Error Mode Select

This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break). In the character mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the block mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last reset error command was issued.

MR1[4:3] – Parity Mode Select

If 'with parity' or 'force parity' is selected, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR1[4:3] = 11 selects the channel to operate in the special wake-up mode.

Table 2. Register Bit Formats

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

MR1 (Mode Register 1)

RxRTS Control	RxINT Select	Error Mode	Parity Mode	Parity Type	Bits per Character
0 = No 1 = Yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With parity 01 = Force parity 10 = No parity 11 = Special mode	0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8

MR2 (Mode Register 2)

Channel Mode	TxRTS Control	CTS Enable Tx	Stop Bit Length[5]
00 = Normal 01 = Auto-echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 4 = 0.813 8 = 1.563 C = 1.813 1 = 0.625 5 = 0.875 9 = 1.625 C = 1.875 2 = 0.688 6 = 0.938 A = 1.688 E = 1.938 3 = 0.750 7 = 1.000 B = 1.750 F = 2.000

NOTE:
5. Add 0.5 to values shown above for 0–7, if channel is programmed for 5 bits/char.

CSR (Clock Select Register)

Receiver Clock Select	Transmitter Clock Select
See text	See text

CR (Command Register)

Miscellaneous Commands	Disable Tx	Enable Tx	Disable Tx	Enable Tx
See text	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE: Access to the upper four bits of the command register should be separated by three (3) edges of the X1 clock.

SR (Status Register)

Rec'd[6] Break	Framing6 Error	Parity6 Error	Overrun Error	TxEMT	TxRDY	FFULL	RxRDY
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
6. These status bits are appended to the corresponding data character in the receive FIFO. A read of the status register provides these bits [7:5] from the top of the FIFO together with bits [4:0]. These bits are cleared by a reset error status command. In character mode, they must be reset when the corresponding data character is read from the FIFO.

OPCR (Output Port Configuration Register)

MPP Function Select	MPOb Pin Function Select	Power-Down Mode[7]	MPOa Pin Function Select
0 = input 1 = output	000 = RTSN 001 = C/TO 010 = TxC (1X) 011 = TxC (16X) 100 = RxC (1X) 101 = RxC (16X) 110 = TxRDY 111 = RxRDY/FF	0 = Off 1 = On	000 = RTSN 001 = C/TO 010 = TxC (1X) 011 = TxC (16X) 100 = RxC (1X) 101 = RxC (16X) 110 = TxRDY 111 = RxRDY/FF

NOTE:
7. Only OPCR[3] in block A controls the power-down mode.

MR1[2] – Parity Type Select
This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special 'wake-up' mode, it selects the polarity of the transmitted A/D bit.

MR1[1:0] – Bits Per Character Select
This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2 – Mode Register 2

MR2 is accessed when the channel MR pointer points to MR2, which occurs after any access to MR1. Accesses to MR2 do not change the pointer.

MR2[7:6] – Mode Select
The Octal UART can operate in one of four modes. MR2[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxD output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e., transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU-to-receiver communication continues normally, but the CPU-to-transmitter link is disabled.

Two diagnostic modes can also be selected. MR2[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxD output is held high.
4. The RxD input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

Table 2. Register Bit Formats (Continued)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

ACR (Auxillary Control Register)

BRG Select	Counter/Timer Mode and Source			Delta MPI1bINT	Delta MPI0bINT	Delta MPI1aINT	Delta MPI0aINT
0 = set 1 1 = set 2	See Text			0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on

IPCR (Input Port Change Register)

Delta MPI1b	Delta MPI0b	Delta MPI1a	Delta MPI0a	MPI1b	MPI0b	MPI1a	MPI0a
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

ISR (Interrupt Status Register)

MPI Port Change	Delta BREAKb	RxRDY/ FFULLb	TxRDYb	Counter Ready	Delta BREAKa	RxRDY/ FFULLa	TxRDYa
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

IMR (Interrupt Mask Register)

MPI Port Change INT	Delta BREAKb INT	RxRDY/ FFULLb INT	TxRDYb INT	Counter Ready INT	Delta BREAKa INT	RxRDY/ FFULLa INT	TxRDYa INT
0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on

CTUR (Counter/Timer Upper Register)

C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]

CTUR (Counter/Timer Lower Register)

C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]

IPR (Input Port Register)

MPP2b	MPP1b	MPP2a	MPP1a	MPI1b	MPI0b	MPI1a	MPI0a
0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

NOTE: When TxEMT and TxRDY bits are at one just before a write to the Transmit Holding register, a command to disable the transmitter should be delayed until the TxRDY is at one again. TxRDY will set to one at the end of the start bit time.

The second diagnostic mode is the remote loopback mode, selected by MR2[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TXD output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., the transmitted parity bit is as received.
5. The receiver must be enabled, but the transmitter need not be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected.

tje devoce wo;; switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes; if the deselection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop bit has been retransmitted.

MR2[5] – Transmitter Request-to–Send Control
This bit controls the deactivation of the RTSN output (MPO) by the transmitter. This output is manually asserted and negated by appropriate commands issued via the command register. MR2[5] = 1 causes RTSN to be reset automatically one bit time after the characters in the transmit shift register and in the THR (if any) are completely transmitted (includes the programmed number of stop bits if the transmitter is not enabled). This feature can be used to automatically terminate the transmission as follows:

1. Program auto-reset mode: MR2[5] = 1.
2. Enable transmitter.
3. Assert RTSN via command.
4. Send message.
5. Verify the next to last character of the message is being sent by waiting until transmitter ready is asserted. Disable transmitter after the last character of the message is loaded in the THR.
6. The last character will be transmitted and RTSN will be reset one bit time after the last stop bit.

NOTE: When TxEMT and TxRDY bits are at one just before a write to the Transmit Holding register, then a command to disable the transmitter should be delayed until the TxRDY is at one again. TxRDY will set to one at the end of the start bit.

MR2[4] – Clear-to-Send Control
The sate of this bit determines if the CTSN input (MPI) controls the operation of the transmitter. If this bit is 0, CTSN has no effect on the transmitter. If this bit is a 1, the transmitter checks the sate of CTSN each time it is ready to send a character. If it is asserted (Low), the character is transmitted. If it is negated (High), the TxD output remains in the marking state and the transmission is delayed until CTSN goes Low. Changes in CTSN, while a character is being transmitted do not affect the transmission of that character. This feature can be used to prevent overrun of a remote receiver.

MR2[3:0] – Stop Bit Length Select
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1–9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character length of 5 bits, 1–1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a mark condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit if parity is enabled). If an external 1X clock is used for the transmitter, MR2[3] = 0 selects one stop bit and MR2[3] = 1 selects two stop bits to be transmittted.

CSR – Clock Select Register

CSR[7:4] – Receiver Clock Select
When using a 3.6864MHz crystal or external clock input, this field selects the baud rate clock for the receiver as shown in Table 3.

Table 3. Baud Rate

CSR[7:4]	ACR[7] = 0	ACR[7] = 1
0 0 0 0	50	75
0 0 0 1	110	110
0 0 1 0	134.5	38.4k
0 0 1 1	200	150
0 1 0 0	300	300
0 1 0 1	600	600
0 1 1 0	1,200	1,200
0 1 1 1	1,050	2,000
1 0 0 0	2,400	2,400
1 0 0 1	4,800	4,800
1 0 1 0	7,200	1,800
1 0 1 1	9,600	9,600
1 1 0 0	38.4k	19.2k
1 1 0 1	Timer	Timer
1 1 1 0	MP2 – 16X	MP2 – 16X
1 1 1 1	MP2 – 1X	MP2 – 1X

The receiver clock is always a 16X clock, except for CSR[7:4] = 1111. When MPP2 is selected as the input, MPP2a is for channel a and MPP2b is for channel b.

CSR[3:] – Transmitter Clock Select
This field selects the baud rate clock for the transmitter. The field definition is as shown in Table 3, except as follows:

CSR[3:0]	ACR[7] = 0	AC
R[7] = 1		
1 1 1 0	MPP1 – 16X	MP
P1 – 16X		
1 1 1 1	MPP1 – 1X	MP
P1 – 1X		

When MPP1 is selected as the input, MPP1a is for channel a and MPP1b is for channel b.

CR – Command Register

CR is used to write commands to the Octal UART.

CR[7:4] – Miscellaneous Commands
The encoded value of this field can be used to specify a single command as follows:

NOTE: Access to the upper four bits of the command register should be separated by three (3) edges of the X1 clock.

0000 No command.
0001 Reset MR pointer. Causes the MR pointer to point to MR1.
0010 Reset receiver. Resets the receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO pointer is reset to the first location.
0011 Reset transmitter. Resets the transmitter as if a hardware reset had been applied.
0100 Reset error status. Clears the received break, parity error, framing error, and overrun error bits in the status register (SR[7:4]}. Used in character mode to clear OE status (although RB, PE, and FE bits will also be cleared), and in block mode to clear all error status after a block of data has been received.
0101 Reset break change interrupt. Causes the break detect change bit in the interrupt status register (ISR[2 or 6]) to be cleared to zero.
0110 Start break. Forces the TxD output low (spacing). If the transmitter is empty, the start of the break condition will be delayed up to two bit times. If the transmitter is active, the break begins when transmission of the character is completed. If a character is in the THR, the start of break is delayed until that character or any others loaded after it have been transmitted (TxEMT must be true before break begins). The transmitter must be enabled to start a break
0111 Stop break. The TxD line will go high (marking) within two bit times. TxD will remain high for one bit time before the next character, if any, is transmitted.
1000 Assert RTSN. Causes the RTSN output to be asserted (Low).
1001 Negate RTSN. Causes the RTSN output to be negated (High).
1010 Set Timeout Mode On. The register in this channel will restart the C/T as each receive character is transferred from the shift register to the RHR. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset.
1011 Reserved.

1100 Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued.

1101 Reserved.

111x Reserved for testing.

CR[3] – Disable Transmitter
This command terminates transmitter operation and resets the TxRDY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CR[2] – Enable Transmitter
Enables operation of the transmitter. The TxRDY status bit will be asserted.

CR[1] – Disable Receiver
This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special wake–up mode is programmed, the receiver operates even if it is disabled (see Wake-up Mode).

CR[0] – Enable Receiver
Enables operation of the receiver. If not in the special wake-up mode, this also forces the receiver into the search for start bit state.

SR – Channel Status Register

SR[7] – Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received; further entries to the FIFO are inhibited until the RxDA line returns to the marking state for at least one-half bit time (two successive edges of the internal or external 1x clock).

When this bit is set, the change in break bit in the ISR (ISR[6 or 2]) is set. ISR[6 or 2] is also set when the end of the break condition, as defined above, is detected. The break detect circuitry is capable of detecting breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must last until the end of the next character in order for it to be detected.

SR[6] – Framing Error (FE)
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SR[5]– Parity Error (PE)
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity. In special 'wake-up mode', the parity error bit stores the received A/D bit.

SR[4] – Overrun Error (OE)
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost. This bit is cleared by a reset error status command.

SR[3] – Transmitter Empty (TxEMT)
This bit will be set when the transmitter underruns, i.e., both the transmit holding register and the transmit shift register are empty. It is set after transmission of the last stop bit of a character, If no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU, or when the transmitter is disabled.

SR[2] – Transmitter Ready (TxRDY)
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, e.g., characters loaded in the THR while the transmitter is disabled will not be transmitted.

SR[1] – FIFO Full (FFULL)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the FIFO and there is no character in the receive shift register. If a character is waiting in the receive shift register because the FIFO is full, FFULL is not reset after reading the FIFO once.

SR[0] – Receiver Ready (RxRDY)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR, and no more characters are in the FIFO.

OPCR – Output Port Configuration Register

OPCR[7] – MPP Function Select
When this bit is a zero, the MPP pins function as inputs, to be used as general purpose inputs or as receiver or transmitter external clock inputs. When this bit is set, the MPP pins function as outputs. MPP1 will be a TxRDY indicator, and MPP2 will be an RxRDY/FFULL indicator.

OPCR[6:4] – MPOb Output Select
This field programs the MPOb output pin to provide one of the following:

000 Request-to-send active-Low output (RTSN). This output is asserted and negated via the command register. Mode RTSN can be programmed to be automatically reset after the character in the transmitter is completely shifted out or when the receiver FIFO and receiver shift register are full using MR2[5] and MR1[7], respectively.

001 The counter/timer output. In the timer mode, this output is a square wave with a period of twice the value (in clock periods) of the contents of the CTUR and CTLR. In the counter mode, the output remains high until the terminal count is reached, at which time it goes low. The output returns to the High state when the counter is stopped by a stop counter command.

010 The 1X clock for the transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a non-synchronized 1X clock is output.

011 The 16X clock for the transmitter. This is the clock selected by CSR[3:0], and is a 1X clock if CSR[3:0] = 1111.

100 The 1X clock for the receiver, which is the clock that samples the received data. If data is not being received, a non-synchronized 1X clock is output.

101 The 16X clock for the receiver. This is the clock selected by CSR[7:4], and is a 1X clock if CSR[7:4] = 1111.

110 The transmitter register empty signal, which is the same as SR[3].

111 The receiver ready or FIFO full signal.

OPCR[3] – Power Down Mode Select
This bit, when set, selects the power-down mode. In this mode, the 2698B oscillator is

stopped and all functions requiring this clock are suspended. The contents of all registers are saved. It is recommended that the transmitter and receiver be disabled prior to placing the 2698B in this mode. This bit is reset with RESET asserted. Note that this bit must be set to a logic 1 after power up. Only OPCR[3] in block A controls the power-down mode.

OPCR[2:0] – MPOa Output Select
This field programs the MPOa output pin to provide one of the same functions as described in OPCR[6:4].

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects one of two sets of baud rates generated by the BRG.

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.

Set 2: 75, 110, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, 19.2k, and 38.4k baud.

The selected set of rates is available for use by the receiver and transmitter.

ACR[6:4] – Counter/Timer Mode and Clock Source Select
This field selects the operating mode of the counter/timer and its clock source (see Table 4).

The MPI1 pin available as the Counter/Timer clock source is MPI1 a,c,e, and g only.

Table 4. ACR[6:4] Operating Mode

[6:4]	Mode	Clock Source
0 0 0	Counter	MPI1a pin
0 0 1	Counter	MPI1a pin divided by 16
0 1 0	Counter	TxC–1XA clock of the transmitter
0 1 1	Counter	Crystal or external clock (X1/CLK) divided by 16
1 0 0	Timer	MPI1a pin
1 0 1	Timer	MPI1a pin divided by 16
1 1 0	Timer	Crystal or external clock (X1/CLK)
1 1 1	Timer	Crystal or external clock (X1/CLK) divided by 16

ACR[3:0] – MPI1b, MPI0b, MPI1a, MPI0a Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register, ISR[7], to be set. If a bit is in the 'on' state, the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7:4] – MPI1b, MPI0b, MPI1a, MPI0a Change-of-State
These bits are set when a change of state, as defined in the Input Port section of this data sheet, occurs at the respective pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – MPI1b, MPI0b, MPI1a, MPI0a Change-of-State
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the inputs pins during the time the IPCR is read.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the interrupt mask register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output is asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR; the true status is provided regardless of the contents of the IMR.

ISR[7] – MPI Change-of-State
This bit is set when a change-of-state occurs at the MPI1b, MPI0b, MPI1a, MPI0a input pins. It is reset when the CPU reads the IPCR.

ISR[6] – Channel b Change in Break
This bit, when set, indicates that the receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a reset break change interrupt command.

ISR[5] – Receiver Ready or FIFO Full Channel b
The function of this bit is programmed by MR1[6]. If programmed as receiver ready, it indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the receiver FIFO. If the FIFO contains more characters, the bit will be set again after the FIFO is read.

If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when FIFO is read and there is no character in the receiver shift register. If there is a character waiting in the receive shift register because the FIFO is full, the bit is set again when the waiting character is transferred into the FIFO.

ISR[4] – Transmitter Ready Channel b
This bit is a duplicate of TxRDY (SR[2]).

ISR[3] – Counter Ready
In the counter mode of operation, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command. It is initialized to '0' when the chip is reset.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time the C/T reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the C/T.

ISR[2] – Channel a Change in Break
This bit, when set, indicates that the receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a reset break change interrupt command.

ISR[1] – Receiver Ready or FIFO Full Channel a
The function of this bit is programmed by MR1[6]. If programmed as receiver ready, it indicates that a character has been received and is waiting in the FIFO to be ready by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the receiver FIFO. If the FIFO contains more characters, the bit will be set again after the FIFO is read. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when FIFO is read and there is no character in the receiver shift register. If there is a character waiting in the receive shift register because the FIFO is full, the bit is set again when the waiting character is transferred into the FIFO.

ISR[0] – Transmitter Ready Channel a
This bit is a duplicate of TxRDY (SR[2]).

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR cause an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is a '1', the INTRN output is asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is H'0002'. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. The waveform so generated is often used for a data clock. The formula for calculating the divisor n to load to the CTUR and CTLR for a particular 1X data clock is shown below:

$$n = \frac{C/T\ Clock\ Frequency}{2 \times 16\ Baud\ rate\ desired}$$

Often this division will result in a non-integer number; 26.03, for example. One can only program integer numbers in a digital divider. Therefore, 26 would be chosen. This gives a baud rate error of 0.03/26.3 which is .114%; well within the ability asynchronous mode of operation.

If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half-periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read at adddress A3–A0 = 1110). After this, while in timer mode, the C/T will run continuously. Receipt of a subsequent sttart counter command causes the C/T to terminate the current timing cycle and to begin a new cycle using the values in the CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command read with A3–A0 = H'F'). The command, however, does not stop the C/T. The generated square wave is output on MPO if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded in CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching the terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If MPO is programmed to be the output of the C/T, the output remains High until the terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command. If new values have not been loaded, the previous values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower eight bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower eight bits to the upper eight bits occurs between the times that both halves of the counter is read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	Note 4	°C
T_{STG}	Storage temperature range	–65 to +150	°C
V_{CC}	Voltage from V_{DD} to GND[3]	–0.5 to +7.0	V
V_S	Voltage from any pin to ground[3]	–0.5 to V_{CC} +0.5	V
P_D	Power dissipation	1	W

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range. See ordering information table for applicable temperature range and operating supply range.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL} V_{IH} V_{IH}	Input low voltage Input high voltage (except X1/CLK) Input high voltage (X1/CLK)		 2.0 $0.8V_{CC}$		0.8	V V V
V_{OL} V_{OH}	Output Low voltage Output High voltage (except OD outputs)	I_{OL} = 2.4mA I_{OH} = –400µA I_{OH} = –100µA	 $0.8V_{CC}$ $0.9V_{CC}$		0.4	V V V
I_{IL} I_{IH}	Input current Low, MPI and MPP pins Input current High, MPI and MPP pins	V_{IN} = 0 V_{IN} = V_{CC}	–50		 20	µA µA
I_I	Input leakage current	V_{IN} = 0 to V_{CC}	–10		10	µA
I_{ILX1} I_{IHX1}	X1/CLK input Low current X1/CLK input High current	V_{IN} = GND, X2 = open V_{IN} = V_{CC}, X2 = open	–100		 100	µA µA
I_{OZH} I_{OZL}	Output off current High, 3-State data bus Output off current Low, 3-State data bus	V_{IN} = V_{CC} V_{IN} = 0	 –10		10	 µA
I_{ODL} I_{ODH}	Open-drain output Low current in off state: IRQN Open-drain output Low current in off state: IRQN	V_{IN} = V_{CC} V_{IN} = 0	–10		 10	 µA
I_{CC}	Power supply current Operating mode				30	mA
	Power down mode[9]				2.0	mA

NOTES:
1. Parameters are valid over specified temperature range. See ordering information table for applicable temperature range and operating supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of V_{IL} and V_{IH}, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test condition for interrupt and MPP outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}. Test conditions for rest of outputs: C_L = 150pF.
5. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
6. If CEN is used as the 'strobing' input, the parameter defines the minimum high times between one CEN and the next. The RDN signal must be negated for t_{RWD} guarantee that any status register changes are valid.
7. Consecutive write operations to the command register require at least three edges of the X1 clock between writes.
8. This value is not tested, but is guaranteed by design.
9. See UART applications note for power down currents less than 5µA.
10. Operation to 0MHz is assured by design. Minimum test frequency is 2MHz.

AC Electrical characteristics[1, 2, 3, 4]

SYMBOL	FIGURE	PARAMETER	LIMITS Min	Typ	Max	UNIT
Reset timing						
t_{RES}	3	Reset pulse width	200			ns
Bus timing[5]						
t_{HS}	4	A0–A5 setup time to RDN, WRN Low	10			ns
t_{AH}	4	A0–A5 hold time from RDN, WRN Low	100			ns
t_{CS}[6]	4	CEN setup time to RDN, WRN Low	0			ns
t_{CH}[6]	4	CEN hold time from RDN, WRN High	0			ns
t_{RW}	4	WRN, RDN pulse width Low	225			ns
t_{DD}	4	Data valid after RDN Low			200	ns
t_{DF}	4	Data bus floating after RDN High			80	ns
t_{DS}	4	Data setup time before WRN High	100			ns
t_{DH}	4	Data hold time after WRN High	10			ns
t_{RWD}[7]	4	Time between reads and/or writes	100			ns
MPI and MPO timing[5]						
t_{PS}	5	MPI or MPP input setup time before RDN Low	0			ns
t_{PH}	5	MPI or MPP input hold time after RDN High	0			ns
t_{PD}	5	MPO output valid from WRN High RDN Low			 250 250	 ns ns
Interrupt timing						
t_{IR}	6	INTRN negated or MPP output High from: Read RHR (RxRDY/FFULL interrupt) Write THR (TxRDY interrupt) Reset command (break change interrupt) Reset command (MPI change interrupt) Stop C/T command (counter interrupt) Write IMR (clear of interrupt mask bit)			 270 270 270 270 270 270	 ns ns ns ns ns ns
Clock timing						
t_{CLK}	7	X1/CLK high or low time	120			ns
t_{CLK}	7	X1/CLK frequency[10]	0	3.6864	4.0	MHz
t_{CTC}	7	Counter/timer clock high or low time	120			ns
f_{CTC}	7	Counter/timer clock frequency	0[8]		4.0	MHz
t_{RX}	7	RxC high or low time	200			ns
f_{RX}	7	RxC frequency (16X) RxC frequency (1X)	0[8] 0[8]		2.0 1.0	MHz MHz
t_{TX}	7	TxC high or low time	200			ns
f_{TX}	7	TxC frequency (16X) TxC frequency (1X)	0[8] 0[8]		2.0 1.0	MHz MHz
Transmitter timing						
t_{TXD}	8	TxD output delay from TxC low			350	ns
t_{TCS}	8	TxC output delay from TxD output data	0		150	ns
Receiver timing						
t_{RXS}	9	RxD data setup time to RxC high	50			ns
t_{RXH}	9	RxD data hold time from RxC high	100			ns

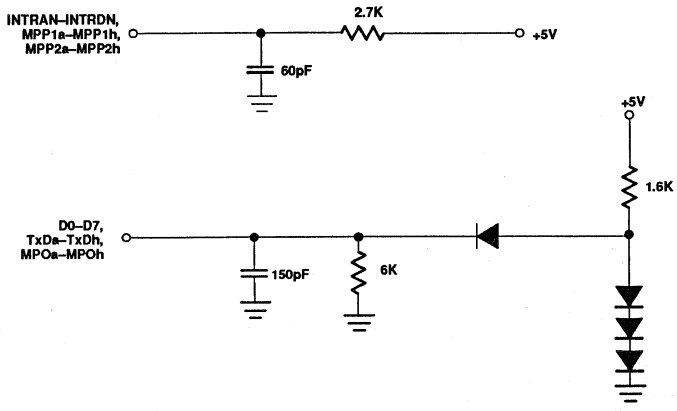


Figure 1. Test Conditions on Outputs

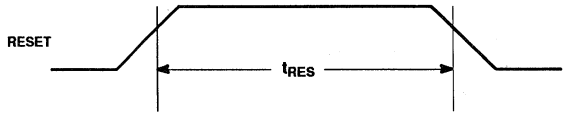


Figure 2. Reset Timing

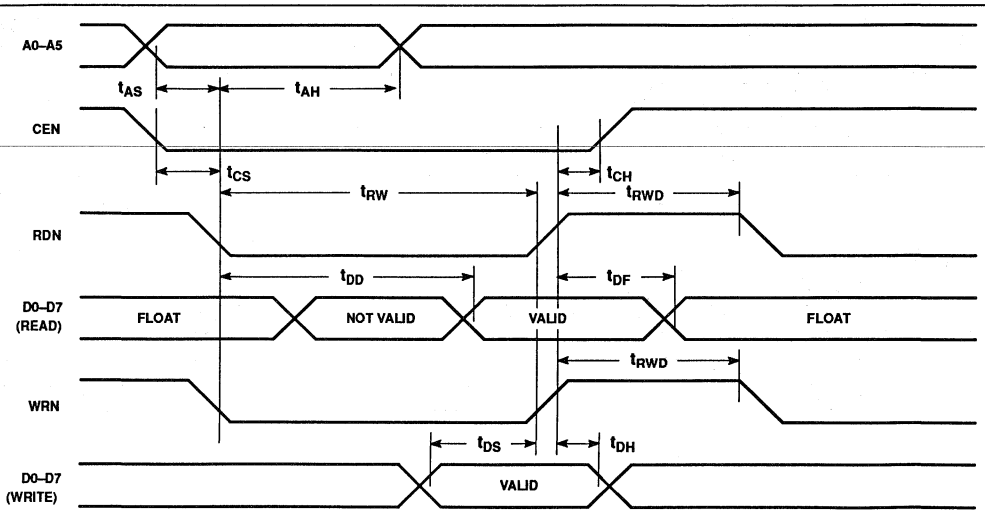


Figure 3. Bus Timing

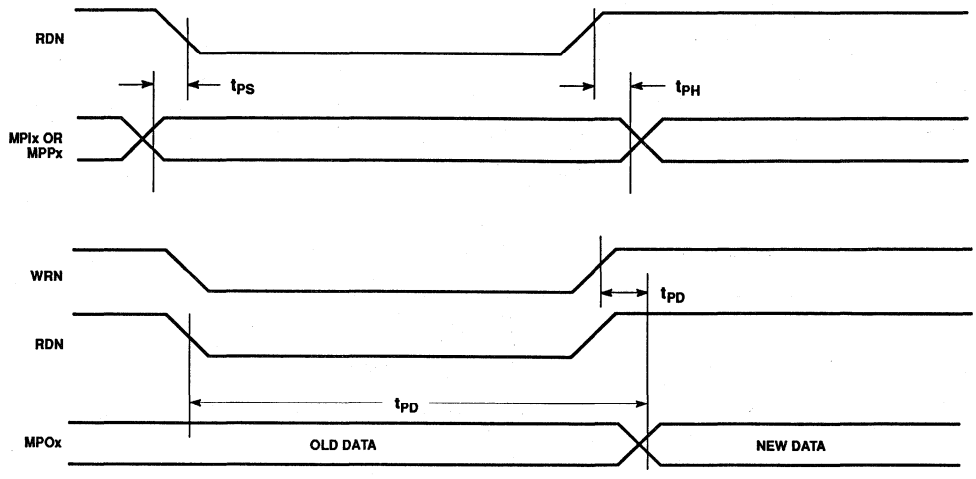
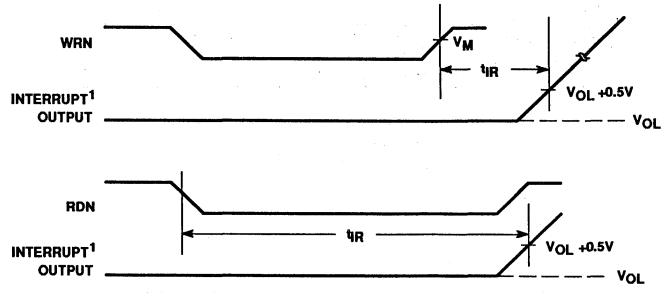
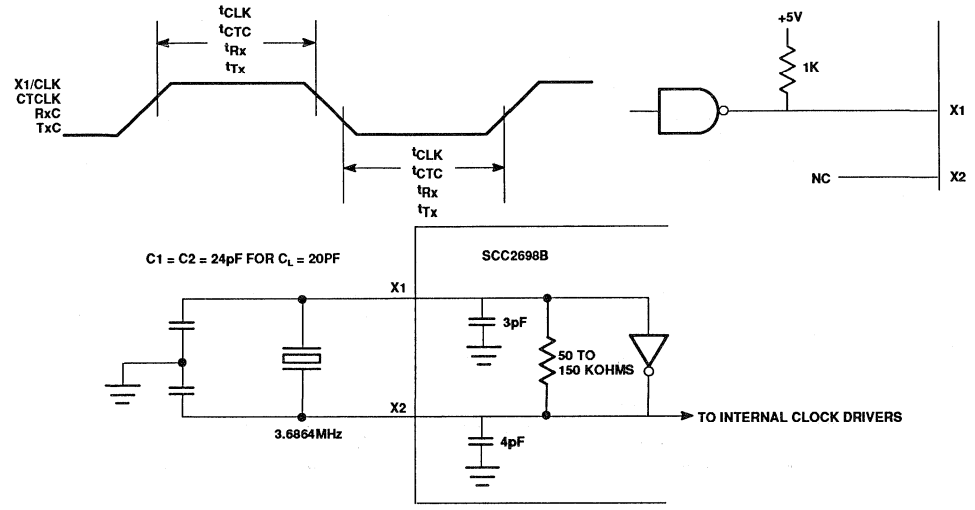


Figure 4. Port Timing



NOTES:
1. INCLUDES MPP WHEN USED AS TxRDY or RxDY/FFULL OUTPUTS AS WELL AS INTRN.
2. THE TEST FOR OPEN DRAIN OUTPUTS IS INTENDED TO GUARANTEE SWITCHING OF THE OUTPUT TRANSISTOR. MEASUREMENT OF THIS RESPONSE IS REFERENCED FROM THE MIDPOINT OF THE SWITCHING SIGNAL, V_M, TO A POINT 0.5V ABOVE V_{OL}. THIS POINT REPRESENTS NOISE MARGIN THAT ASSURES TRUE SWITCHING HAS OCCURRED. BEYOND THIS LEVEL, THE EFFECTS OF EXTERNAL CIRCUITRY AND TEST ENVIRONMENT ARE PRONOUNCED AND CAN GREATLY AFFECT THE RESULTANT MEASUREMENT.

Figure 5. Interrupt Timing



NOTE:
C1 AND C2 SHOULD BE BASED ON MANUFACTURER'S SPECIFICATION.

TYPICAL CRYSTAL SPECIFICATION

FREQUENCY:	2 – 4MHZ
LOAD CAPACITANCE (C_L):	12 – 32pF
TYPE OF OPERATION:	PARALLEL RESONANT, FUNDAMENTAL MODE

Figure 6. Clock Timing

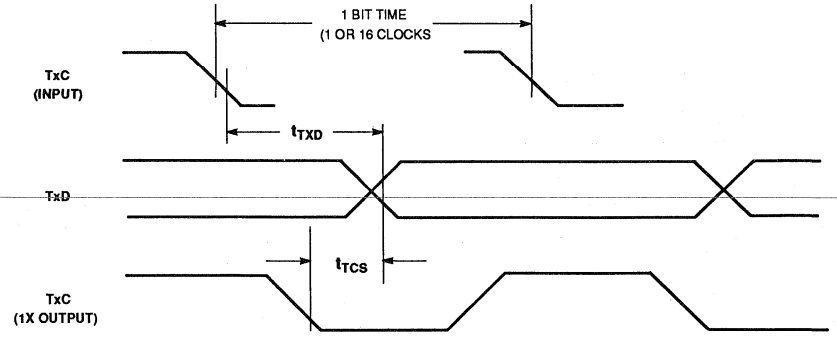


Figure 7. Transmit Timing

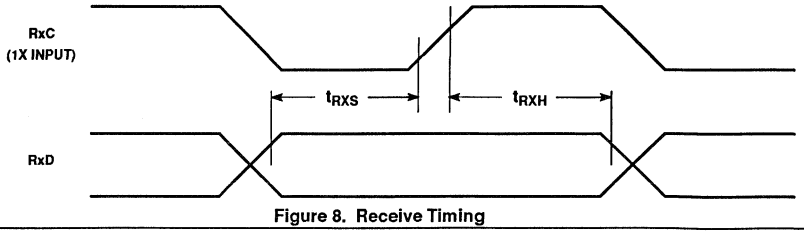


Figure 8. Receive Timing

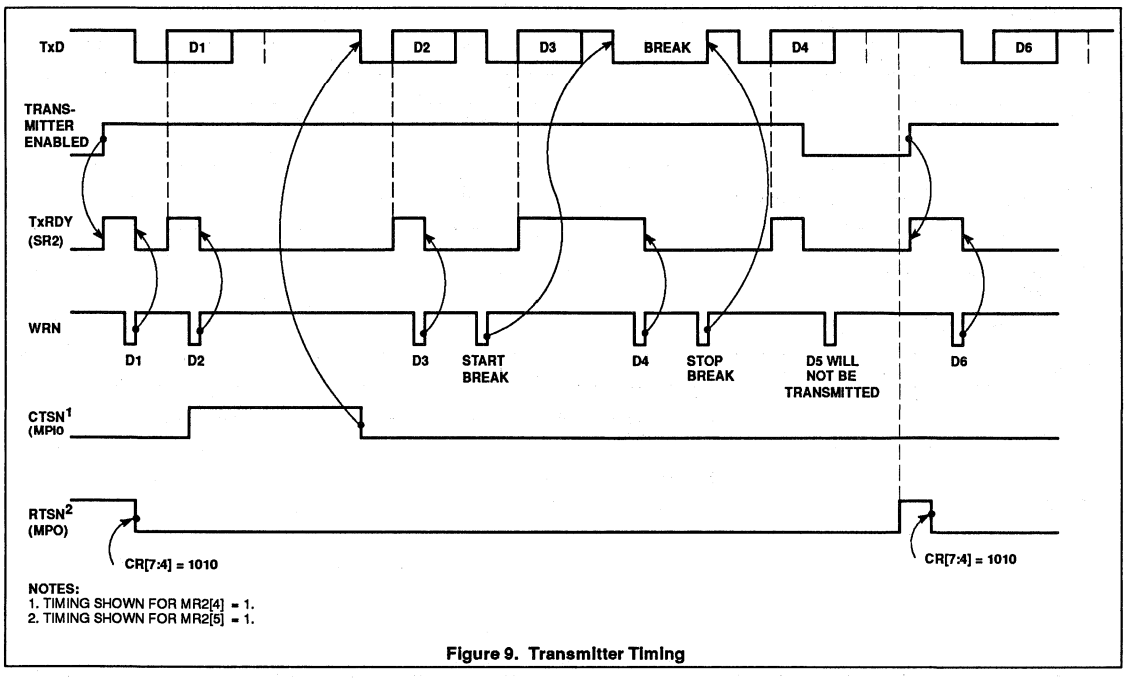


Figure 9. Transmitter Timing

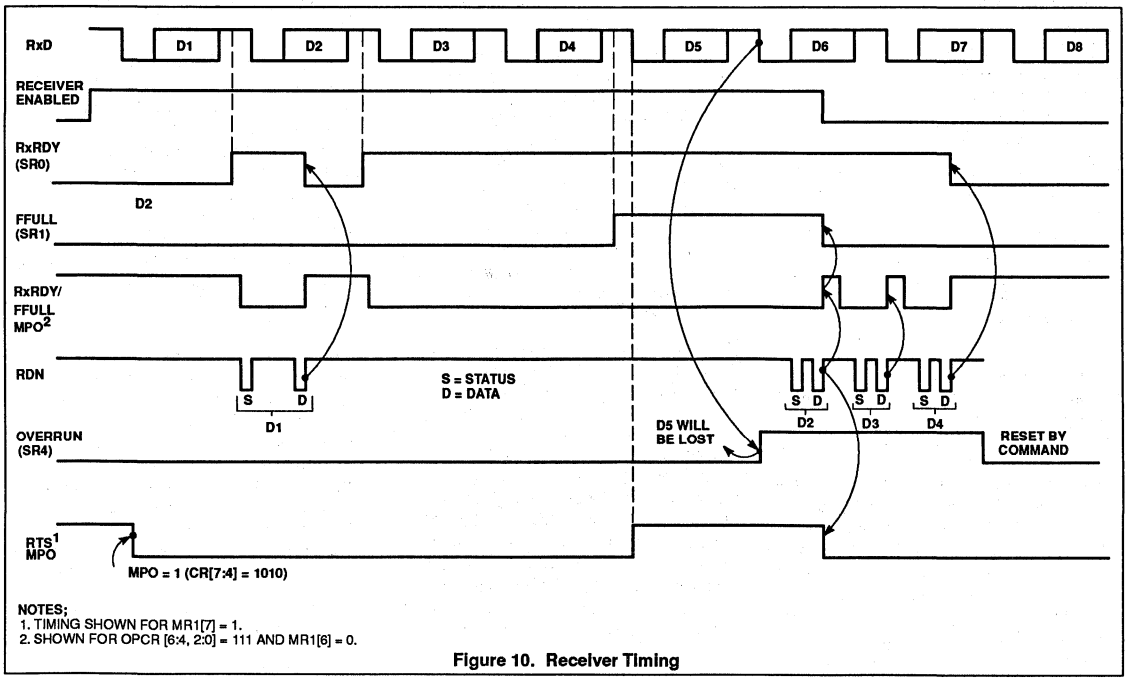


Figure 10. Receiver Timing

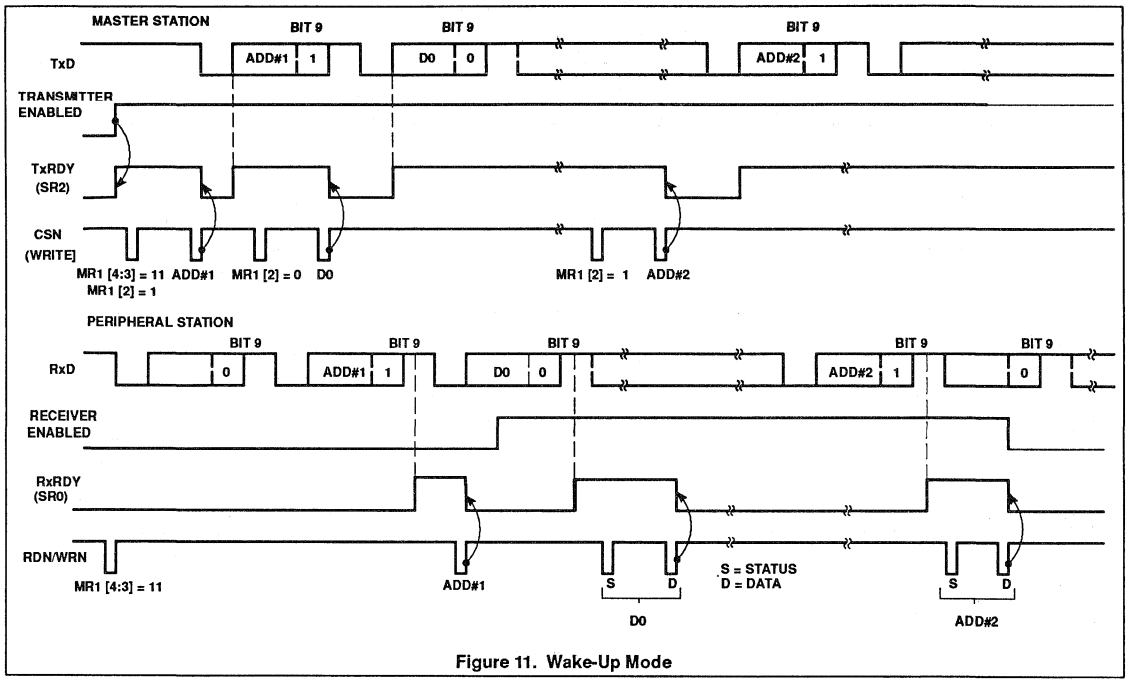


Figure 11. Wake-Up Mode

The CTS, RTS, CTS Enable Tx signals

CTS (Clear To Send) is usually meant to be a signal to the transmitter meaning that it may transmit data to the receiver. The CTS input is on pin MPI. The CTS signal is active low; thus, it is called CTS.

RTS is usually meant to be a signal from the receiver indicating that the receiver is ready to receive data. It is also active low and is, thus, called RTSN. RTSN is on pin MP0. A receiver's RTS output will usually be connected to the CTS input of the associated transmitter. Therefore, one could say that RTS and CTS are different ends of the same wire!

MR2(4) is the bit that allows the transmitter to be controlled by the CTS pin (MPI). When this bit is set to one AND the CTS input is driven high, the transmitter will stop sending data at the end of the present character being serialized. It is usually the RTS output of the receiver that will be connected to the transmitter's CTS input. The receiver will set RTS high when the receiver FIFO is full AND the start bit of the fourth character is sensed. Transmission then stops with four valid characters in the receiver. When MR2(4) is set to one, CTSN must be at zero for the transmitter to operate. If MR2(4) is set to zero, the MP pin will have no effect on the operation of the transmitter.

MR1(7) is the bit that allows the receiver to control MP0. When MP0 is controlled by the receiver, the meaning of that pin will be RTS. However, a point of confusion arises in that MP0 may also be controlled by the transmitter. When the transmitter is controlling this pin, its meaning is not RTS at all. It is, rather, that the transmitter has finished sending its last data byte. Programming the MP0 pin to be controlled by the receiver and the transmitter at the same time is allowed, but would usually be incompatible.

RTS can also be controlled by the commands 1000 and 1001 in the command register. RTS is expressed at the MP0 pin which is still an output port. Therefore, the state of MP0 should be set low (either by commands of the CR register or by writing to the Set Output Ports Register) for the receiver to generate the proper RTS signal. The logic at the output is basically a NAND of the MP0 bit register and the RTS signal as generated by the receiver. When the RTS flow control is selected via the MR(7) bit the state of the MP0 register is not changed. Terminating the use of "Flow Control" (via the MR registers) will return the MP0 pin to the control of the MP0 register.

Transmitter Disable Note

The sequence of instructions enable transmitter — load transmit holding register — disable transmitter will result in nothing being sent if the time between the end of loading the transmit holding register and the disable command is less that 3/16 bit time in the 16x mode or one bit time in the 1x mode. Also, if the transmitter, while in the enabled state and underrun condition, is immediately disabled after a single character is loaded to the transmit holding register, that character will not be sent.

In general, when it is desired to disable the transmitter before the last character is sent AND the TxEMT bit is set in the status register (TxEMT is always set if the transmitter has underrun or has just been enabled), be sure the TxRDY bit is active immediately before issuing the transmitter disable instruction. TxRDY sets at the end of the "start bit" time. It is during the start bit that the data in the transmit holding register is transferred to the transmit shift register.

Non-standard baud rates are available as shown in Table 6 below, via the BRG Test function.

Table 5. Baud Rate

	Normal BRG		BRG Test	
CSR[7:4]	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0000	50	75	4,800	7,200
0001	110	110	880	880
0010	134.5	38.4K	1,076	38.4K
0011	200	150	19.2K	14.4K
0100	300	300	28.8K	28.8K
0101	600	600	57.6K	57.6K
0110	1,200	1,200	115.2K	115.2K
0111	1,050	2,000	1,050	2,000
1000	2,400	2,400	57.6K	57.6K
1001	4,800	4,800	4,800	4,800
1010	7,200	1,800	57.6K	14.4K
1011	9,600	9,600	9,600	9,600
1100	38.4K	19.2K	38.4K	19.2K
1101	Timer	Timer	Timer	Timer
1110	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X
1111	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X

NOTE:
Each read on address H'2' will toggle the baud rate test mode. When in the BRG test mode, the baud rates change as shown to the left. This change affects all receivers and transmitters on the DUART. Also, the RTSN output (MP0) become the transmitter 1x clock.

The test mode at address H'2' changes all transmitters and receivers to the 1x mode and connects the output ports to some internal nodes.

Dual universal serial communications controller (DUSCC)

SCN26562

DESCRIPTION

The Signetics SCN26562 Dual Universal Serial Communications Controller (DUSCC) is a single-chip MOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SCN26562 interfaces to synchronous bus MPUs and is capable of program-polled, interrupt driven, block-move or DMA data transfers.

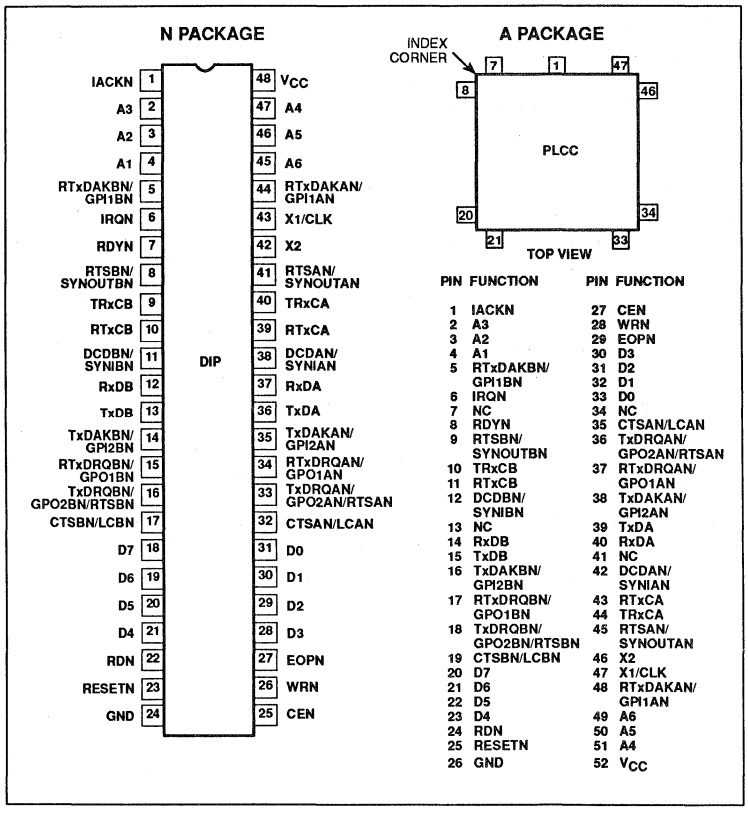
The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multi-function counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides 16 common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock, making the DUSCC well suited for dual-speed channel applications. Data rates up to 4Mbits per second are supported.

The transmitter and receiver each contain a four-deep FIFO with appended transmitter command and receiver status bits and a shift register. This permits reading and writing of up to four characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs and outputs are general purpose in nature, they can be optionally programmed for other functions.

This document contains the electrical specifications for the SCN26562. See SCN26562/SCN68562 User's Guide for complete functional description.

PIN CONFIGURATIONS



PIN	FUNCTION	PIN	FUNCTION
1	IACKN	27	CEN
2	A3	28	WRN
3	A2	29	EOPN
4	A1	30	D3
5	RTxDAKBN/ GPI1BN	31	D2
6	IRQN	32	D1
7	NC	33	D0
8	RDYN	34	NC
9	RTSBN/ SYNOUTBN	35	CTSAN/LCAN
10	TRxCB	36	TxDRQAN/ GPO2AN/RTSAN
11	RTxCB	37	RTxDRQAN/ GPO1AN
12	DCDBN/ SYNIBN	38	TxDAKAN/ GPI2AN
13	NC	39	TxDA
14	RxDB	40	RxDA
15	TxDB	41	NC
16	TxDAKBN/ GPI2BN	42	DCDAN/ SYNIAN
17	RTxDRQBN/ GPO1BN	43	RTxCA
18	TxDRQBN/ GPO2BN/RTSBN	44	TRxCA
19	CTSBN/LCBN	45	RTSAN/ SYNOUTAN
20	D7	46	X2
21	D6	47	X1/CLK
22	D5	48	RTxDAKAN/ GPI1AN
23	D4	49	A6
24	RDN	50	A5
25	RESETN	51	A4
26	GND	52	VCC

FEATURES

General Features

- Dual full-duplex synchronous/asynchronous receiver and transmitter
- Multiprotocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
  - COP: BISYNC, DDCMP
  - ASYNC: 5–8 bits plus optional parity
- Four character receiver and transmitter FIFOs
- 0 to 4Mbit/sec data rate
- Programmable bit rate for each receiver and transmitter selectable from:
  - 16 fixed rates: 50 to 38.4k baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
  - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- and half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Single- or dual-address dual transfers
  - Half- or full-duplex operation
  - Automatic frame termination on counter/timer terminal count or DMA EOPN input
- Interrupt capabilities
  - Vector output (fixed or modified by status)
  - Programmable internal priorities
  - Maskable interrupt conditions
- Multi-function programmable 16-bit counter/timer
  - Bit rate generator
  - Event counter

  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general purpose pins per channel
  - CTS and DCD programmable auto-enables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- 1X or 16X and Tx clock factors
- Parity, overrun, and framing error detection
- False start bit detection
- Start bit search 1/2-bit time after framing error detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmits up to 4Mbit/sec data rate
  Receives up to 2Mbit/sec data rate

Character-Oriented Protocol Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK linefill on underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun, and underrun error detection

BISYNC Features

- EBCDIC or ASCII header, text and control messages
- SYN, DLE stripping
- EOM (end of message) detection and transmission
- Auto transparent mode switching
- Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
- Control character sequence detection for both transparent and normal text

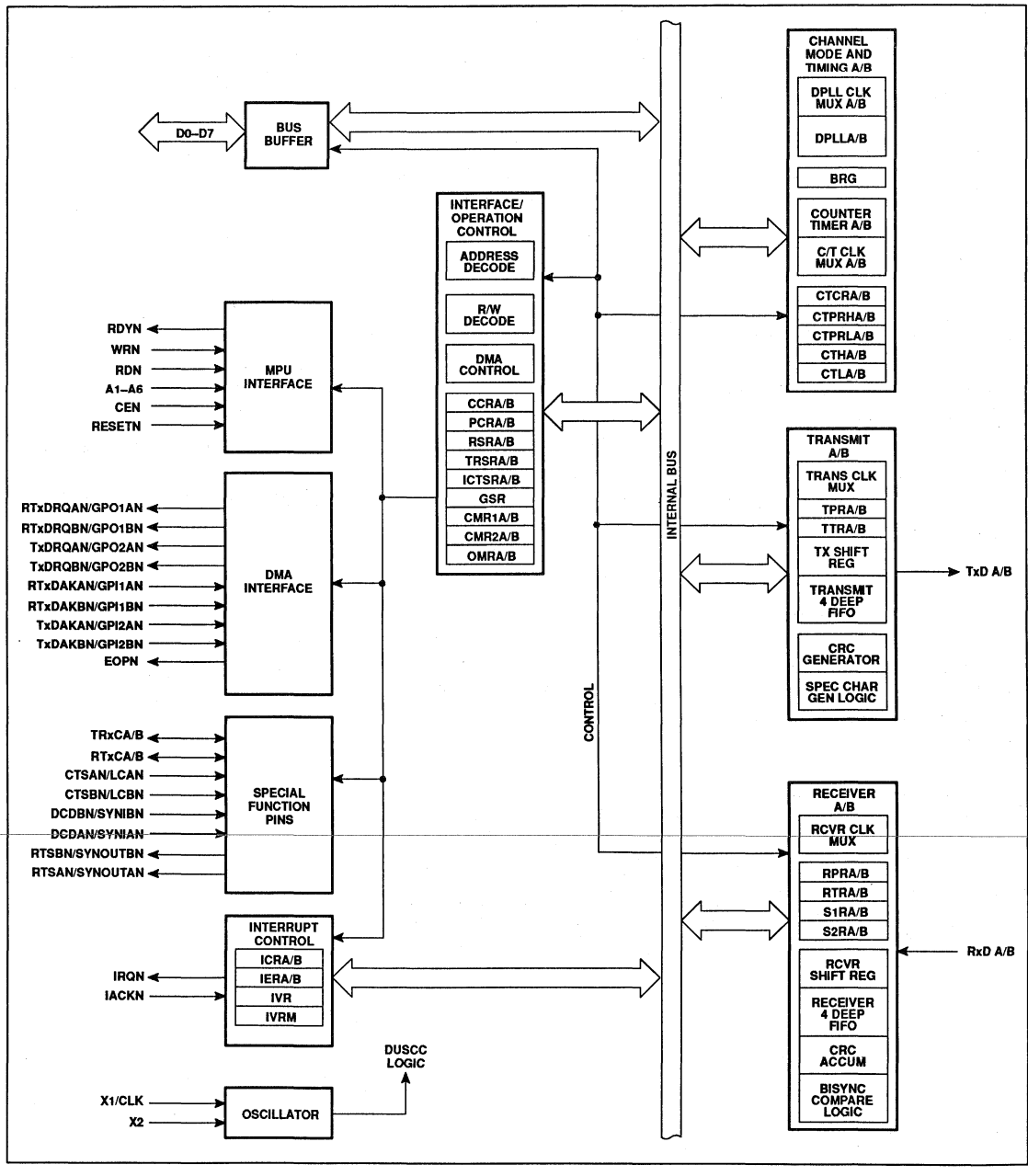
Bit-Oriented Protocol Features

- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Automatic switch to programmed character length for I field
- Zero insertion and detection
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- ABORT, ABORT-FLAGs, or FCS FLAGs linefill on underrun
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±5%, T_A = 0°C to +70°C	
	Serial Data Rate = 2.5Mbps Maximum	**Serial Data Rate = 4Mbps Maximum**
48-Pin Plastic DIP 52-Pin PLCC	SCN26562C2N48 SCN26562C2A52	SCN26562C4N48 SCN26562C4A52

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A1–A6	4–2, 47–45	4–2, 51–49	I	Address lines.
D0–D7	31–28, 21–18	33–30, 23–20	I/O	Bidirectional data bus.
RDN	22	24	I	Read strobe.
WRN	26	28	I	Write strobe.
CEN	25	27	I	Chip select.
RDYN	7	8	O	Ready.
IRQN	6	6	O	Interrupt request.
IACKN	1	1	I	Interrupt acknowledge.
X1/CLK	43	47	I	Crystal 1 or external clock.
X2	42	46	I	Crystal 2.
RESETN	23	25	I	Master reset.
RxDA, RxDB	37, 12	40, 14	I	Channel A (B) receiver serial data.
TxDA, TxDB	36, 13	39, 15	O	Channel A (B) transmitter serial data.
RTxCA, RTxCB	39, 10	43, 11	I/O	Channel A (B) receiver/transmitter clock.
TRxCA, TRxCB	40, 9	44, 10	I/O	Channel A (B) transmitter/receiver clock.
CTSA/BN, LCA/BN	32, 17	35, 19	I/O	Channel A (B) clear-to-send input or loop control output.
DCDA/BN, SYNIA/BN	38, 11	42, 12	I	Channel A (B) data carrier detected or external sync.
RTxDRQA/BN, GPO1A/BN	34, 15	37, 17	O	Channel A (B) receiver/transmitter DMA service request or general purpose output.
TxDRQA/BN, GPO2A/BN, RTSA/BN	33, 16	36, 18	O	Channel A (B) transmitter DMA service request, general purpose output or request-to-send.
RTxDAKA/BN, GPI1A/BN	44, 5	48, 5	I	Channel A (B) receiver/transmitter DMA acknowledge or general purpose input 1.
TxDAKA/BN, GPI2A/BN	35, 14	38, 16	I	Channel A (B) transmitter DMA acknowledge or general purpose input 2.
EOPN	27	29	I/O	DMA transfer complete.
RTSA/BN, SYNOUTA/BN	41, 8	45, 9	O	Channel A (B) request-to-send or Sync detect.
V_{CC}	48	52	I	Power input.
GND	24	26	I	Signal and power ground.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature[2]	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	–0.5 to +7.0	V
V_S	Voltage from any pin to ground[3]	–0.5 to V_{CC} +0.5	V

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 36°C/W junction to ambient for ceramic DIP, 40°C/W for plastic DIP, and 42°C/W for PLCC.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

DC ELECTRICAL CHARACTERISTICS[1, 3] T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage:					
	All except X1/CLK				0.8	V
	X1/CLK				0.4	V
V_{IH}	Input high voltage:					
	All except X1/CLK		2.0			V
	X1/CLK		2.4		V_{CC}	V
V_{OL}	Output low voltage:					
	All except IRQN	I_{OL} = 5.3mA			0.5	V
	IRQN	I_{OL} = 8.8mA			0.5	V
V_{OH}	Output high voltage:					
	(Except open drain outputs)	I_{OH} = –400µA	2.4			V
I_{ILX1}	X1/CLK input low current[3]	V_{IN} = 0, X2 = GND	–5.5		0.0	mA
I_{IHX1}	X1/CLK input high current[3]	V_{IN} = V_{CC}, X2 = GND			1.0	mA
I_{ILX2}	X2 input low current[3]	V_{IN} = 0, X1 = open	–100			µA
I_{IHX2}	X2 input high current[3]	V_{IN} = V_{CC}, X1 = open			100	µA
I_{IL}	Input low current RESETN, TxDAKN, RxDAKN	V_{IN} = 0	–40			µA
I_I	Input leakage current	V_{IN} = 0 to V_{CC}	–5		5	µA
I_{OZH}	Output off current high, 3-State data bus	V_{IN} = V_{CC}			5	µA
I_{OZL}	Output off current low, 3-State data bus	V_{IN} = 0	–5			µA
I_{ODL}	Open drain output low current in off state: EOPN	V_{IN} = 0	–120		–25	µA
	IRQN, RDYN		–5			µA
I_{ODH}	Open drain output high current in off state: EOPN, IRQN, RDYN	V_{IN} = V_{CC}			5	µA
I_{CC}	Power supply current	V_O = 0 to V_{CC}			275	mA
C_{IN}	Input capacitance[2]	V_{CC} = GND = 0			10	pF
C_{OUT}	Output capacitance[2]	V_{CC} = GND = 0			15	pF
$C_{I/O}$	Input/output capacitance[2]	V_{CC} = GND = 0			20	pF

NOTES:
1. Parameters are valid over specified temperature range.
2. These values were not explicitly tested; they are guaranteed by design and characterization data.
3. X1/CLK and X2 are not tested with a crystal installed.

AC ELECTRICAL CHARACTERISTICS[1, 2, 3, 4] T_A = 0°C to +70°C, V_{CC} = 5V ±5%

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{RELREH}	RESETN low to RESETN high	1.2		1.2		µs

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.8V and 2.0V with a transition time of 20ns maximum. For X1/CLK, this swing is between 0.4V and 2.4V. All time measurements are referenced at input voltages of 0.4V and 2.4V and output voltages of 1.2V and 2.0V, as appropriate.
3. See Figure 17 for test conditions for outputs.
4. Tests for open drain outputs are intended to guarantee switching of the output transistor. Measurement of this response is referenced from midpoint of the switching signal to a point 0.2V above the actual output signal level. This point represents noise margin that assures true switching has occurred.

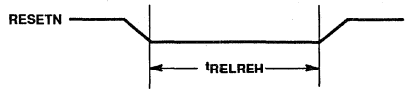
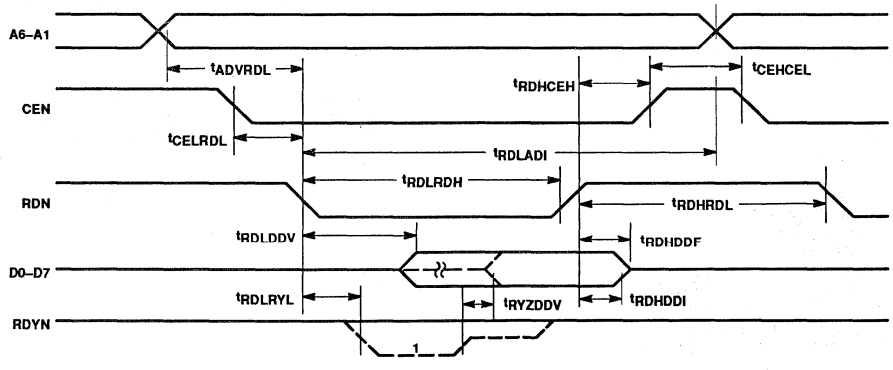


Figure 1. Reset Timing

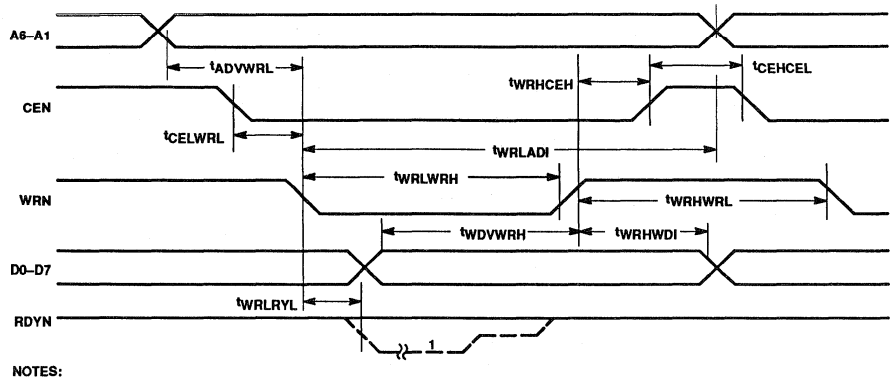


NOTES:
1. Wait on Rx. Receiver FIFO empty.
2. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.

Figure 2. Read Cycle

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{ADVRDL}	Address valid to RDN low	10		10		ns
t_{CELRDL}	CEN low to RDN low	0		0		ns
t_{RDLADI}	RDN low to address invalid	150		150		ns
t_{RDLRYL}	RDN low to RDYN low		275		275	ns
t_{RDLDDV}	RDN low to read data valid		280		300	ns
t_{RDLRDH}	RDN low to RDN high	300		310		ns
t_{RYZDDV}	RDYN high impedance to read data valid		100		100	ns
t_{RDHCEH}	RDN high to CEN high	0		0		ns
t_{CEHCEL}	CEN high to CEN low	160		170		ns
t_{RDHDDI}	RDN high to read data invalid	10		10		ns
t_{RDHRDL}	RDN high to RDN low	160		170		ns
t_{RDHDDF}	RDN high to data bus floating		75		75	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

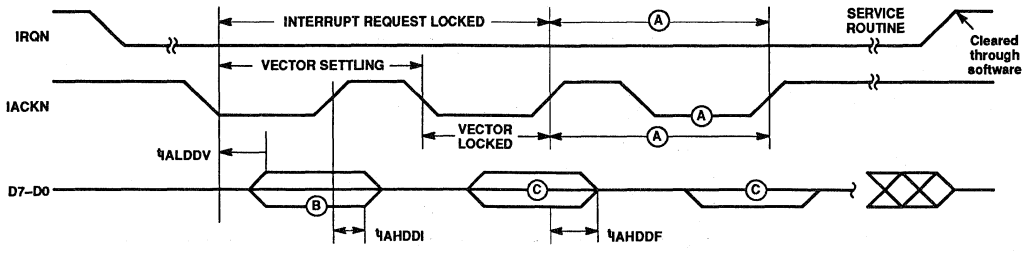


NOTES:
1. Wait on Tx. Transmitter FIFO full.
2. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.

Figure 3. Write Cycle

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{ADVWRL}	Address valid to WRN low	10		10		ns
t_{CELWRL}	CEN low to WRN low	0		0		ns
t_{WRLRYL}	WRN low to READY low		275		275	ns
t_{WRHCEH}	WRN high to CEN high	0		0		ns
t_{WRLWRH}	WRN low to WRN high	300		310		ns
t_{WDVWRH}	Write data valid to WRN high	100		100		ns
t_{CEHCEL}	CEN high to CEN low	160		170		ns
t_{WRLADI}	WRN low to address invalid	150		150		ns
t_{WRHWRL}	WRN high to WRN low	160		170		ns
t_{WRHWDI}	WRN high to write data invalid	10		10		ns

AC ELECTRICAL CHARACTERISTICS (Continued)



NOTES:
(A) ICR[5:4] = 01 or 10 (mode 1 or mode 2)
(B) Call instruction (mode 2)
(C) ICR[5:4] = 11 (mode 3)

Figure 4. Interrupt Acknowledge Cycle

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{IALDDV}	IACKN low to data bus valid		280		280	ns
t_{IAHDDF}	IACKN high to data bus floating		150		150	ns
t_{IAHDDI}	IACKN high to data bus invalid	10		10		ns

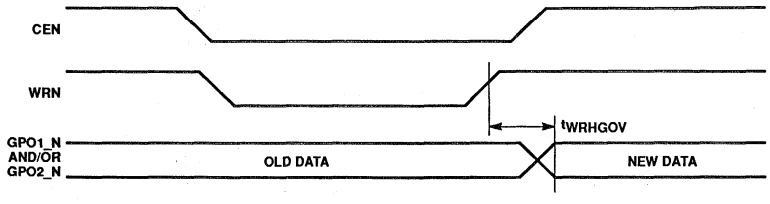


Figure 5. Output Port Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{WRHGOV}	WRN high to GPO output data valid		300		300	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

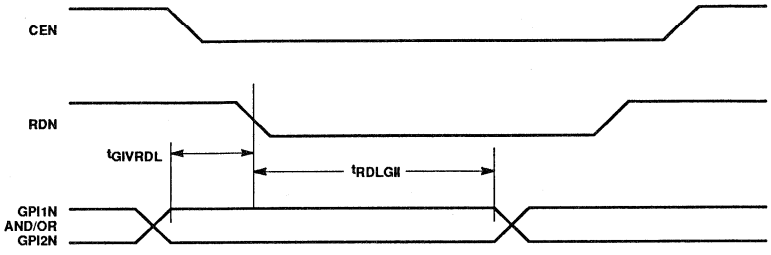


Figure 6. Input Port Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{GIVRDL}	GPI input valid to RDN low	20		20		ns
t_{RDLGII}	RDN low to GPI input invalid	100		100		ns

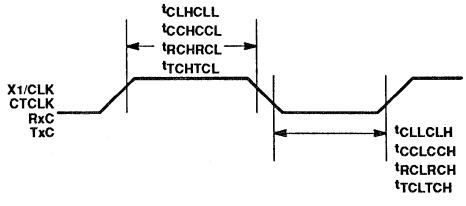


Figure 7. Clock Timing

SYMBOL	PARAMETER	LIMITS						UNIT
		SCN26562C4			SCN26562C2			
		Min	Typ	Max	Min	Typ	Max	
t_{CLHCLL}	X1/CLK high to low time	25			25			ns
t_{CLLCLH}	X1/CLK low to high time	25			25			ns
t_{CCHCCL}	C/T CLK high to low time	100			100			ns
t_{CCLCCH}	C/T CLK low to high time	100			100			ns
t_{RCHRCL}	RxC high to low time	110			150			ns
t_{RCLRCH}	RxC low to high time	110			150			ns
t_{TCHTCL}	TxC high to low time	110			150			ns
t_{TCLTCH}	TxC low to high time	110			150			ns
f_{CL}	X1/CLK frequency	2.0	14.7456	16.0	2.0	14.7456	16.0	MHz
f_{CC}	C/T CLK frequency	0		4.0	0		4.0	MHz
f_{RC}	RxC frequency (16X or 1X)	0		4.0	0		2.5	MHz
f_{TC}	TxC frequency (16X or 1X)	0		4.0	0		2.5	MHz

AC ELECTRICAL CHARACTERISTICS (Continued)

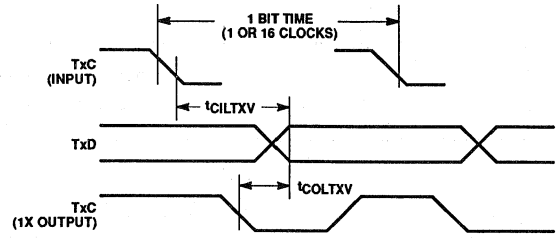


Figure 8. Transmit Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{CILTXV}	TxC input low (1X) to TxD output		240		240	ns
	TxC input low (16X) to TxD output		435		435	ns
t_{COLTXV}	TxC output low to TxD output		50		50	ns

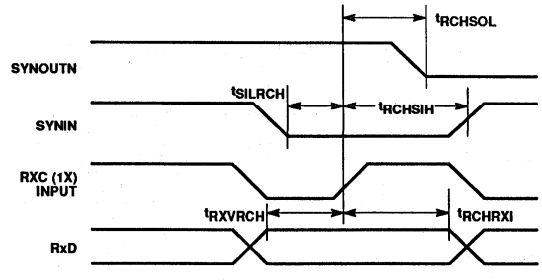


Figure 9. Receive Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{RXVRCH}	RxD data valid to RxC high:					
	For NRZ data	50		50		ns
t_{RCHRXI}	For NRZI, Manchester, FM0, FM1 data	120		130		ns
	RxC high to RxD data invalid:					
	For NRZ data	50		50		ns
	For NRZI, Manchester, FM0, FM1 data	10		10		ns
t_{SILRCH}	SYNIN low to RxC high	100		100		ns
t_{RCHSIH}	RxC high to SYNIN high	50		50		ns
t_{RCHSOL}	RxC high to SYNOUT low		300		300	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

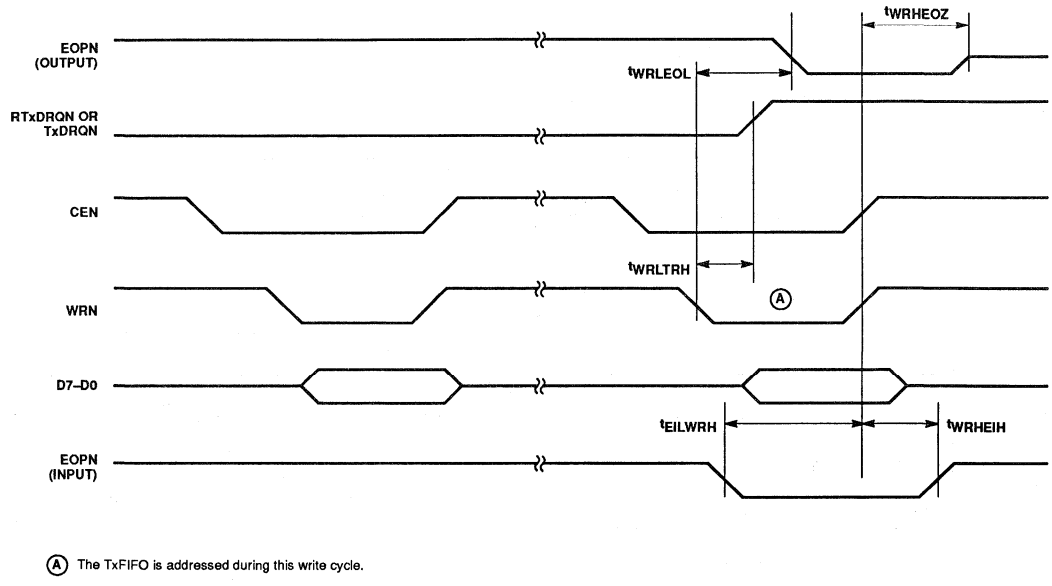
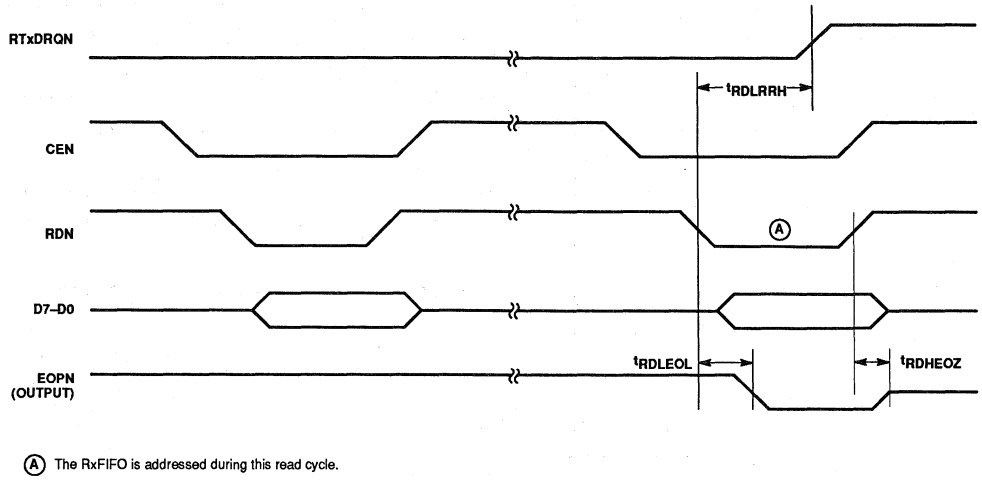


Figure 10. Transmit Dual Address DMA Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{WRLTRH}	WRN low to Tx DMA REQN high		320		320	ns
t_{WRLEOL}	WRN low to EOPN output low		225		225	ns
t_{WRHEOZ}	WRN high to EOPN output high impedance		225		225	ns
t_{EILWRH}	EOPN input low to WRN high	50		50		ns
t_{WRHEIH}	WRN high to EOPN input high	50		50		ns

AC ELECTRICAL CHARACTERISTICS (Continued)

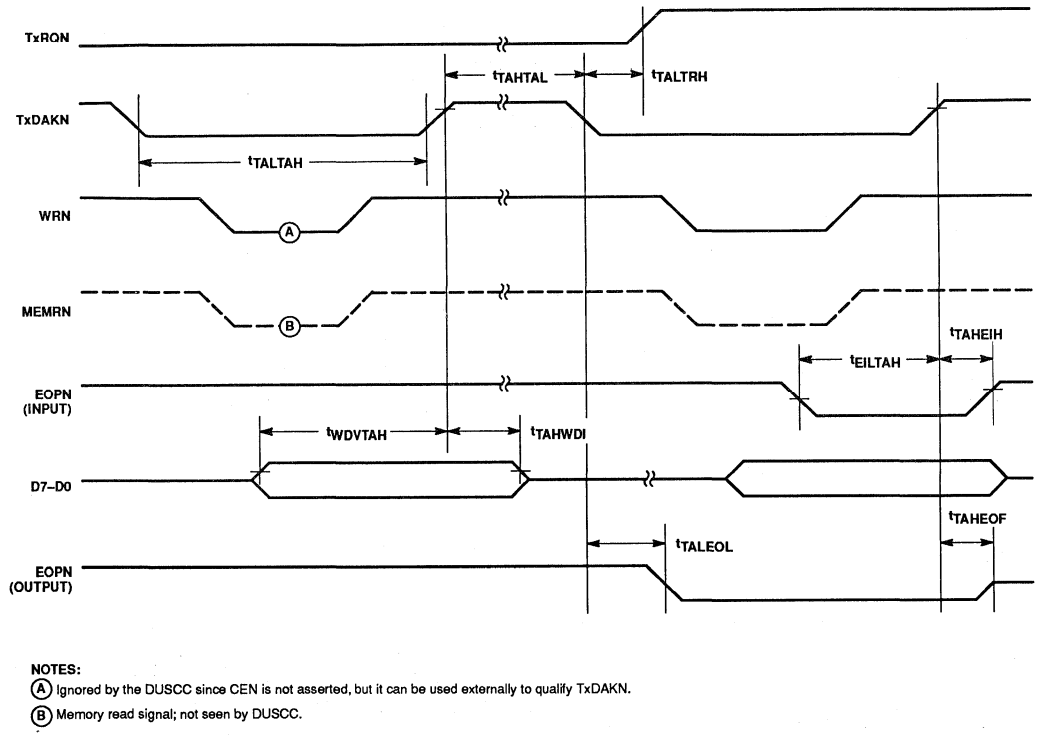


(A) The RxFIFO is addressed during this read cycle.

Figure 11. Receive Dual Address DMA Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{RDLRRH}	RDN low to Rx DMA REQN high		320		320	ns
t_{RDLEOL}	RDN low to EOPN output low		300		300	ns
t_{RDHEOZ}	RDN high to EOPN output high impedance		225		225	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

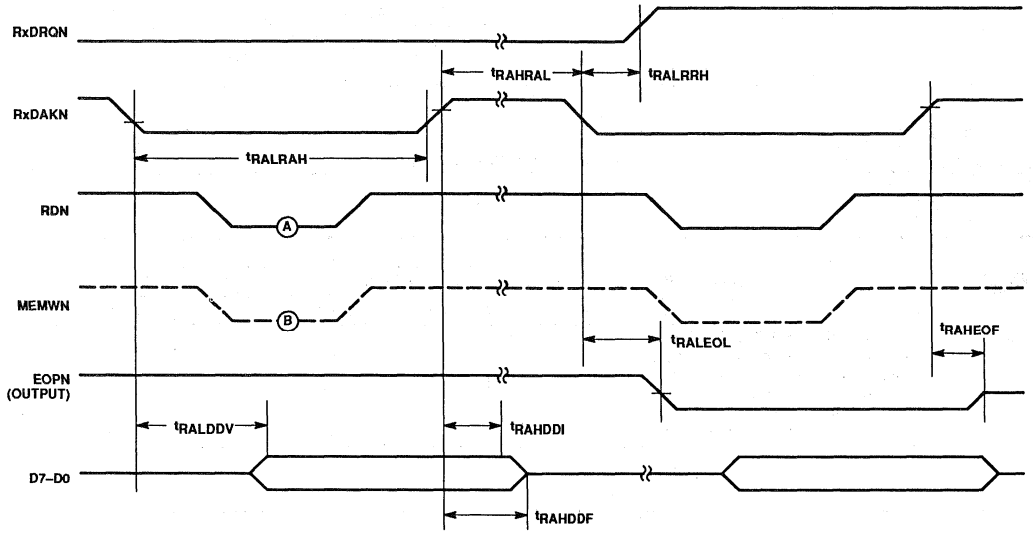


NOTES:
(A) Ignored by the DUSCC since CEN is not asserted, but it can be used externally to qualify TxDAKN.
(B) Memory read signal; not seen by DUSCC.

Figure 12. DMA-Transmit Single Address Mode

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{TAHTAL}	Transmit DMA ACKN high to low time	100		100		ns
t_{TALTAH}	Transmit DMA ACKN low to high time	250		250		ns
t_{TALTRH}	Tx DMA ACKN low to Tx DMA REQN high		250		250	ns
t_{WDVTAH}	Write data valid to Tx DMA ACKN high	90		90		ns
t_{TAHWDI}	Tx DMA ACKN high to write data invalid	30		30		ns
t_{TALEOL}	Tx DMA ACKN low to EOPN output low		170		170	ns
t_{TAHEOF}	Tx DMA ACKN high to EOPN output float		200		200	ns
t_{EILTAH}	EOPN input low to Tx DMA ACKN high	50		50		ns
t_{TAHEIH}	Tx DMA ACKN high to EOPN input high	50		50		ns

AC ELECTRICAL CHARACTERISTICS (Continued)



NOTES:
(A) Ignored by the DUSCC bit; it can be used to qualify RxDAKN.
(B) Memory read signal; not seen by DUSCC.

Figure 13. DMA-Receive Single Address Mode

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{RAHRAL}	Receive DMA ACKN high to low time	160		160		ns
t_{RALRAH}	Receive DMA ACKN low to high time	250		250		ns
t_{RALRRH}	Rx DMA ACKN low to Rx DMA REQN high		320		320	ns
t_{RALEOL}	Rx DMA ACKN low to EOPN output low		200		200	ns
t_{RAHEOF}	Rx DMA ACKN high to EOPN output float		225		225	ns
t_{RALDDV}	Rx DMA ACKN low to read data valid		225		225	ns
t_{RAHDDI}	Rx DMA ACKN high to read data invalid	10		10		ns
t_{RAHDDF}	Rx DMA ACKN high to data bus float		125		125	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

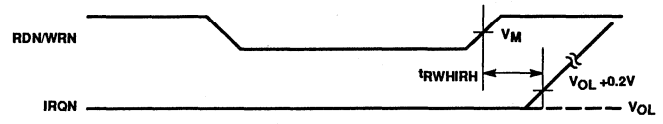


Figure 14. Interrupt Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{RWHIRH}	RDN/WRN high to IRQN high for:					
	Read RxFIFO (RxRDY interrupt)		450		450	ns
	Write TxFIFO (TxRDY interrupt)		450		450	ns
	Write RSR (Rx condition interrupt)		400		400	ns
	Write TRSR (Rx/Tx interrupt)		400		400	ns
	Write ICTSR (counter/timer interrupt)		400		400	ns

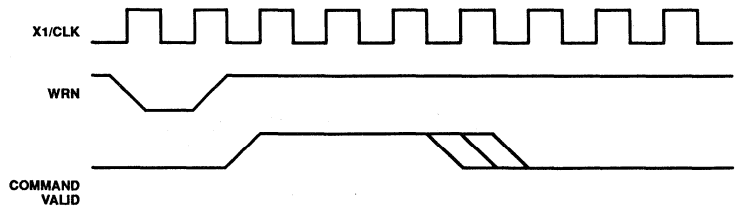


Figure 15. Command Timing

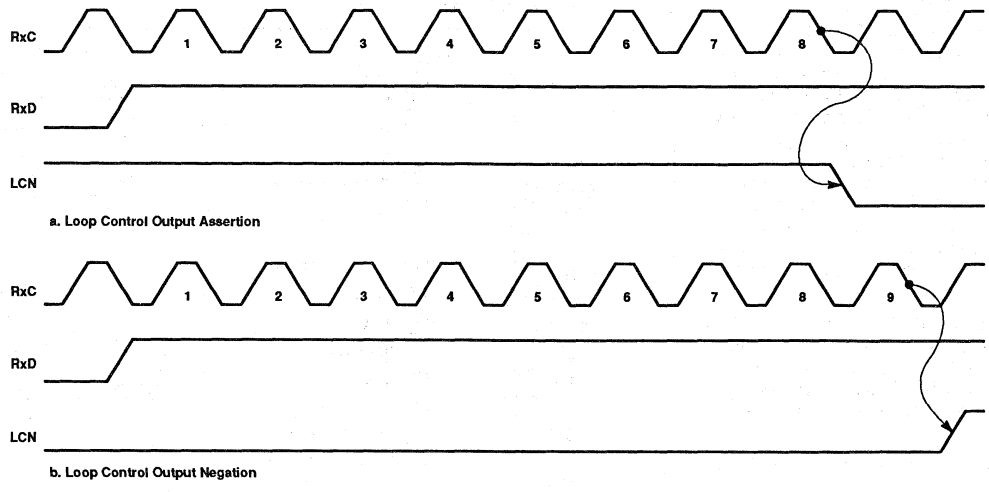
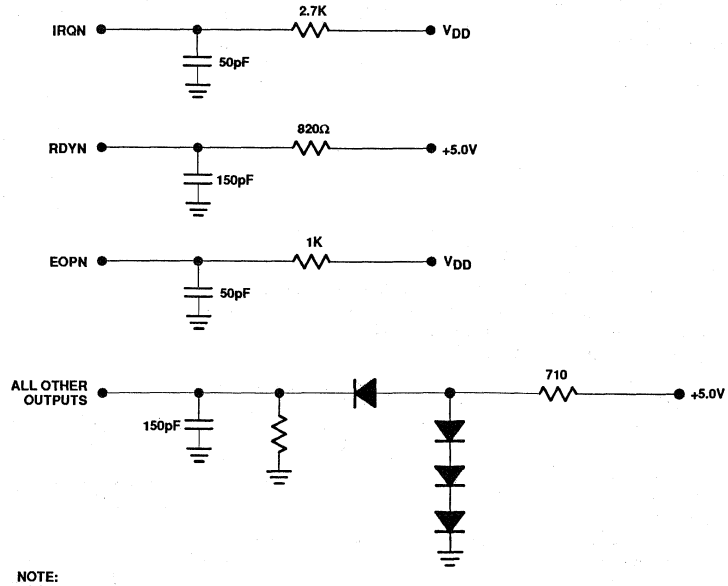


Figure 15. Relationship Between Received Data and the Loop Control Output



NOTE:
All C_L includes 50pF stray capacitance,
i.e., C_L = 150pF = 100pF discrete +50pF stray.

Figure 16. Test Conditions for Outputs

CMOS dual universal serial communications controller (CDUSCC) SC26C562

DESCRIPTION

The Signetics SC26C562 Dual Universal Serial Communications Controller (CDUSCC) is a single-chip CMOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SC26C562 interfaces to synchronous bus MPUs and is capable of program-polled, interrupt driven, block-move or DMA data transfers.

The SC26C562 (CDUSCC) is (PIN) hardware and (REGISTER) software comaptible with the existing SCN26562 (DUSCC). CDUSCC will automatically configure to the NMOS DUSCC register map (default mode) on power up.

The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides sixteen common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock, making the CDUSCC well-suited for dual-speed channel applications. Data rates up to 10Mbits per second are supported.

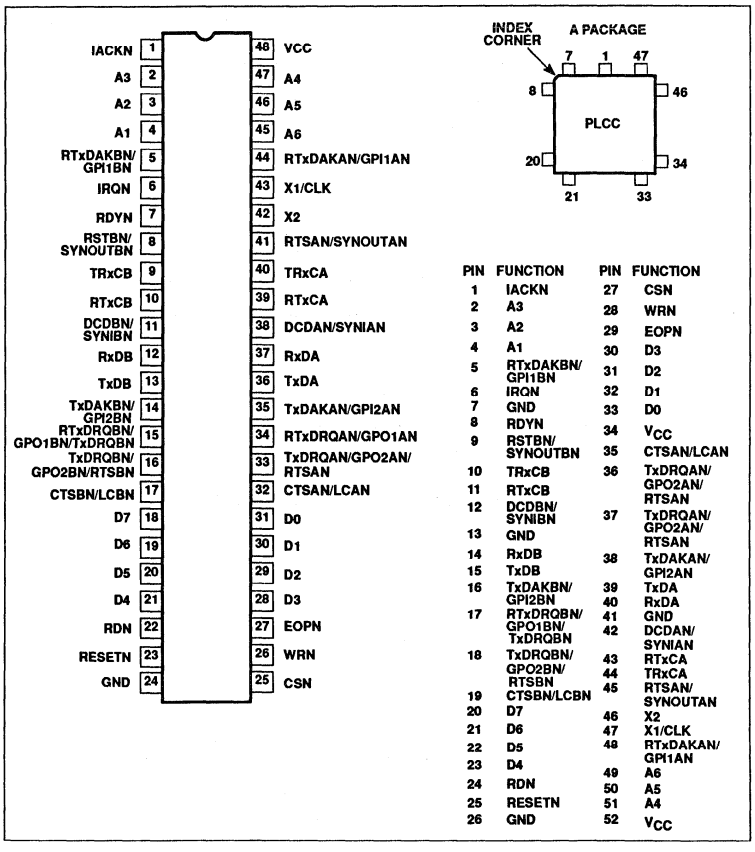
The transmitter and receiver each contain a sixteen-deep FIFO with appended transmitter command and receiver status bits and a shift register. This permits reading and writing of up to sixteen characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs and outputs are general purpose in nature, they can be optionally programmed for other functions.

The SC26C562 CDUSCC is optimized to interface with processors using a synchronous bus interface, such as the 8086, and iAPX86 family. For systems using an asynchronous bus, such as the 68000 and 68010, refer to the SC68C562 documentation.

Refer to the CMOS Dual Universal Serial Communication Controller (CDUSCC) User's Manual for a complete operational description.

PIN CONFIGURATIONS



PIN	FUNCTION	PIN	FUNCTION
1	IACKN	27	CSN
2	A3	28	WRN
3	A2	29	EOPN
4	A1	30	D3
5	RTxDAKBN/ GPI1BN	31	D2
6	IRQN	32	D1
7	GND	33	D0
8	RDYN	34	V_{CC}
9	RSTBN/ SYNOUTBN	35	CTSAN/LCAN
10	TRxCB	36	TxDRQAN/ GPO2AN/ RTSAN
11	RTxCB	37	TxDRQAN/ GPO2AN/ RTSAN
12	DCDBN/ SYNIBN	38	TxDAKAN/ GPI2AN
13	GND	39	TxDA
14	RxDB	40	RxDA
15	TxDB	41	GND
16	TxDAKBN/ GPI2BN	42	DCDAN/ SYNIAN
17	RTxDRQBN/ GPO1BN/ TxDRQBN	43	RTxCA
18	TxDRQBN/ GPO2BN/ RTSBN	44	TRxCA
19	CTSBN/LCBN	45	RTSAN/ SYNOUTAN
20	D7	46	X2
21	D6	47	X1/CLK
22	D5	48	RTxDAKAN/ GPI1AN
23	D4	49	A6
24	RDN	50	A5
25	RESETN	51	A4
26	GND	52	V_{CC}

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±10%, T_A = 0 to +70°C Serial Data Rate = 10Mbps Maximum
48-Pin Plastic DIP	SC26C562C1N
52-Pin PLCC	SC26C562C1A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	-0.5 to +7.0	°C
V_S	Voltage from any pin to ground[3]	-0.5 to V_{CC} +0.5	°C

CMOS dual universal serial communications controller (CDUSCC) SC26C562

FEATURES

General Features

- Dual full-duplex synchronous/ asynchronous receiver and transmitter
- Multi-protocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
  - COP: Single SYNC, dual SYNC, BiSYNC, DDCMP
  - ASYNC: 5-8 bits plus optional parity
- Sixteen character receive and transmit FIFOs with interrupt threshold control
- FIFO'ed status bits
- Watchdog timer
- 0 to 10 Mbit/sec data rate
- Programmable bit rate for each receiver and transmitter selectable from:
  - 19 fixed rates: 50 to 64K baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
  - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- or half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Compatible with Synchronous and Asynchronous bus DMA controllers
  - Half- or full-duplex operation
  - Single or dual address data transfers
  - Automatic frame termination on counter/ timer terminal count or DMA DONE (EOPN)
- Transmit path clear status
- High speed data bus interface: 160ns bus cycle
- DPLL operation up to 312.5kHz with internal clock
- Interrupt capabilities
  - Vector output (fixed or modified by status)
  - Individual interrupt enable bits
  - Programmable internal priorities
  - Maskable interrupt conditions
  - 80XX/X compatible
- Multi-function programmable 16-bit counter/timer
  - Bit rate generator
  - Event counter
  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general purpose I/O pins per channel
  - CTS and DCD programmable auto-enables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- 1X or 16X Rx and Tx clock factors
- Parity, overrun and framing error detection
- False start bit detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmit and receive up to 10Mbps at 1x or 1Mbps at 16x data rates

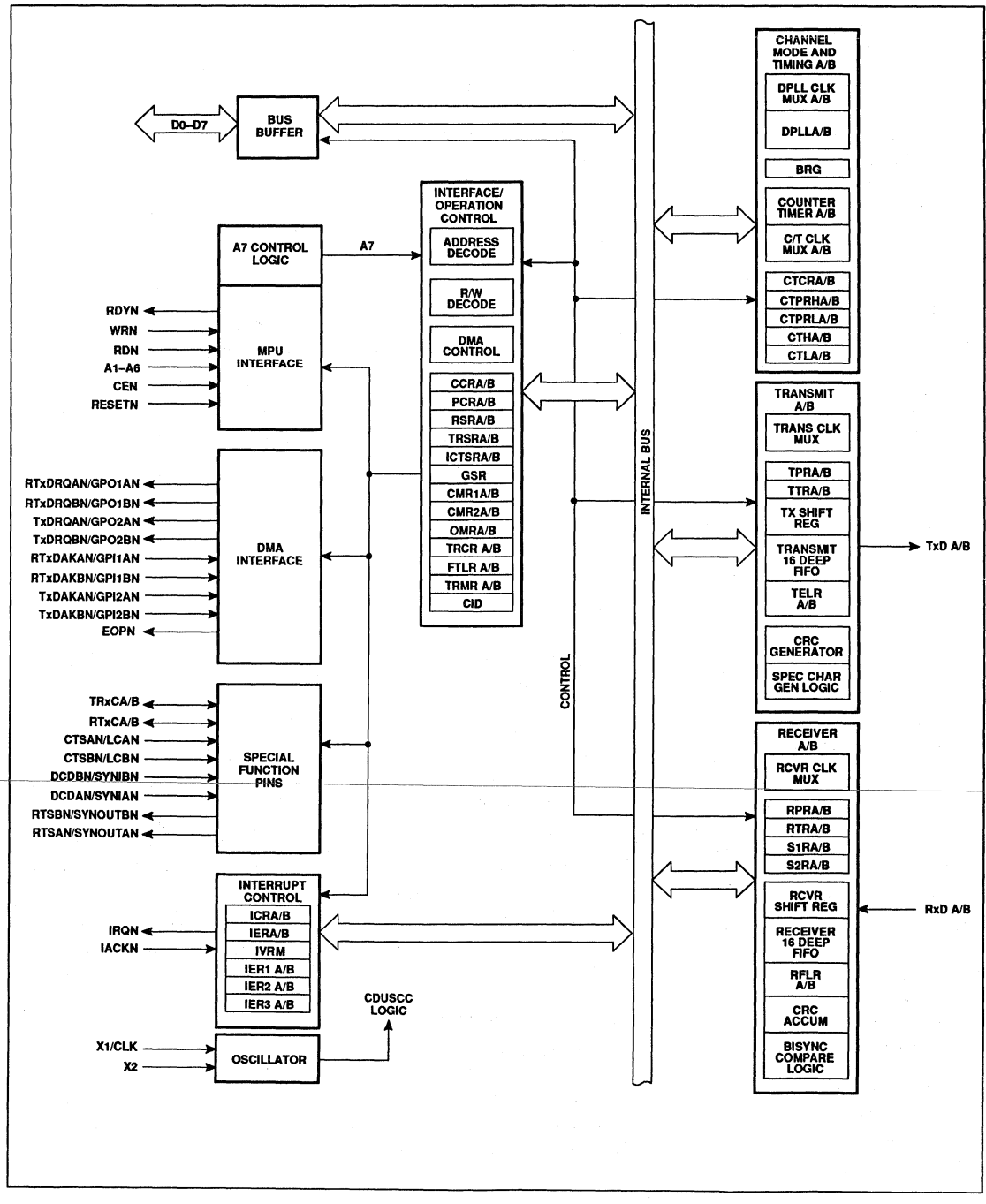
Bit-Oriented Protocol

- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Automatic switch to programmed character length for I field
- Zero insertion and deletion
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Transmit 7 or 8 bit ABORT
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

Character-Oriented Protocols

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK linefill or underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun and underrun error detection
- Optional SYNC exclusion from FCS
- BISYNC features
  - EBCDIC or ASCII header, text and control messages
  - SYN, DLE stripping
  - EOM (end of message) detection and transmission
  - Auto transparency mode switching
  - Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
  - Control character sequence detection for both transparent and normal text
  - Parity generation for data and LRC characters

BLOCK DIAGRAM — SC26C562



PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A1–A6	4-2, 47-45	4-2, 51-49	I	**Address Lines:** Active-high. Address inputs which specify which of the internal registers is accessed for read/write operation.
D0–D7	31-28, 21-18	33-30, 23-20	I/O	**Bidirectional Data Bus:** Active-high, 3-State. Bit 0 is the LSB and bit 7 is the MSB. All data, command and status transfers between the CPU and the CDUSCC take place over this bus. The data bus is enabled when CSN and RDN, or CSN and WRRN are low during interrupt acknowledge cycles and single address DMA acknowledge cycles.
RDN	22	24	I	**Read Strobe:** Active-low input. When active and CSN is also active, causes the content of the addressed register to be present on the data bus. RDN is ignored unless CSN is active.
WRN	26	28	I	**Write Strobe:** Active-low input. When active and CSN is also active, the content of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of WRN. WRN is ignored unless CEN is active.
CSN	25	27	I	**Chip Select:** Active-low input. When active, data transfers between the CPU and the CDUSCC are enabled on D0–D7 as controlled by RDN or WRN and A1–A6 inputs. When CSN is high, the data lines are placed in the 3-State condition (except during interrupt acknowledge cycles and single address DMA transfers).
RDYN	7	8	O	**Ready:** Active-low, open drain. Used to synchronize data transfers between the CPU and the CDUSCC. It is valid only during read and write cycles where the CDUSCC is configured in 'wait on Rx', 'wait on Tx' or 'wait on Tx or Rx' modes, otherwise it is always inactive. RDYN becomes active on the leading edge of RDN and WRN if the requested operation cannot be performed (viz, no data in RxFIFO in the case of a read or no room in the TxFIFO in the case of a write).
IRQN	6	6	O	**Interrupt Request:** Active-low, open-drain. This output is asserted upon occurrence of any enabled interrupting condition. The CPU can read the general status register to determine the interrupting condition(s), or can respond with an interrupt acknowledge cycle to cause the CDUSCC to output an interrupt vector on the data bus.
IACKN	1	1	I	**Interrupt Acknowledge:** Active-low. When IACKN is asserted, the CDUSCC responds by either forcing the bus into high-impedance, placing a vector number, call instruction or zero on the data bus. The vector number can be modified or unmodified by the status. If no interrupt is pending, IACKN is ignored and the data bus placed in high-impedance.
X1/CLK	43	47	I	**Crystal or External Clock:** When using the crystal oscillator, the crystal is connected between pins X1 and X2. If a crystal is not used, an external clock is supplied at this input. This clock is used to drive the internal bit rate generator, as an optional input to the counter/timer or DPLL, and to provide other required clocking signals. When a crystal is used, a capacitor must be connected from this pin to ground.
X2	42	46	O	**Crystal 2:** Connection for other side of crystal. When a crystal is used, a capacitor must be connected from this pin to ground. If an external clock is used on X1, this pin should be left floating.
RESETN	23	25	I	**Master Reset:** Active-low. A low on this pin resets the transmitters and receivers and resets the registers shown in Table 1 of the CDUSCC Users' Guide. Reset is asynchronous, i.e., no clock is required.
RxDA, RxDB	37, 12	40, 14	I	**Channel A (B) Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified for the channel, the input is sampled on the rising edge of the clock.
TxDA, TxDB	36, 13	39, 15	O	**Channel A (B) Transmitter Serial Data Output:** The least signifiicant bit is transmitted first. This output is in the marking (high) condition when the transmitter is disabled or when the channel is operating in local loopback mode. If external transmitter clock is specified for the channel, the data is shifted on the falling edge of the clock.
RTxCA, RTxCB	39, 10	43, 11	I/O	**Channel A (B) Receiver/Transmitter Clock:** As an input, it can be programmed to supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the transmitter shift clock (1X), or the receiver sampling clock (1X).
TRxCA, TRxCB	40, 9	44, 10	I/O	**Channel A (B) Transmitter/Receiver Clock:** As an input, it can supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the DPLL output, the transmitter shift clock (1X), the receiver sampling clock (1X), the transmitter BRG clock (16X), The receiver BRG clock (16X), or the internal system clock (X1 ÷ 2).

PIN DESCRIPTION (Continued)

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
CTSA/BN, LCA/BN	32, 17	35, 19	I/O	**Channel A (B) Clear-to-Send Input or Loop Control Output:** Active-low. The signal can be programmed to act as an enable for the transmitter when not in loop mode. The CDUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. When operating in the BOP loop mode, this pin becomes a loop control output which is asserted and negated by CDUSCC commands. This output provides the means of controlling external loop interface hardware to go on-line and off-line without disturbing operation of the loop.
DCDA/BN, SYNIA/BN	38, 11	42, 12	I	**Channel A (B) Data Carrier Detected or External Sync Input:** The function of this pin is programmable. As a DCD active-low input, it acts as an enable for the receiver or can be used as a general purpose input. For the DCD function, the CDUSCC detects logic level transitions on this pin and can be programmed to generate an interrupt when a transition occurs. As an active-low external sync input, it is used in COP mode to obtain character synchronization for the receiver without receipt of a SYN character. This mode can be used in disc or tape controller applications or for the optional byte timing lead in X.21.
RTxDRQA/BN, GPO1A/BN	34, 15	37, 17	O	**Channel A (B) Receiver/Transmitter DMA Service Request or General Purpose Output:** Active-low. For half-duplex DMA operation, this output indicates to the DMA controller that one or more characters are available in the receiver FIFO (when the receiver is enabled) or that the transmit FIFO is not full (when the transmitter is enabled). For full-duplex DMA operation, this output indicates to the DMA controller that data is available in the receiver FIFO. In non-DMA mode, this pin is a general purpose output that can be asserted and negated under program control.
TxDRQA/BN, GPO2A/BN, RTSA/BN	33, 16	36, 18	O	**Channel A (B) Transmitter DMA Service Request, General Purpose Output, or Request-to-Send:** Active-low. For full-duplex DMA operation, this output indicates to the DMA controller that the transmit FIFO is not full and can accept more data. When not in full-duplex DMA mode, this pin can be programmed as a general purpose or a Request-to-Send output, which can be asserted and negated under program control.
RTxDAKA/BN, GPI1A/BN	44, 5	48, 5	I	**Channel A (B) Receiver/Transmitter DMA Acknowledge or General Purpose Input:** Active-low. For half-duplex single address operation, this input indicates to the CDUSCC that the DMA controller has acquired the bus and that the requested bus cycle (read receiver FIFO when the receiver is enabled or load transmitter FIFO when the transmitter is enabled) is beginning. For full-duplex single address DMA operation, this input indicates to the CDUSCC that the DMA controller has acquired the bus and that the requested read receiver FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in single address DMA mode.
TxDAKA/BN, GPI2A/BN	35, 14	38, 16	I	**Channel A (B) Transmitter DMA Acknowledge or General Purpose Input:** Active-low. When the channel is programmed for full-duplex single address DMA operation, this input is asserted to indicate to the CDUSCC that the DMA controller has acquired the bus and that the requested load transmitter FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in full-duplex single address DMA mode.
EOPN	27	29	I/O	**Done (EOP):** Active-low, open-drain. EOPN can be used and is active in both DMA and non-DMA modes. As an input, EOPN indicates the last DMA transfer cycle to the TxFIFO. As an output, EOPN indicates either the last DMA transfer from the RxFIFO or that the transmitted character count has reached terminal count.
RTSA/BN, SYNOUTA/BN	41, 8	45, 9	O	**Channel A (B) Sync Detect or Request-to-Send:** Active-low. If programmed as a sync output, it is asserted one bit time after the specified sync character (COP or BISYNC modes) or a FLAG (BOP modes) is detected by the receiver. As a Request-to-Send modem control signal, it functions as described previously for the TxDRQN/RTSN pin.
V_{CC}	48	34, 52	I	**+5V Power Input**
GND	24	26, 13, 41, 7	I	**Signal and Power Ground Input**

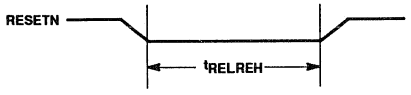
DC ELECTRICAL CHARACTERISTICS[4,5] T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%[4,5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage:					
	All except X1/CLK				0.8	V
	X1/CLK				0.4	V
V_{IH}	Input high voltage:					
	All except X1/CLK		2.0			V
	X1/CLK		0.8		V_{CC}	V
V_{OL}	Output low voltage:					
	All except IRQN[7]	I_{OL} = 5.3mA			0.5	V
	IRQN	I_{OL} = 8.8mA			0.5	V
V_{OH}	Output high voltage:					
	(Except open drain outputs)	I_{OH} = –400µA	2.4			V
I_{ILX1}	X1/CLK input low current[10]	V_{IN} = 0, X2 = open	–150		0.0	µA
I_{IHX1}	X1/CLK input high current[10]	V_{IN} = V_{CC}, X2 = GND			150	µA
I_{IL}	Input low current RESETN, TxDAKN, RxDAKN	V_{IN} = 0	–40			µA
I_I	Input leakage current	V_{IN} = 0 to V_{CC}	–5		5	µA
I_{OZH}	Output off current high, 3-State data bus	V_{IN} = V_{CC}			5	µA
I_{OZL}	Output off current low, 3-State data bus	V_{IN} = 0	–5			µA
I_{ODL}	Open drain output low current in off state: EOPN	V_{IN} = 0	–120		–25	µA
	IRQN, RDYN		–5			µA
I_{ODH}	Open drain output high current in off state: EOPN, IRQN, RDYN	V_{IN} = V_{CC}			5	µA
I_{CC}	Power supply current	V_O = 0 to V_{CC} Rx and Tx clocks at 14.7MHz X1 clock at 14.7MHz			60	mA
C_{IN}	Input capacitance[9]	V_{CC} = GND = 0			10	pF
C_{OUT}	Output capacitance[9]	V_{CC} = GND = 0			15	pF
$C_{I/O}$	Input/output capacitance[9]	V_{CC} = GND = 0			20	pF

NOTES:

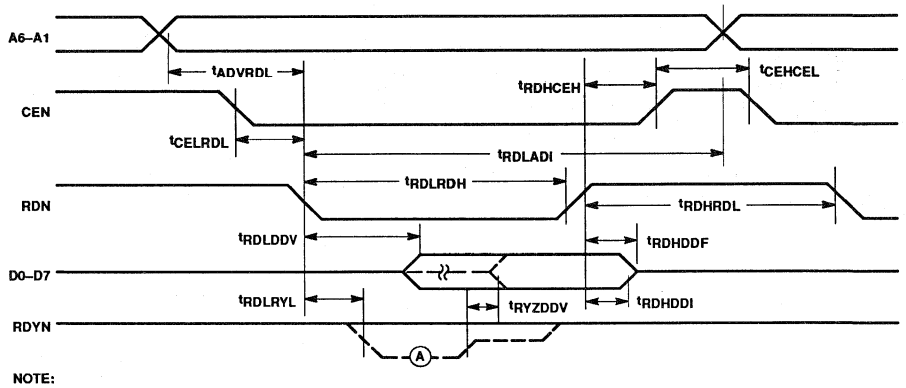
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.
2. Clock may be stopped (DC) for testing purposes, or when CDUSCC is in non-operational modes.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.
5. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK, this swing is between 0.4V and 2.8V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
6. See Figure 17 for test conditions for outputs.
7. Tests for open drain outputs are intended to guarantee switching of the output transistor. Measurement of this response is referenced from midpoint of the switching signal to a point 0.2V above the actual output signal level. This point represents noise margin that assures true switching has occurred.
8. Execution of the valid command (after it is latched) requires 3 rising edges of X1 (see Figure 15).
9. These values were not explicitly tested; they are guaranteed by design and characterization data.
10. X1/CLK and X2 are not tested with a crystal installed.
11. X1/CLK frequency must be at least the faster of the receiver or transmitter serial data rate.
12. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CSN as the 'strobing' input. CSN and RDN (also CSN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.

AC ELECTRICAL CHARACTERISTICS[4,5,6,7] T_A = 0°C to +70°C, V_{CC} = 5V ±10%



1. Reset Timing

SYMBOL	PARAMETER	LIMITS		UNIT
		SC26C562		
		Min	Max	
t_{RELREH}	RESETN low to RESETN high	1.2		µs

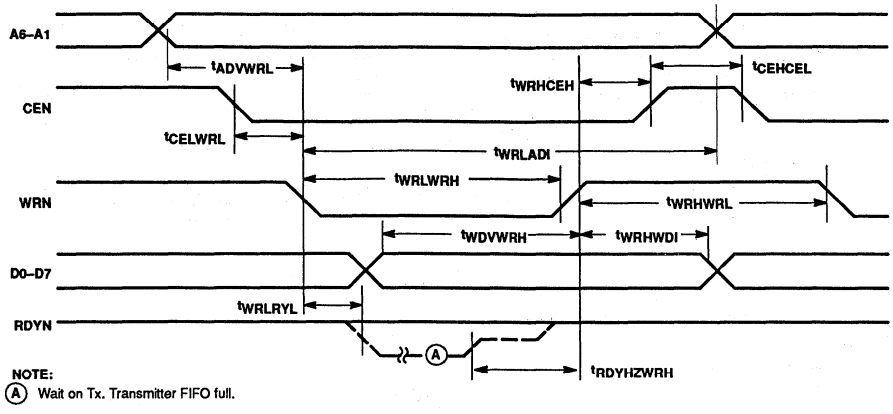


NOTE:
(A) Wait on Rx. Receiver FIFO empty.

2. Read Cycle[12]

SYMBOL	PARAMETER	LIMITS		UNIT
		SC26C562		
		Min	Max	
t_{ADVRDL}	Address valid to RDN low	0		ns
t_{CELRDL}	CEN low to RDN low	0		ns
t_{RDLADI}	RDN low to address invalid	30		ns
t_{RDLRYL}	RDN low to RDYN low		80	ns
t_{RDLDDV}	RDN low to read data valid		110	ns
t_{RDLRDH}	RDN low to RDN high	110		ns
t_{RYZDDV}	RDYN high impedance to read data valid		-10	ns
t_{RDHCEH}	RDN high to CEN high	0		ns
t_{CEHCEL}	CEN high to CEN low	60		ns
t_{RDHDDI}	RDN high to read data invalid	5		ns
t_{RDHRDL}	RDN high to RDN low	60		ns
t_{RDHDDF}	RDN high to data bus floating		40	ns
t_{RDLDLZ}	RDN low to data bus low impedance	20		ns

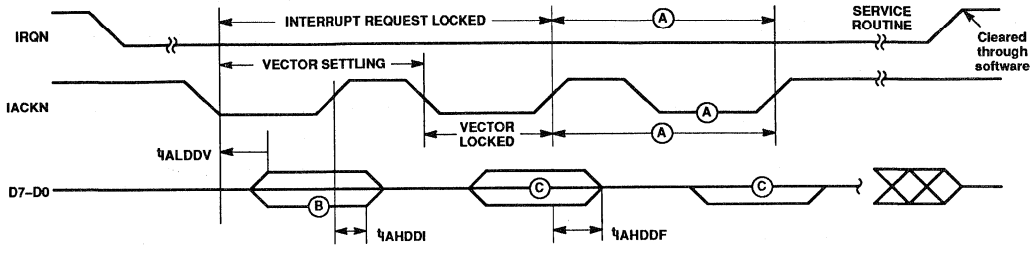
AC ELECTRICAL CHARACTERISTICS (Continued)



3. Write Cycle[12]

SYMBOL	PARAMETER	LIMITS		UNIT
		SC26C562		
		Min	Max	
t_{ADVWRL}	Address valid to WRN low	0		ns
t_{CELWRL}	CSN low to WRN low	0		ns
t_{WRLRYI}	WRN low to READY low		80	ns
t_{WRHCEH}	WRN high to CSN high	0		ns
t_{WRLWRH}	WRN low to WRN high	110		ns
t_{WDVWRH}	Write data valid to WRN high	40		ns
t_{CEHCEL}	CSN high to CSN low[8]	60		ns
t_{WRLADI}	WRN low to address invalid	30		ns
t_{WRHWRL}	WRN high to WRN low	60		ns
t_{WRHWDI}	WRN high to write data invalid[8]	0		ns
$t_{RYHZWRH}$	RDYN hi impedance to WRN high	0		ns

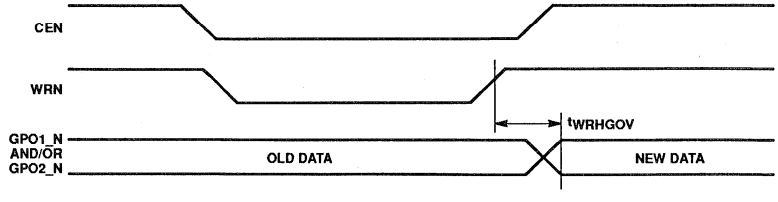
AC ELECTRICAL CHARACTERISTICS (Continued)



NOTES:
(A) ICR[5:4] = 01 or 10 (mode 1 or mode 2)
(B) Call instruction (mode 2)
(C) ICR[5:4] = 11 (mode 3)

4. Interrupt Acknowledge Cycle

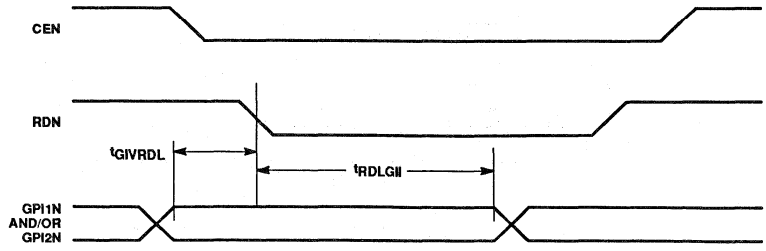
SYMBOL	PARAMETER	LIMITS SC26C562 Min	LIMITS SC26C562 Max	UNIT
t_{IALDDV}	IACKN low to data bus valid		110	ns
t_{IAHDDF}	IACKN high to data bus floating		50	ns
t_{IAHDDI}	IACKN high to data bus invalid	5		ns
t_{IALDLZ}	IACKN low to data bus low impedance	20		ns
t_{IAH}	IACKN high time	60		ns



5. Output Port Timing

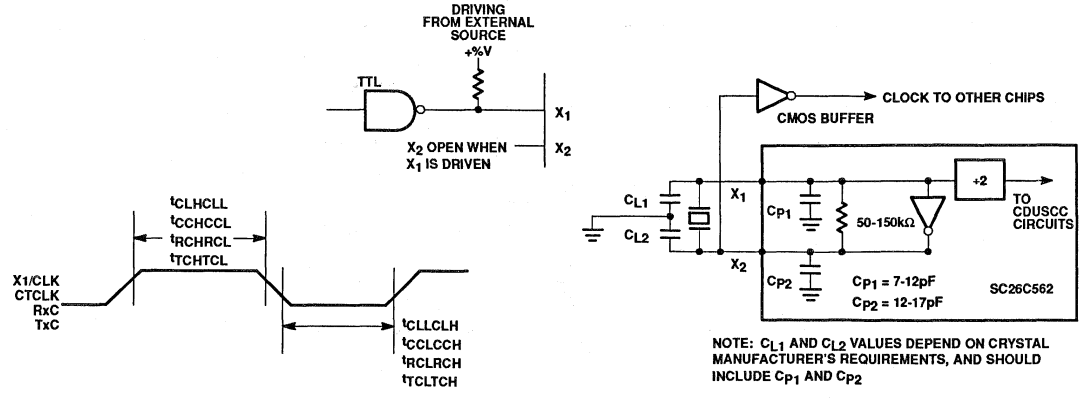
SYMBOL	PARAMETER	LIMITS SC26C562 Min	LIMITS SC26C562 Max	UNIT
t_{WRHGOV}	WRN high to GPO output data valid		100	ns

AC ELECTRICAL CHARACTERISTICS (Continued)



6. Input Port Timing

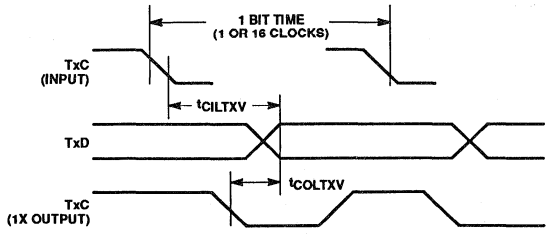
SYMBOL	PARAMETER	LIMITS SC26C562 Min	LIMITS SC26C562 Max	UNIT
t_{GIVRDL}	GPI input valid to RDN low	20		ns
t_{RDLGII}	RDN low to GPI input invalid	50		ns



7. Clock Timing

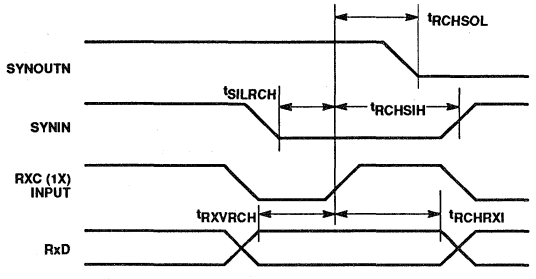
SYMBOL	PARAMETER	LIMITS SC26C562 Min	Typ	Max	UNIT
t_{CLHCLL}	X1/CLK high to low time	25			ns
t_{CLLCLH}	X1/CLK low to high time	25			ns
t_{CCHCCL}	C/T CLK high to low time	40			ns
t_{CCLCCH}	C/T CLK low to high time	40			ns
t_{RCHRCL}	RxC high to low time	40			ns
t_{RCLRCH}	RxC low to high time	40			ns
t_{TCHTCL}	TxC high to low time	40			ns
t_{TCLTCH}	TxC low to high time	40			ns
f_{CL}	X1/CLK frequency[11]	0	14.7456	16.0	MHz
f_{CC}	C/T CLK frequency	0		10	MHz
f_{RC}	RxC frequency (16X or 1X)	0		10	MHz
f_{TC}	TxC frequency (16X or 1X)	0		10	MHz

AC ELECTRICAL CHARACTERISTICS (Continued)



8. Transmit Timing

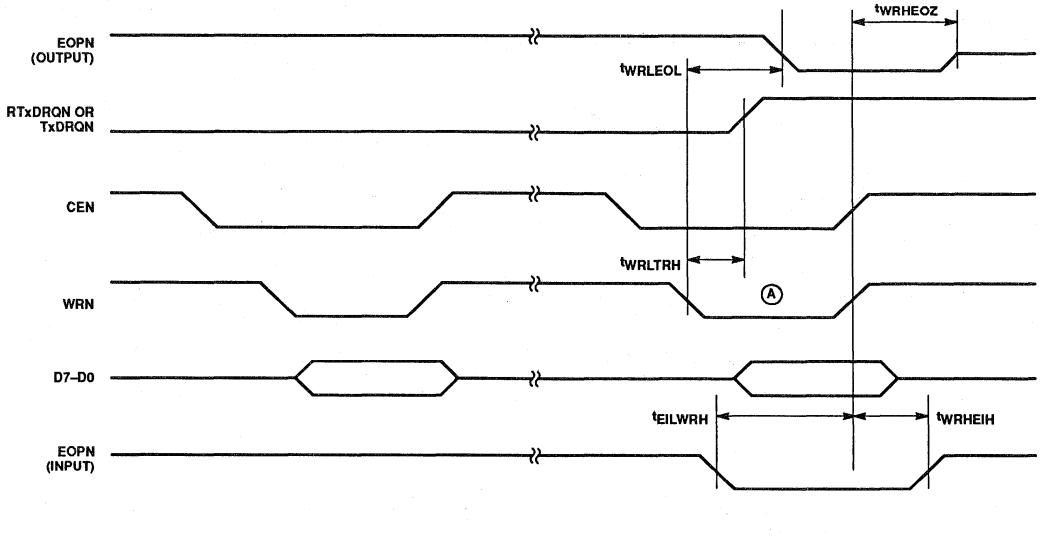
SYMBOL	PARAMETER	LIMITS SC26C562 Min	LIMITS SC26C562 Max	UNIT
t_{CILTXV}	TxC input low (1X) to TxD output		100	ns
	TxC input low (16X) to TxD output		120	ns
t_{COLTXV}	TxC output low to TxD output		50	ns



9. Receive Timing

SYMBOL	PARAMETER	LIMITS SC26C562 Min	LIMITS SC26C562 Max	UNIT
t_{RXVRCH}	RxD data valid to RxC high:			
	For NRZ data	50		ns
t_{RCHRXI}	For NRZI, Manchester, FM0, FM1 data	50		ns
	RxC high to RxD data invalid:			
	For NRZ data	20		ns
	For NRZI, Manchester, FM0, FM1 data	20		ns
t_{SILRCH}	SYNIN low to RxC high	50		ns
t_{RCHSIH}	RxC high to SYNIN high	20		ns
t_{RCHSOL}	RxC high to SYNOUT low		100	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

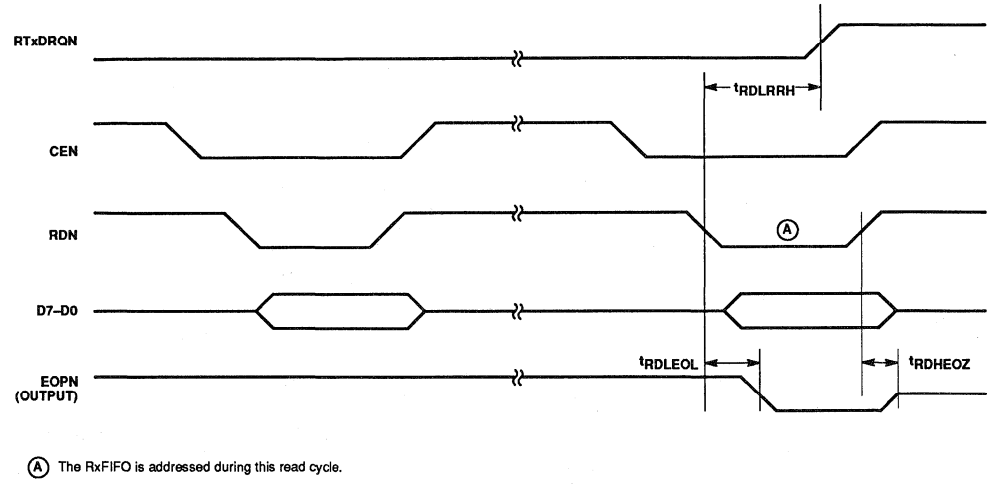


(A) The TxFIFO is addressed during this write cycle.

10. Transmit Dual Address DMA Timing

SYMBOL	PARAMETER	LIMITS		UNIT
		SC26C562		
		Min	Max	
t_{WRLTRH}	WRN low to Tx DMA REQN high		100	ns
t_{WRLEOL}	WRN low to EOPN output low		100	ns
t_{WRHEOZ}	WRN high to EOPN output high impedance		90	ns
t_{EILWRH}	EOPN input low to WRN high	30		ns
t_{WRHEIH}	WRN high to EOPN input high	0		ns

AC ELECTRICAL CHARACTERISTICS (Continued)

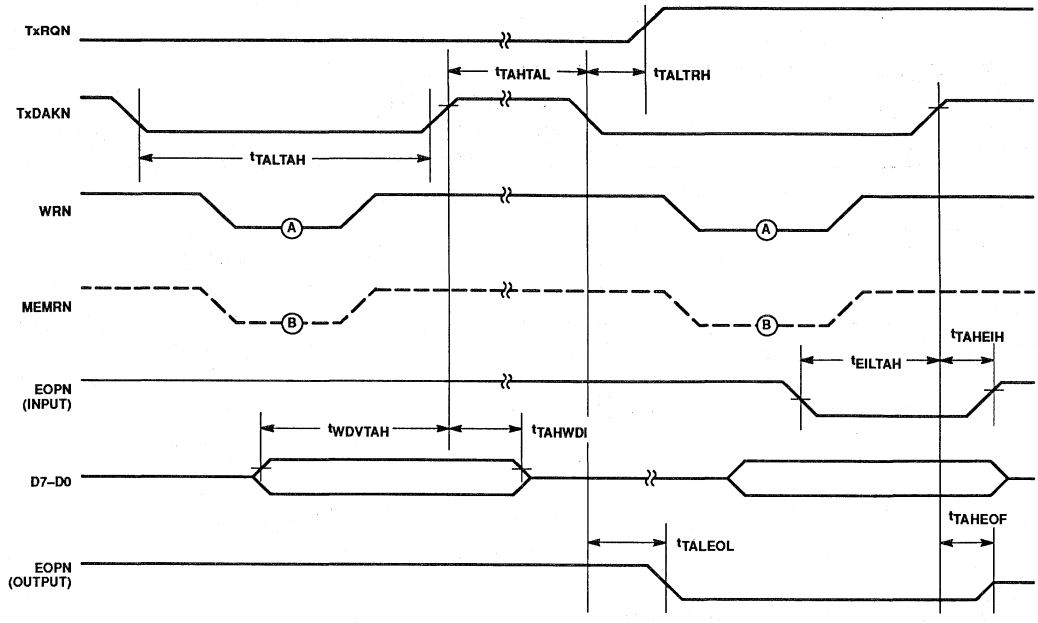


A The RxFIFO is addressed during this read cycle.

11. Receive Dual Address DMA Timing

SYMBOL	PARAMETER	LIMITS		UNIT
		SC26C562		
		Min	Max	
t_{RDLRRH}	RDN low to Rx DMA REQN high		100	ns
t_{RDLEOL}	RDN low to EOPN output low		100	ns
t_{RDHEOZ}	RDN high to EOPN output high impedance		90	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

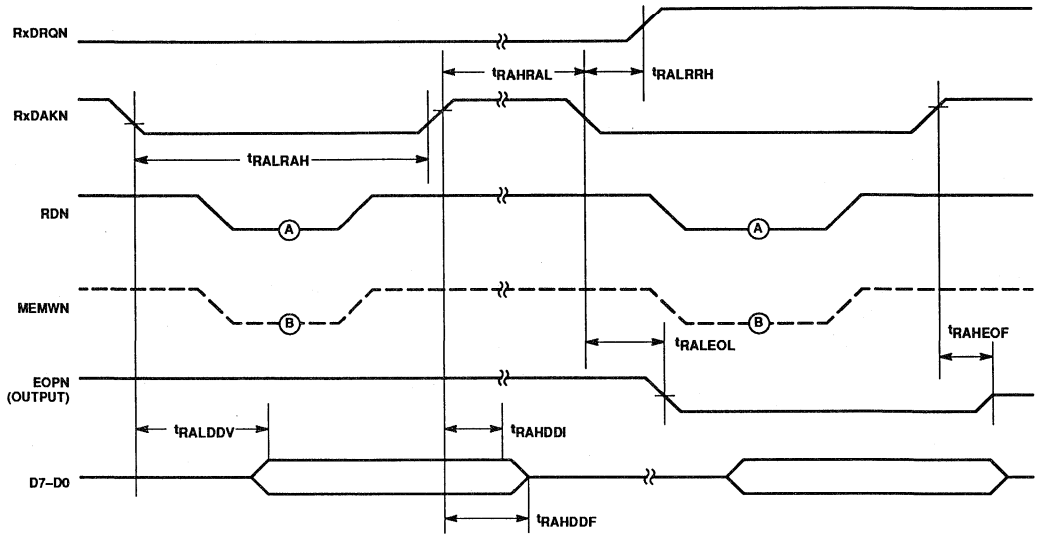


NOTES:
(A) Ignored by the CDUSCC since CEN is not asserted, but it can be used externally to qualify TxDAKN.
(B) Memory read signal; not seen by CDUSCC.

12. DMA–Transmit Single Address Mode

SYMBOL	PARAMETER	LIMITS		UNIT
		SC26C562		
		Min	Max	
t_{TAHTAL}	Transmit DMA ACKN high to low time	60		ns
t_{TALTAH}	Transmit DMA ACKN low to high time	110		ns
t_{TALTRH}	Tx DMA ACKN low to Tx DMA REQN high		80	ns
t_{WDVTAH}	Write data valid to Tx DMA ACKN high	40		ns
t_{TAHWDI}	Tx DMA ACKN high to write data invalid	0		ns
t_{TALEOL}	Tx DMA ACKN low to EOPN output low		80	ns
t_{TAHEOF}	Tx DMA ACKN high to EOPN output float		50	ns
t_{EILTAH}	EOPN input low to Tx DMA ACKN high	30		ns
t_{TAHEIH}	Tx DMA ACKN high to EOPN input high	0		ns

AC ELECTRICAL CHARACTERISTICS (Continued)

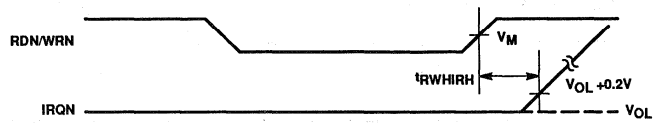


NOTES:
(A) Ignored by the CDUSCC bit; it can be used to qualify RxDAKN.
(B) Memory read signal; not seen by CDUSCC.

13. DMA–Receive Single Address Mode

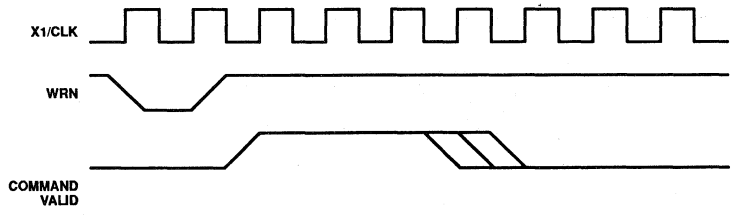
SYMBOL	PARAMETER	LIMITS SC26C562 Min	LIMITS SC26C562 Max	UNIT
t_{RAHRAL}	Receive DMA ACKN high to low time	60		ns
t_{RALRAH}	Receive DMA ACKN low to high time	110		ns
t_{RALRRH}	Rx DMA ACKN low to Rx DMA REQN high		100	ns
t_{RALEOL}	Rx DMA ACKN low to EOPN output low		100	ns
t_{RAHEOF}	Rx DMA ACKN high to EOPN output float		50	ns
t_{RALDDV}	Rx DMA ACKN low to read data valid		110	ns
t_{RAHDDI}	Rx DMA ACKN high to read data invalid	5		ns
t_{RAHDDF}	Rx DMA ACKN high to data bus float		40	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

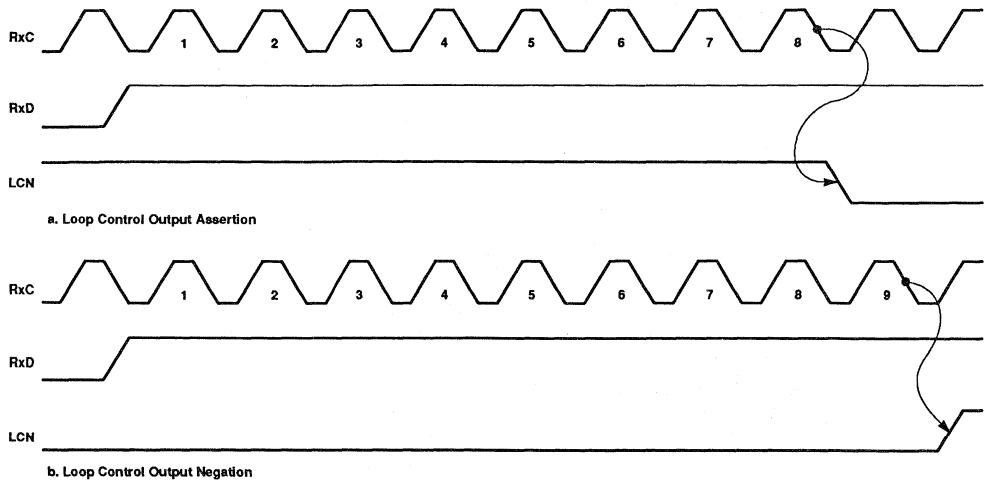


14. Interrupt Timing

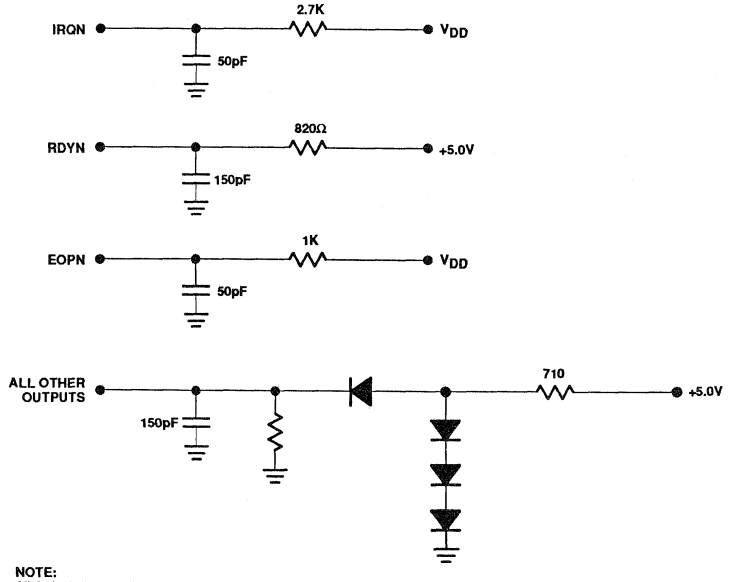
SYMBOL	PARAMETER	LIMITS SC26C562 Min	LIMITS SC26C562 Max	UNIT
t_{RWHIRH}	RDN/WRN high to IRQN high for:			
	Read RxFIFO (RxRDY interrupt)		80	ns
	Write TxFIFO (TxRDY interrupt)		80	ns
	Write RSR (Rx condition interrupt)		80	ns
	Write TRSR (Rx/Tx interrupt)		80	ns
	Write ICTSR (counter/timer interrupt)		80	ns



15. Command Timing



16. Relationship Between Received Data and the Loop Control Output



NOTE:
All C_L includes 50pF stray capacitance,
i.e., C_L = 150pF = 100pF discrete +50pF stray.

17. Test Conditions for Outputs

CMOS Dual universal serial communications controller (CDUSCC)

SC68C562

DESCRIPTION

The Signetics SC68C562 Dual Universal Serial Communications Controller (CDUSCC) is a single-chip CMOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SC68C562 interfaces to the 68000 MPUs via asynchronous bus control signals and is capable of program-polled, interrupt driven, block-move or DMA data transfers.

The SC68C562 is hardware (pin) and software (Register) compatible with SCN68562 (NMOS version). It will automatically configure to NMOS DUSCC register map on power-up or reset.

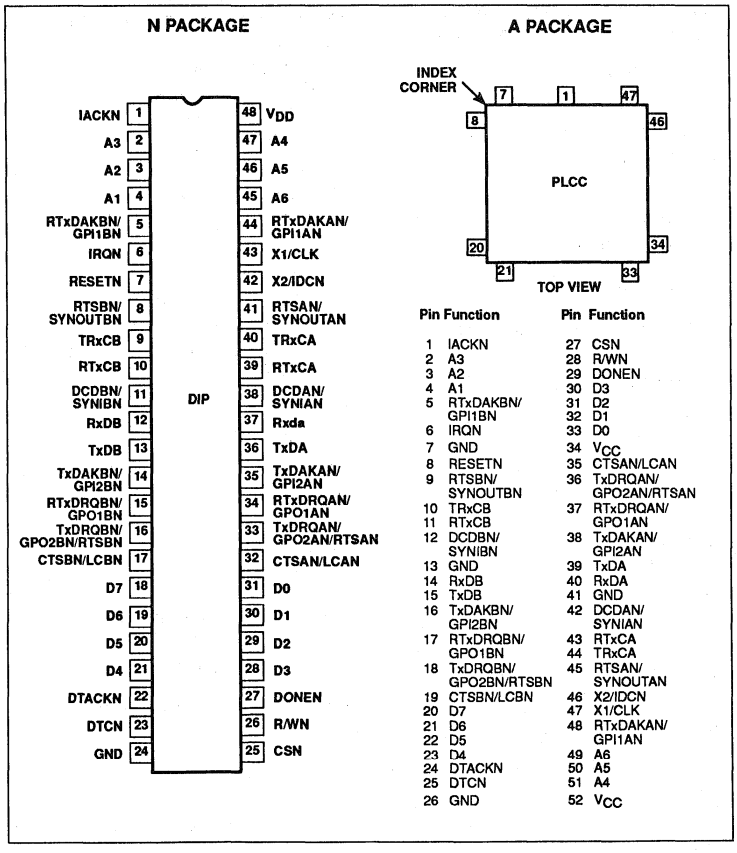
The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides 16 common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock.

This makes the CDUSCC well suited for dual speed channel applications. Data rates up to 10Mb/s are supported.

Each transmitter and each receiver is serviced by a 16 byte FIFO. The receiver FIFO also stores 9 status bits for each character received; the transmit FIFO is able to store transmitter commands with each byte. This permits reading and writing of up to 16 bytes at a time, thus minimizing the potential for transmitter underrun, receiver overrun and reducing interrupt or DMA overhead.

In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full. Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs are general purpose in nature, they can be optionally programmed for other functions. This document contains the electrical specifications for the SC68C562. Refer to the CMOS Dual Universal Serial Communications Controller (CDUSCC) User Manual for a complete operational description of this product.

PIN CONFIGURATIONS



Pin	Function	Pin	Function
1	IACKN	27	CSN
2	A3	28	R/WN
3	A2	29	DONEN
4	A1	30	D3
5	RTxDAKBN/ GPI1BN	31	D2
6	IRQN	32	D1
7	GND	33	D0
8	RESETN	34	V_{CC}
9	RTSBN/ SYNOUTBN	35	CTSAN/LCAN
10	TRxCB	36	TxDRQAN/ GPO2AN/RTSAN
11	RTxCB	37	RTxDRQAN/ GPO1AN
12	DCDBN/ SYNIBN	38	TxDAKAN/ GPI2AN
13	GND	39	TxDA
14	RxDB	40	RxDA
15	TxDB	41	GND
16	TxDAKBN/ GPI2BN	42	DCDAN/ SYNIAN
17	RTxDRQBN/ GPO1BN	43	RTxCA
18	TxDRQBN/ GPO2BN/RTSBN	44	TRxCA
19	CTSBN/LCBN	45	RTSAN/ SYNOUTAN
20	D7	46	X2/IDCN
21	D6	47	X1/CLK
22	D5	48	RTxDAKAN/ GPI1AN
23	D4	49	A6
24	DTACKN	50	A5
25	DTCN	51	A4
26	GND	52	V_{CC}

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±10%, T_A = 0°C to +70°C Serial Data Rate = 10Mpbs Maximum
48-Pin Plastic DIP	SC68C562C1N
52-Pin PLCC	SC68C562C1A

CMOS Dual universal serial communications controller (CDUSCC) SC68C562

FEATURES

- Full hardware and software upwared compatibility with previous NMOS device

General Features

- Dual full-duplex synchronous/ asynchronous receiver and transmitter
- Low power CMOS process
- Multiprotocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
  - COP: BISYNC, DDCMP
  - ASYNC: 5–8 bits plus optional parity
- Sixteen character receiver and transmitter FIFOs
- 0 to 10MHz data rate
- Programmable bit rate for each receiver and transmitter selectable from:
  - 19 fixed rates: 50 to 64k baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
  - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- and half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Compatible with the Signetics SCB68430 Direct Memory Access Interface (DMAI) and other DMA controllers
  - Single- or dual-address dual transfers
  - Half- or full-duplex operation
  - Automatic frame termination on counter/timer terminal count or DMA DONE
- Transmit path clear status
- Interrupt capabilities
  - Daisy chain option
  - Vector output (fixed or modified by status)
  - Programmable internal priorities
  - Interrupt at any FIFO fill level
  - Maskable interrupt conditions
- FIFO'd status bits
- Watchdog timer
- Multi-function programmable 16-bit counter/timer
  - Bit rate generator
  - Event counter
  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general I/O pins per channel
  - CTS and DCD programmable auto-enables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- 1X or 16X Rx and Tx clock factors
- Parity, overrun, and framing error detection
- False start bit detection
- Start bit search 1/2-bit time after framing error detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmits up to 10Mb/s at 1X and receive up to 1Mb/s at 16X data rates

Character-Oriented Protocol Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK line fill on underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun, and underrun error detection

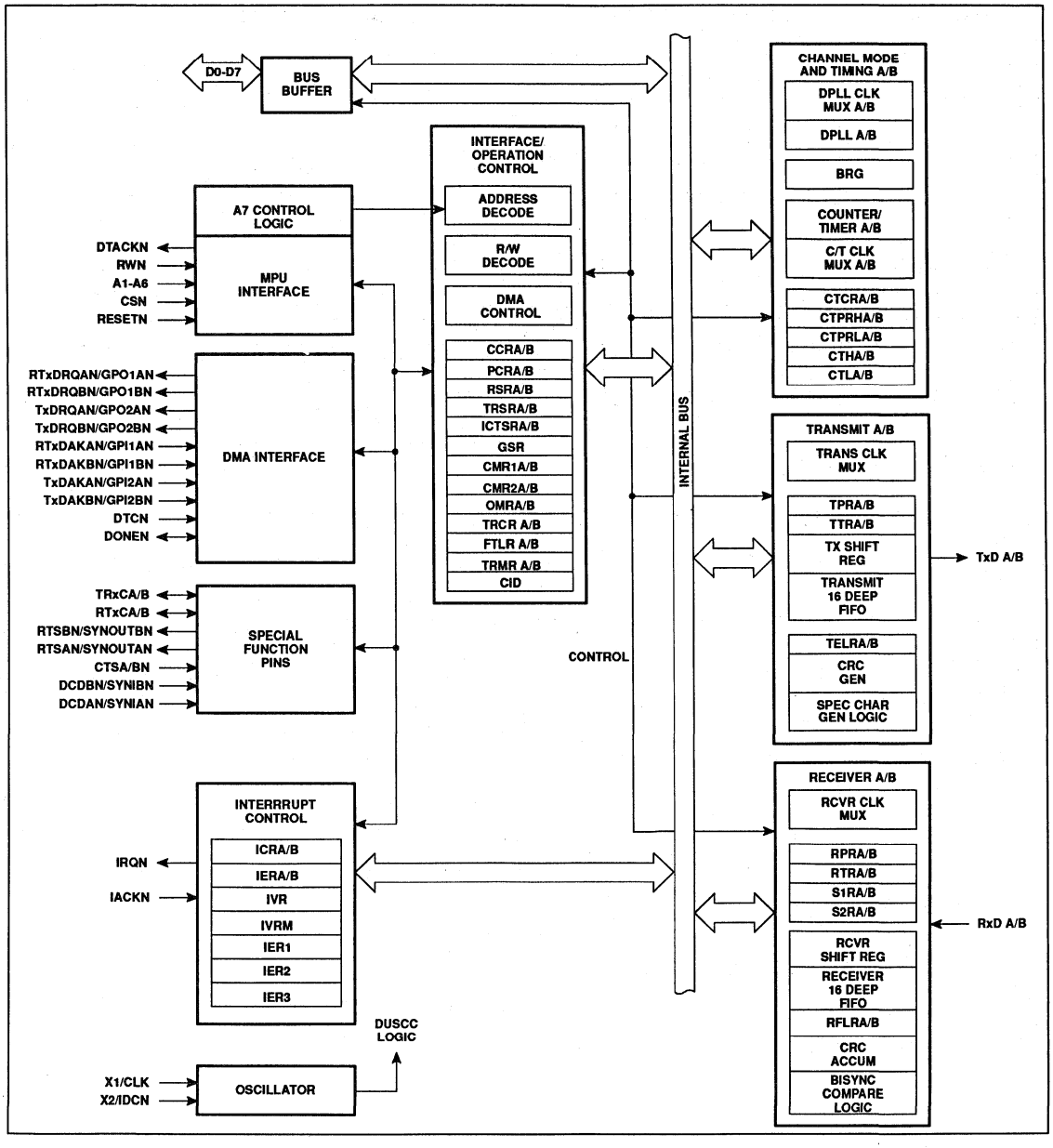
BISYNC Features

- EBCDIC or ASCII header, text and control messages
- SYN, DLE stripping
- EOM (end of message) detection and transmission
- Auto transparent mode switching
- Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
- Control character sequence detection for both transparent and normal text

Bit-Oriented Protocol Features

- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Automatic switch to programmed character length for I field
- Zero insertion and deletion
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- ABORT, ABORT-FLAGs, or FCS FLAGs line fill on underrun
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A1 – A6	4-2, 47-45	4-2, 51-49	I	Address Lines
D0 – D7	31-28, 21-18	33-30, 23-20	I/O	Bidirectional Data Bus
R/WN	26	28	I	Read/Write
CSN	25	27	I	Chip Select
DTACKN	22	24	O	Data Transfer Acknowledge
IRQN	6	6	O	Interrupt Request
IACKN	1	1	I	Interrupt Acknowledge
X1/CLK	43	47	I	Crystal or External Clock
X2/IDCN	42	46	O	Crystal or Interrupt Daisy Chain
RESETN	7	8	I	Master Reset
RxDA, RxDB	37, 12	40, 14	I	Channel A (B) Receiver Serial Data Input
TxDA, TxDB	36, 13	39, 15	O	Channel A (B) Transmitter Serial Data Output
RTxCA, RTxCB	39, 10	43, 11	I/O	Channel A (B) Receiver/Transmitter Clock
TRxCA, TRxCB	40, 9	44, 10	I/O	Channel A (B) Transmitter/Receiver Clock
CTSA/BN, LCA/BN	32, 17	35, 19	I/O	Channel A (B) Clear-To-Send Input or Loop Control Output
DCDA/BN, SYNIA/BN	38, 11	42, 12	I	Channel A (B) Data Carrier Detected or External Sync Input
RTxDRQA/BN, GPO1A/BN	34, 15	37, 17	O	Channel A (B) Receiver/Transmitter DMA Service Request or General Purpose Output
TxDRQA/BN, GPO2A/BN, RTSA/BN	33, 16	36, 18	O	Channel A (B) Transmitter DMA Service Request, General Purpose Output, or Request-to-Send
RTxDAKA/BN, GPI1A/BN	44, 5	48, 5	I	Channel A (B) Receiver/Transmitter DMA Acknowledge or General Purpose Input
TxDAKA/BN, GP12A/BN	35, 14	38, 16	I	Channel A (B) Transmitter DMA Acknowledge or General Purpose Input
DTCN	23	25	I	Device Transfer Complete
DONEN	27	29	I/O	Done
RTSA/BN, SYNOUTA/BN	41, 8	45, 9	O	Channel A (B) Sync Detect or Request-to-Send
V_{CC}	48	34, 52	I	Power input
GND	24	7, 13, 26, 41	I	Signal and power ground

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature	0 to +70	°C
T_{STG}	Storage Temperature	-65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	-0.5 to +7.0	V
V_S	Voltage from any pin to ground[3]	-0.5 to V_{CC} +0.5	V

DC ELECTRICAL CHARACTERISTICS[4, 5] T_A = 0 to +70°C, V_{CC} = 5.0V ± 10%

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage:					
	All except X1/CLK				0.8	V
	X1/CLK				0.4	V
V_{IH}	Input high voltage:					
	All except X1/CLK		2.0			V
	X1/CLK		2.4		V_{CC}	V
V_{OL}	Output low voltage:					
	All except IRQN, DONEN[14]	I_{OL} = 5.3mA			0.5	V
	IRQN, DONEN[7]	I_{OL} = 8.8mA			0.5	V
	Output high voltage:					
V_{OH}	(Except open drain outputs)	I_{OH} = -400µA	2.4			V
I_{ILX1}	X1/CLK input low current[10]	V_{IN} = 0, X2 = GND	-5.5		0.0	mA
I_{IHX1}	X1/CLK input high current[10]	V_{IN} = V_{CC}, X2 = GND			1.0	mA
I_{SCX2}	X2 short circuit current[4]	X2 = GND, X1 open			15	µA
I_{IL}	Input low current					
	DTCN, TxDAKA/BN, RTxDAKA/BN	V_{IN} = 0	-40			µA
I_L	Input leakage current	V_{IN} = 0 to V_{CC}	-5		5	µA
I_{OZH}	Output off current high, 3-State data bus	V_{IN} = V_{CC}			5	µA
I_{OZL}	Output off current low, 3-State data bus	V_{IN} = 0	-5			µA
I_{ODL}	Open drain output low current in off	V_{IN} = 0				
	state: DONEN		-120		-25	µA
	IRQN, DTACKN (3-state)		-5			µA
I_{ODH}	Open drain output high current in off	V_{IN} = V_{CC}				
	state: DONEN, IRQN, DTACKN (3-state)				5	µA
I_{CC}	Power supply current	V_O = 0 to V_{CC}, Rx/Tx at 10MHz and X1 at 14.745MHz			60	mA
C_{IN}	Input capacitance[9]	V_{CC} = GND = 0			10	pF
C_{OUT}	Output capacitance[9]	V_{CC} = GND = 0			15	pF
$C_{I/O}$	Input/output capacitance[9]	V_{CC} = GND = 0			20	pF

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.
2. Clock may be stopped (DC) for testing purposes or when the CDUSCC is in non-operational modes. Operation down to 0 rate clocks is implied by a full static CMOS design, but is not verified in testing or characterization.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature and voltage range.
5. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK, this swing is between 0V and 2.8V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
6. See Figure 17 for test conditions for outputs.
7. Tests for open drain outputs are intended to guarantee switching of the output transistor. Measurement of this response is referenced from midpoint of the switching signal to a point 0.2V above the actual output signal level. This point represents noise margin that assures that the true switching has occurred.
8. Execution of the valid command (after it is latched) requires a minimum of three and a maximum of four falling edges of X1 (see Figure 18).
9. These values were no explicitly tested; they are guaranteed by design and characterization data.
10. X1/CLK and X2 are not tested with a crystal installed.
11. X1/CLK frequency must be at least as fast as the faster of the receiver or transmitter data rate.
12. Based on a 14.7456MHz X1 clock. The X1 clock is used in the timing of DTACKN, Baud Rate Generator, command register and the update of the FIFO fill level encoders. The Command Register requires three X1 clocks between two commands; FIFO fill level encoding requires 2.5 to 3.5 X1 cycles. The Baud Rate Generator is driven by the X1 clock.
13. The 68562 bus interface may be operated in two modes; a 68000 compatible mode with automatic DTACK generation and a short chip select mode. DTACKN should not be used externally in the short chip select mode. The DTACKN signal is generated by the assertion of the chip select, and data is latched by assertion of DTACKN or by de-assertion of the chip select. In single address DMA, the DTACK signal will be de-asserted by the assertion of the DTCN or from the de-assertion of the TxDAKN, whichever occurs first.
14. Also includes X2/IDCN pin in IDC mode.

Figure 1. Reset Timing

SYMBOL	PARAMETER	LIMITS SC68C562 Min	LIMITS SC68C562 Max	UNIT
t_{RELREH}	RESETN low to RESETN high	1.2		µs

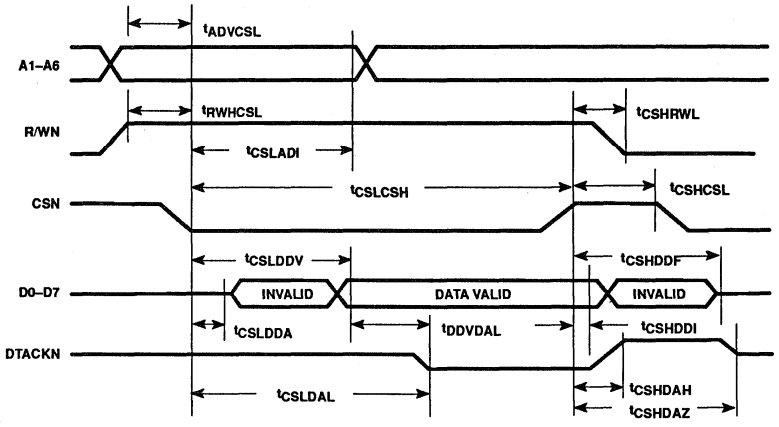


Figure 2. Read Cycle Bus Timing

Times represent an X1 clock frequency of 14.745MHz

SYMBOL	PARAMETER	LIMITS SC68C562 Min	LIMITS SC68C562 Max	UNIT
t_{ADVCSL}	A0-A6 valid to CSN low	0		ns
t_{RWHCSL}	RWN high to CSN low	0		ns
t_{CSHRWL}	CSN high to RWN low	0		ns
t_{CSHCSL}	CSN high to CSN low[8]	60		ns
t_{CSLDDV}	CSN low to read data valid		110	ns
t_{CSHDDF}	CSN high to data bus float		40	ns
t_{DDVDAL}	Read data valid to DTACKN low	0		ns
t_{DALCSH}	DTACKN low to CSN high	0		ns
t_{CSLDAL}	CSN low to DTACKN low[12]	70	135	ns
t_{CSHDAH}	CSN high to DTACKN high		40	ns
t_{CSHDAZ}	CSN high to DTACKN high impedance		60	ns
t_{CSLADI}	CSN low to address invalid	30		ns
t_{CSLCSH}	CSN low to CSN high	110		ns
t_{CSLDDA}	CSN low to data bus driver active	0		ns
t_{CSHDDI}	CSN high to data invalid	5		ns

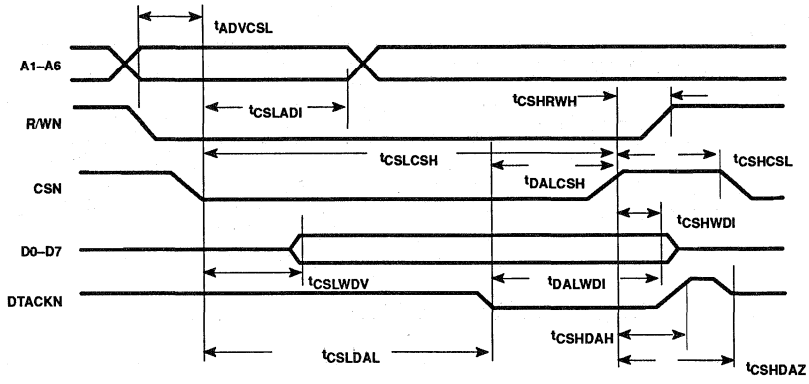


Figure 3. Write Cycle Bus Timing

SYMBOL	PARAMETER[12]	LIMITS SC68C562		UNIT
		Min	Max	
t_{ADVCSL}	A0-A6 valid to CSN low	0		ns
t_{CSLADI}	CSN low to A0-A6 invalid	30		ns
t_{RWLCSL}	RWN low to CSN low	0		ns
t_{CSHRWH}	CSN high to RWN high	0		ns
t_{CSHCSL}	CSN high to CSN low[8]	60		ns
t_{DALCSH}	DTACKN low to CSN high	0		ns
t_{DALWDI}	DTACKN low to write data invalid	0		ns
t_{CSLDAL}	CSN low to DTACKN low[12]	70	135	ns
t_{CSHDAH}	CSN high to DTACKN high		40	ns
t_{CSHDAZ}	CSN high to DTACKN high impedance		60	ns
t_{CSLCSH}	CSN low to CSN high	110		ns
t_{CSLWDV}	CSN low to write data valid		50	ns
t_{CSHWDI}	CSN high to write data invalid	0		ns

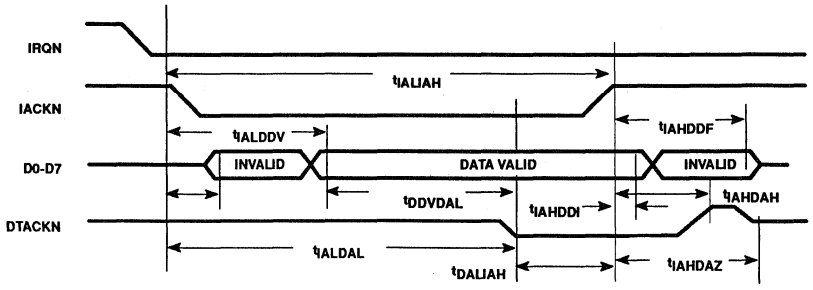


Figure 4. Interrupt Cycle Timing

SYMBOL	PARAMETER[12]	LIMITS		UNIT
		SC68C562		
		Min	Max	
t_{IALIAH}	IACKN low to IACKN high	110		ns
t_{IALDDA}	IACKN low to data bus drivers active	0		ns
t_{IALDDV}	IACKN low to read data valid		110	ns
t_{IALDDF}	IACKN high to data bus floating		50	ns
t_{DDVDAL}	Read data valid to DTACKN low	0		ns
t_{IAHDAH}	IACKN high to DTACKN high		50	ns
t_{IAHDAZ}	IACKN high to DTACKN high impedance		60	ns
t_{IALDAL}	IACKN low to DTACKN low[12]	75	135	ns
t_{IAHDDI}	IACKN high to data bus invalid	5		ns
t_{DALIAH}	DTACKN low to IACKN high	0		ns

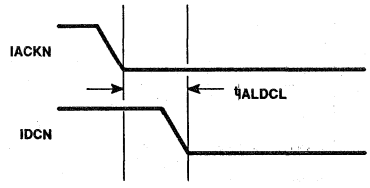


Figure 5. Interrupt Daisy Chain Timing

SYMBOL	PARAMETER	LIMITS		UNIT
		SC68C562		
		Min	Max	
t_{IALDCL}	IACKN low to IDCN (daisy chain) low		50	ns

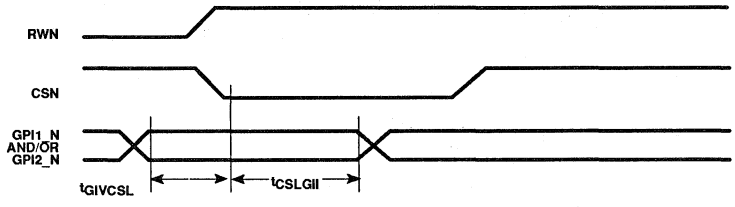


Figure 6. Input Port Timing

SYMBOL	PARAMETER	LIMITS		UNIT
		SC68C562		
		Min	Max	
t_{GIVCSL}	GPI input valid to CSN low	20		ns
t_{CLSGII}	CSN low to GPI input invalid	50		ns

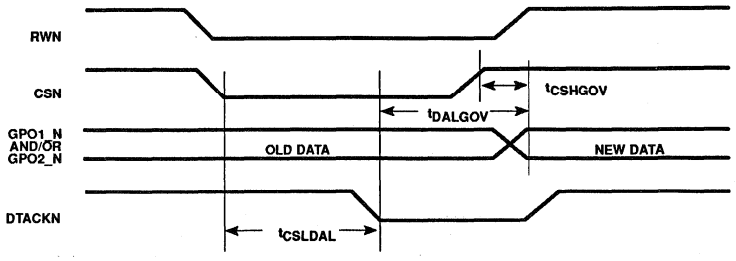


Figure 7. Output Port Timing

SYMBOL	PARAMETER	LIMITS SC68C562 Min	LIMITS SC68C562 Max	UNIT
t_{DALGOV}	DTACKN low to GPO output data valid		50	ns
t_{CSLDAL}	CSN low to DTACKN low	70	135	ns
t_{CSHGOV}	CSN high to GPO output data valid		50	ns

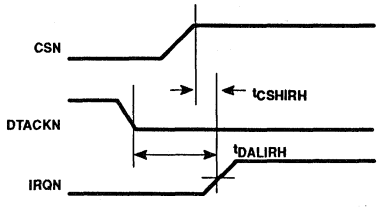


Figure 8. Interrupt Timing, Write Cycle

SYMBOL	PARAMETER	LIMITS SC68C562 Min	LIMITS SC68C562 Max	UNIT
t_{DALIRH}	DTACKN low to IRQN high, write cycle			
	Write TxFIFO (TxRDY interrupt)		50	ns
	Write RSR (Rx condition interrupt)		50	ns
	Write TRSR (Rx/Tx interrupt)		50	ns
	Write ICTSR (port change and CT interrupt)		50	ns
t_{CSHIRH}	CSN high to IRQN high, write cycle			
	Write TxFIFO (TxRDY interrupt)		50	ns
	Write RSR (Rx condition interrupt)		50	ns
	Write TRSR (Rx/Tx interrupt)		50	ns
	Write ICTSR (port change and CT interrupt)		50	ns

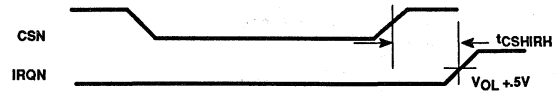


Figure 9. Interrupt Timing, Read Cycle

SYMBOL	PARAMETER	LIMITS SC68C562		UNIT
		Min	Max	
t_{CSHIRH}	CSN high to IRQN high, read cycle			
	Read RxFIFO (RxRDY interrupt)		50	ns

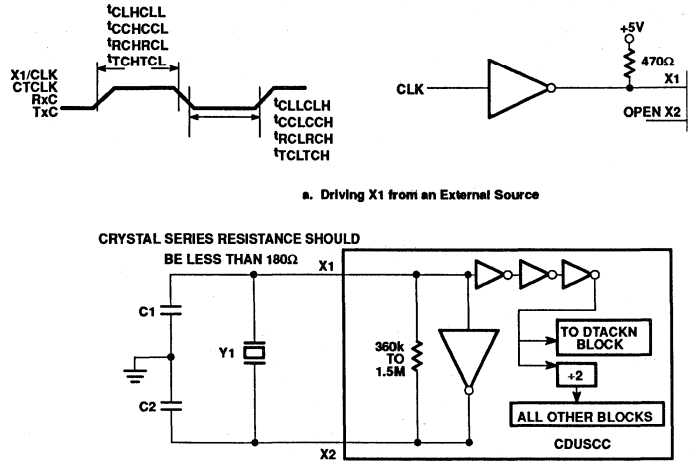


Figure 10. Receive, Dual Adress DMA

SYMBOL	PARAMETER	LIMITS SC68C562			UNIT
		Min	Typ	Max	
t_{CLHCLL}	X1/CLK high to low time	25			ns
t_{CLLCLH}	X1/CLK low to high time	25			ns
t_{CCHCCL}	CT CLK high to low time	50			ns
t_{CCLCCH}	CT CLK low to high time	50			ns
t_{RCHRCL}	RxC high to low time	50			ns
t_{RCLRCH}	RxC low to high time	50			ns
t_{TCHTCL}	TxC high to low time	50			ns
t_{TCLTCH}	TxC low to high time	50			ns
f_{CL}	X1/CLK frequency[11, 2]	0	14.7456	16.0	MHz
f_{CC}	CT CLK frequency	0[9]		10	MHz
f_{RC}	RxC frequency (16X or 1X)	0[9]		10	MHz
f_{TC}	TxC frequency (16X or 1X)	0[9]		10	MHz

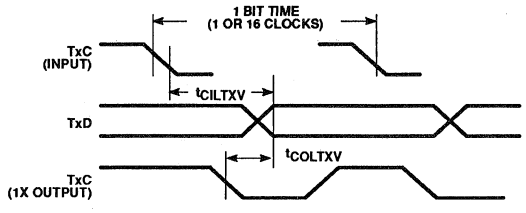


Figure 11. Transmit Timing

SYMBOL	PARAMETER	LIMITS SC68C562 Min	LIMITS SC68C562 Max	UNIT
t_{CILTXV}	TxC input low (1X) to TxD output		70	ns
	TxC input low (16X) to TxD output		80	ns
t_{COLTXV}	TxC output low to TxD output		30	ns

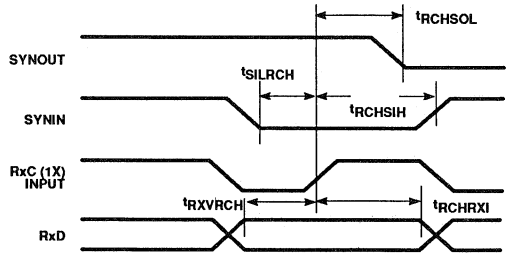


Figure 12. Receive Timing

SYMBOL	PARAMETER	LIMITS SC68C562 Min	LIMITS SC68C562 Max	UNIT
t_{RXVRCH}	RxD data valid to RxC high:			
	For NRZ data	50		ns
	For NRZI, Manchester, FM0, FM1 data	50		ns
t_{RCHRXI}	RxC high to RxD data invalid:			
	For NRZ data	0		ns
	For NRZI, Manchester, FM0, FM1 data	0		ns
t_{SILRCH}	SYNIN low to RxC high	50		ns
t_{RCHSIH}	RxC high to SYNIN high	0		ns
t_{RCHSOL}	RxC high to SYNOUT low		80	ns

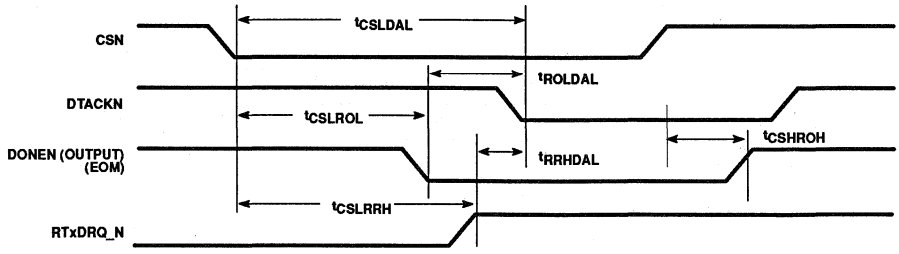


Figure 13. Receive, Dual Address DMA

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{CSLROL}	CSN low to Rx DONEN output low		100	ns
t_{CSLRRH}	CSN low to Rx DMA REQN high	90	100	ns
t_{CSHROH}	CSN high to Rx DONEN output high		60	ns
t_{ROLDAL}	Rx DONEN output low to DTACKN low	20		ns
t_{RRHDAL}	Rx DMA REQN high to DTACKN low	20		ns
t_{CSLDAL}	CSN low to DTACKN low	70	135	ns

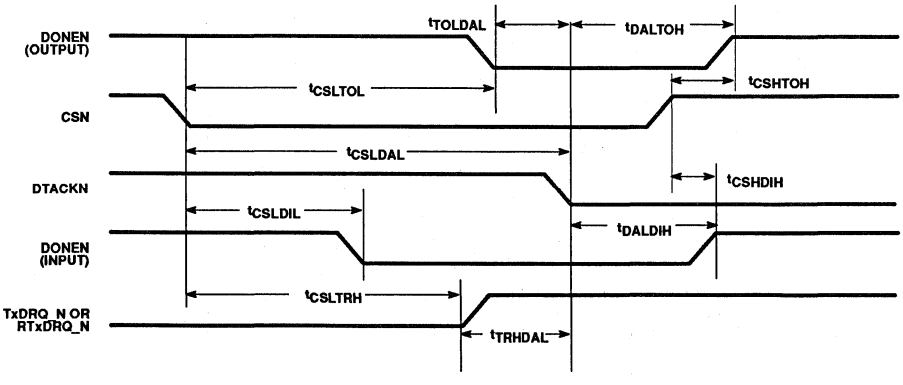


Figure 14. Transmit, Dual Adress DMA

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{CSLTOL}	CSN low to Tx DONEN output low		150	ns
t_{CSLTRH}	CSN low to Tx DMA REQN high	90	150	ns
t_{DALDIH}	DTACKN low to Tx DONEN input high	0		ns
t_{DALTOH}	DTACKN low to Tx DONEN output high		60	ns
t_{TOLDAL}	Tx DONEN output low to DTACKN low	20		ns
t_{TRHDAL}	Tx DMA REQN high to DTACKN low	20		ns
t_{CSLDAL}	CSN low to DTACKN low	70	135	ns
t_{CSLDIL}	CSN low to Tx DONEN input low		75	ns
t_{CSHTOH}	CSN high to Tx DONEN output high		50	ns
t_{CSHDIH}	CSN high to Tx DONEN input high	0		ns

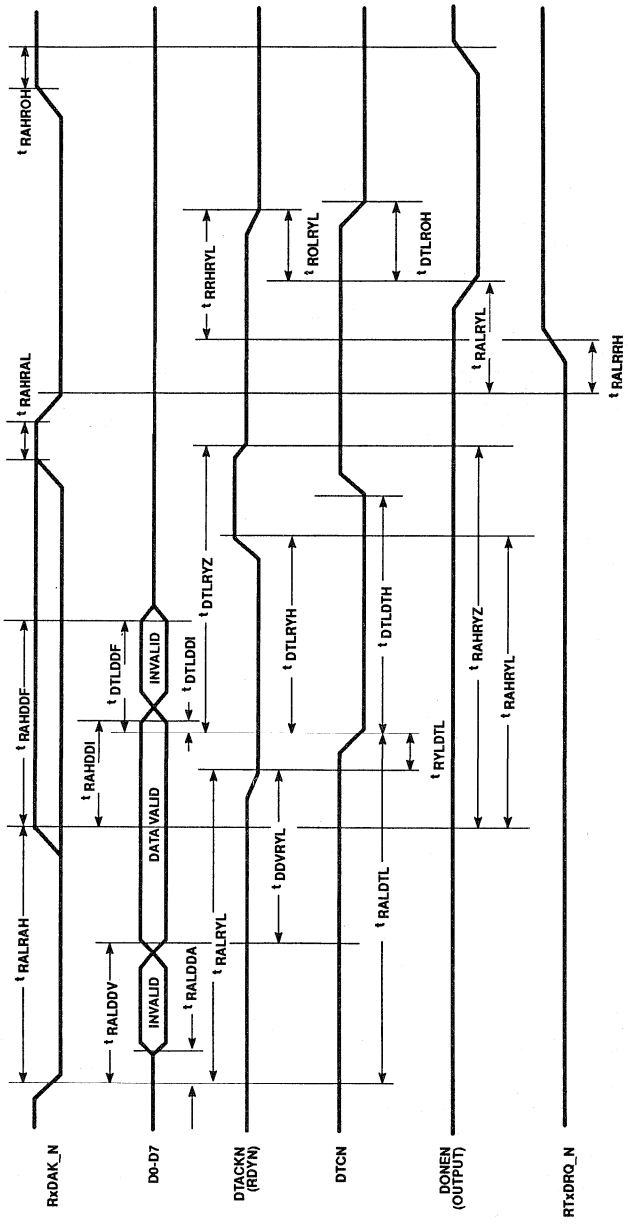


Figure 15. DMA Rx Read Timing — Single Address DMA

DMA Rx Read Timing — Single Address DMA

SYMBOL	PARAMETER	LIMITS		UNIT
		SC68C562		
		Min	Max	
t_{RALDDV}	Receive DMA ACKN low to read data valid		110	ns
t_{DTLDTH}	DTCN low to DTCN high	40		ns
t_{RYLDTL}	RDYN low to DTCN low	0		ns
t_{DTLDDF}	DTCN low to data bus float[13]		80	ns
t_{RALRYL}	Rx DMA ACK low to RDYN low[12]		135	ns
t_{DDVRYL}	Read data valid to RDYN low[12]	0		ns
t_{DTLRYH}	DTCN low to RDYN high		80	ns
t_{DTLRYZ}	DTCN low to RDYN high impedance		100	ns
t_{RRHRYL}	Rx DMA REQN high to RDYN low[12]	10		ns
t_{ROLRYL}	Rx DONEN output low to RDYN low[12]	0		ns
t_{RALRRH}	Rx DMA ACKN low to receive DMA REQN high		150	ns
t_{RAHRAL}	Receive DMA ACKN high to low time	60		ns
t_{RALROL}	Rx DMA ACK low to Rx DONEN output low		150	ns
t_{DTLROH}	DTCN low to Rx DONEN output high		60	ns
t_{RALRAH}	Rx DMA ACKN low to Rx DMA ACKN high	110		ns
t_{RAHDDF}	Rx DMA ACKN high to data bus float		40	ns
t_{RALDDA}	Rx DMA ACKN low to data bus drivers active[12]	0		ns
t_{RAHDDI}	Rx DMA ACKN high to data bus invalid	0		ns
t_{DTLDDI}	DTCN low to data bus invalid	0		ns
t_{RALDTL}	Rx DMA ACKN low to DTCN low	70		ns
t_{RAHRYH}	Rx DMA ACKN high to RDYN high		80	ns
t_{RAHRYZ}	Rx DMA ACKN high to RDYN high impedance		100	ns
t_{RAHROH}	Rx DMA ACKN high to DONEN output high		50	ns

DMA Tx Write Timing — Single Address DMA

SYMBOL	PARAMETER	LIMITS		UNIT
		SC68C562		
		Min	Max	
t_{DTLDTH}	DTCN low to DTCN high	40		ns
t_{RYLDTL}	RDYN low to DTCN low	0		ns
t_{TALRYL}	Tx DMA ACK low to RDYN low		135	ns
t_{DTLRYH}	DTCN low to RDYN high[12]		80	ns
t_{DTLRYZ}	DTCN low to RDYN high impedance		100	ns
t_{TRHRYL}	Tx DMA REQN high to RDYN low[12]	0		ns
t_{TOLRYL}	Tx DONEN output low to RDYN low[12]	0		ns
t_{DTLTOH}	DTCN low to Tx DONEN output high[12]		60	ns
t_{WDVDTL}	Write data valid to DTCN low	0		ns
t_{DTLWDI}	DTCN low to write data invalid	10		ns
t_{TALTRH}	ACKN low to transmit DMA REQN high		80	ns
t_{TAHTAL}	Transmit DMA ACKN high to low time	60		ns
t_{TALTOL}	Tx DMA ACKN to Tx DONEN output low		80	ns
t_{DILDTL}	Transmit DONEN input low to DTCN low	0		ns
t_{DTLDIH}	DTCN low to transmit DONEN input high	60		ns
t_{TALTAH}	Tx ACKN low to Tx ACKN high	110		ns
t_{TAHWDI}	Tx ACKN high to write data invalid	0		ns
t_{WDVTAH}	Write data valid to Tx DAKN high	40		ns
t_{TAHRYH}	Tx DAKN high to RDYN high		80	ns
t_{TAHRYZ}	Tx DAKN high to RDYN high impedance		100	ns
t_{TAHTOH}	Tx DAKN high to DONEN output high		50	ns
t_{DILTAH}	DONEN input low to Tx DAKN high	0		ns
t_{TAHDIH}	Tx DAKN high to DONEN input high	0		ns
t_{TALDTL}	Tx DAKN low to DTCN low	70	135	ns

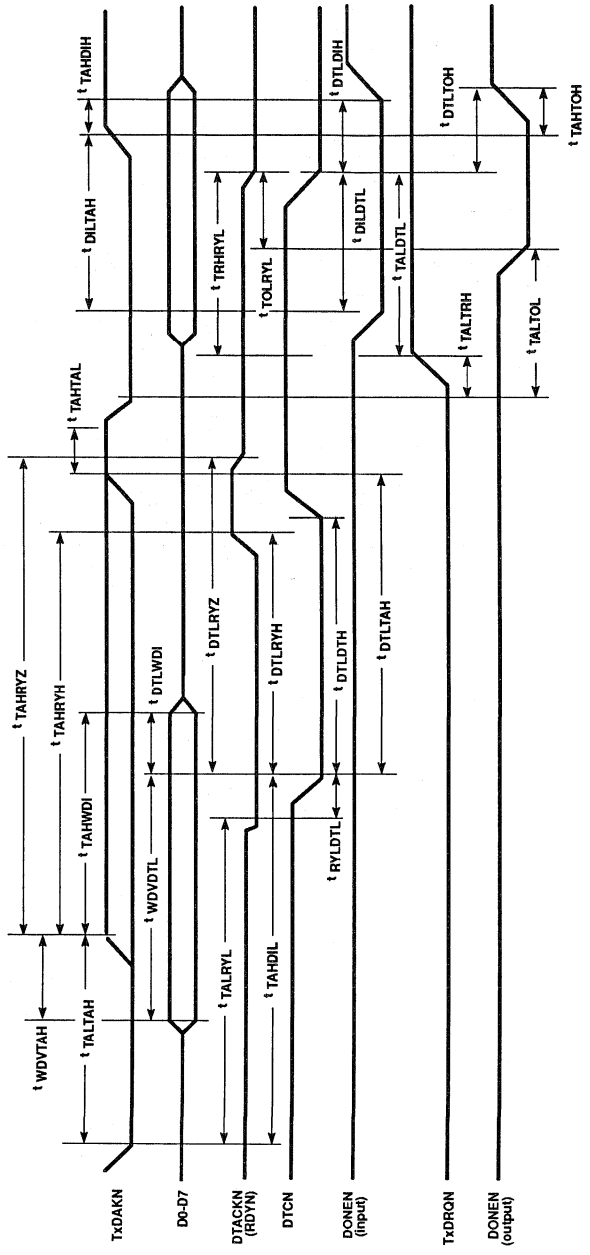
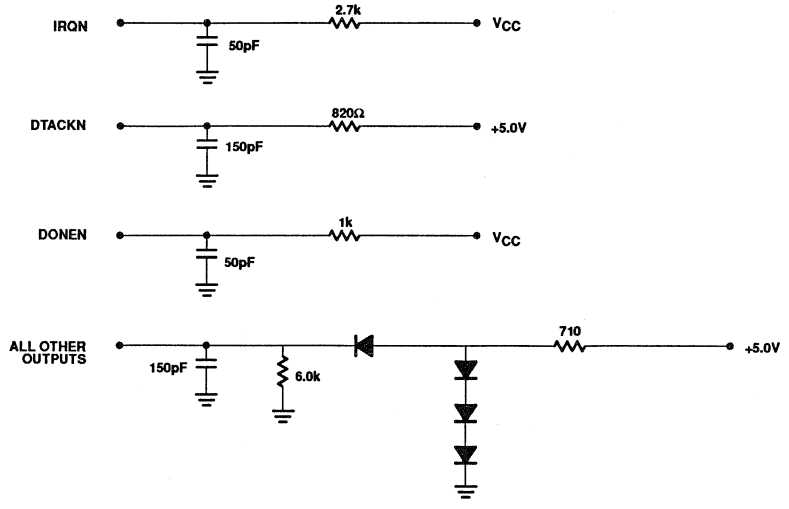


Figure 16. DMA Rx Write Timing — Single Address DMA



NOTE:
All C_L includes 50pF stray capacitance, i.e., C_L = 150pF = (100pF discrete + 50pF stray).

Figure 17. Test Conditions for Outputs

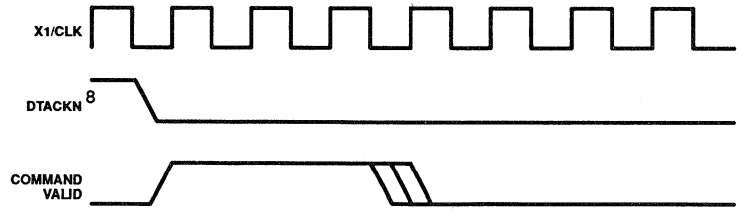


Figure 18. Command Timing

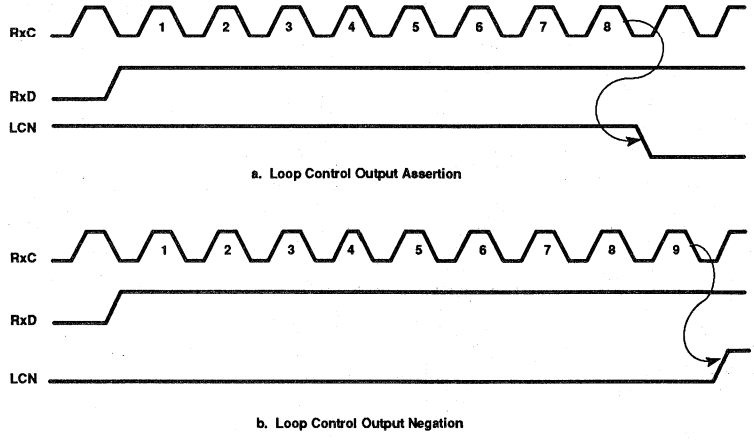


Figure 19. Relationship Between Received Data and the Loop Control Output

Dual universal serial communications controller (DUSCC) SCN68562

DESCRIPTION

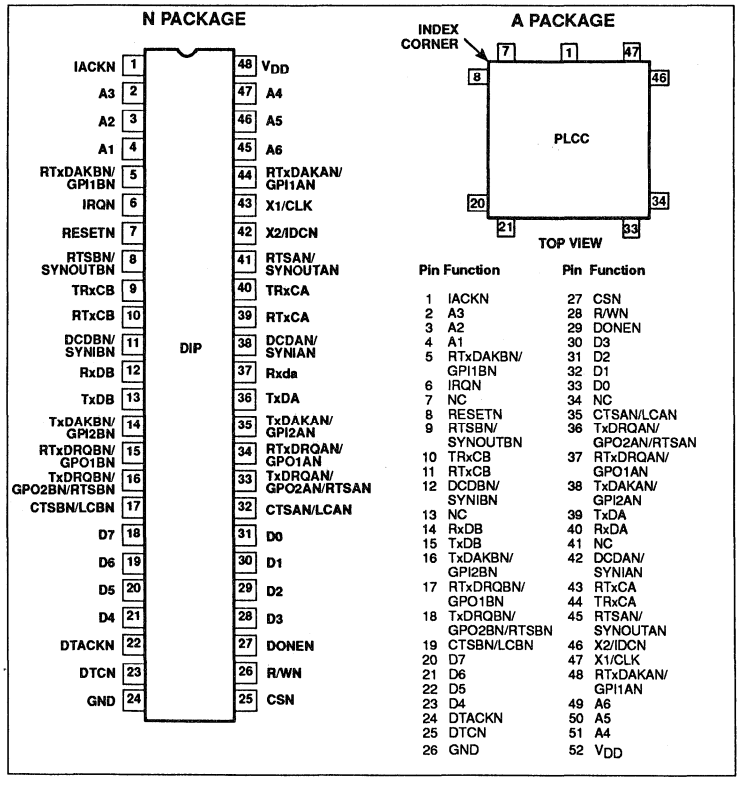
The Signetics SCN68562 Dual Universal Serial Communications Controller (DUSCC) is a single-chip MOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SCN68562 interfaces to the 68000 MPUs via asynchronous bus control signals and is capable of program-polled, interrupt driven, block-move or DMA data transfers. The operating mode and data format of each channel can be programmed independently.

Each channel consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides 16 common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock, making the DUSCC well suited for dual-speed channel applications. Data rates up to 4Mbits per second are supported.

The transmitter and receiver each contain a four-deep FIFO with appended transmitter command and receiver status bits and a shift register. This permits reading and writing of up to four characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

Two modem control inputs (DCD and CTS) and three modem control outputs are provided. These inputs and outputs can be optionally programmed for other functions.

PIN CONFIGURATIONS



Pin	Function	Pin	Function
1	IACKN	27	CSN
2	A3	28	R/WN
3	A2	29	DONEN
4	A1	30	D3
5	RTxDAKBN/ GPI1BN	31	D2
		32	D1
6	IRQN	33	D0
7	NC	34	NC
8	RESETN	35	CTSAN/LCAN
9	RTSBN/ SYNOUTBN	36	TxDRQAN/ GPO2AN/RTSAN
10	TRxCB	37	RTxDRQAN/ GPO1AN
11	RTxCB	38	TxDAKAN/ GPI2AN
12	DCDBN/ SYNIBN	39	TxDA
13	NC	40	RxDA
14	RxDB	41	NC
15	TxDB	42	DCDAN/ SYNIAN
16	TxDAKBN/ GPI2BN	43	RTxCA
17	RTxDRQBN/ GPO1BN	44	TRxCA
18	TxDRQBN/ GPO2BN/RTSBN	45	RTSAN/ SYNOUTAN
19	CTSBN/LCBN	46	X2/IDCN
20	D7	47	X1/CLK
21	D6	48	RTxDAKAN/ GPI1AN
22	D5	49	A6
23	D4	50	A5
24	DTACKN	51	A4
25	DTCN	52	VDD
26	GND		

FEATURES

General Features

- Dual full-duplex synchronous/ asynchronous receiver and transmitter
- Multiprotocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
  - COP: BISYNC, DDCMP
  - ASYNC: 5–8 bits plus optional parity
- Four character receiver and transmitter FIFOs
- 0 to 4MHz data rate
- Programmable bit rate for each receiver and transmitter selectable from:
  - 16 fixed rates: 50 to 38.4k baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
  - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- and half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Compatible with the Signetics SCB68430 Direct Memory Access Interface (DMAI) and other DMA controllers
  - Single- or dual-address dual transfers
  - Half- or full-duplex operation
  - Automatic frame termination on counter/timer terminal count or DMA DONE
- Interrupt capabilities
  - Daisy chain option
  - Vector output (fixed or modified by status)
  - Programmable internal priorities
  - Maskable interrupt conditions
- Multi-function programmable 16-bit counter/timer
  - Bit rate generator

  - Event counter
  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general I/O pins per channel
  - CTS and DCD programmable autoenables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- 1X or 16X Rx and Tx clock factors
- Parity, overrun, and framing error detection
- False start bit detection
- Start bit search 1/2-bit time after framing error detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmits up to 4Mbs and receive up to 2Mbps data rates

Character-Oriented Protocol Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK linefill on underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun, and underrun error detection

BISYNC Features

  - EBCDIC or ASCII header, text and control messages
  - SYN, DLE stripping
  - EOM (end of message) detection and transmission
  - Auto transparent mode switching
  - Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
  - Control character sequence detection for both transparent and normal text

Bit-Oriented Protocol Features

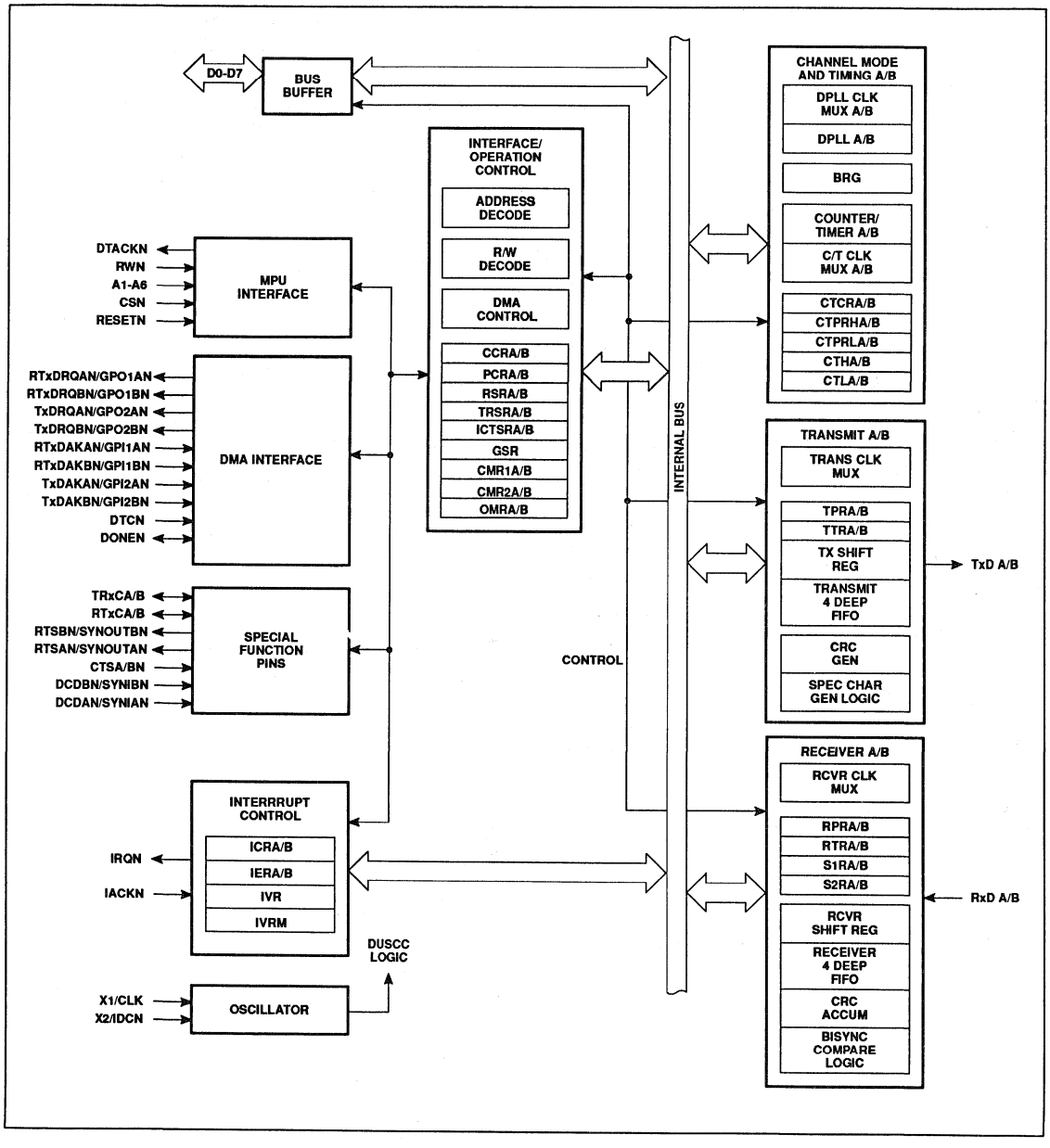
- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Automatic switch to programmed character length for 1 field
- Zero insertion and deletion
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- ABORT, ABORT-FLAGs, or FCS FLAGs linefill on underrun
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±5%, T_A = 0°C to +70°C	
	Serial Data Rate = 2.5Mbps Maximum	**Serial Data Rate = 4Mpbs Maximum**
48-Pin Plastic DIP	SCN68562C2N48	SCN68562C4N48
52-Pin PLCC	SCN68562C2A52	SCN68562C4A52

NOTE: See SCN26562/SCN68562 User's Guide for detailed description of all the features.

BLOCK DIAGRAM



PIN DESCRIPTION

In this data sheet, signals are discussed using the terms 'active' and 'inactive' or 'asserted' and 'negated' independent of whether the signal is active in the High (logic 1) or Low (logic 0) state. N at the end of a pin name signifies the signal associated with the pin is active-Low (see individual pin description for the definition of the active level of each signal.) Pins which are provided for both channels are designated by A/B after the name of the pin and the active-Low state indicator, N, if applicable. A similar method is used for registers provided for both channels: these are designated by either an underline or by A/B after the name.

MNEMONIC	DIP PIN NO.	TYPE	NAME AND FUNCTION
A1 – A6	4-2, 45-47	I	**Address Lines:** Active-High. Address inputs which specify which of the internal registers is accessed for read/write operation.
D0 – D7	31-28, 21-18	I/O	**Bidirectional Data Bus:** Active High, 3-State. Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the DUSCC take place over this bus. The data bus is enabled when CSN is Low, during interrupt acknowledge cycles and single-address DMA acknowledge cycles.
R/WN	26	I	**Read/Write:** A High input indicates a read cycle and a Low input indicates a write cycle when a cycle is initiated by assertion of the CSN input.
CSN	25	I	**Chip Select:** Active-Low input. When Low, data transfers between the CPU and the DUSCC are enabled on D0 – D7 as controlled by the R/WN and A1 – A6 inputs. When CSN is High, the DUSCC is isolated from the data bus (except during interrupt acknowledge cycles and single-address DMA transfers) and D0 – D7 are placed in the 3-State condition.
DTACKN	22	O	**Data Transfer Acknowledge:** Active-Low, 3-State. DTACKN is asserted on a write cycle to indicate that the data on the bus has been latched, and on a read cycle or interrupt acknowledge cycle to indicate valid data is on the bus. The signal is negated when completion of the cycle is indicated by negation of the CSN or IACKN input, and returns to the inactive state (3-State) a short period after it is negated. In a single address DMA mode, data is latched with the falling edge of DTCN. DTACKN is negated when completion of the cycle is indicated by the assertion of DTCN or negation of DMA acknowledge inputs (whichever occurs first), and returns to the inactive state (3-State) a short period after it is negated. When negated, DTACKN becomes an open-drain output and requires an external pull-up resistor.
IRQN	6	O	**Interrupt Request:** Active-Low, open-drain. This output is asserted upon occurrence of any enabled interrupting condition. The CPU can read the general status register to determine the interrupting condition(s), or can respond with an interrupt acknowledge cycle to cause the DUSCC to output an interrupt vector on the data bus.
IACKN	1	I	**Interrupt Acknowledge:** Active-Low. When IACKN is asserted, the DUSCC responds by placing the contents of the interrupt vector register (modified or unmodified by status) on the data bus and asserting DTACKN. If no active interrupt is pending, DTACKN is not asserted.
X1/CLK	43	I	**Crystal or External Clock:** When using the crystal oscillator, the crystal is connected between pins X1 and X2. If a crystal is not used, and external clock is supplied at this input. This clock is used to drive the internal bit rate generator, as an optional input to the counter/timer or DPLL, and to provide other required clocking signals.
X2/IDCN	42	O	**Crystal or Interrupt Daisy Chain:** When a crystal is used as the timing source, the crystal is connected between pins X1 and X2. This pin can be programmed to provide and interrupt daisy chain active-Low output which propagates the IACKN signal to lower priority devices, if no active interrupt is pending. This pin should be grounded when an external clock is used on X1 and X2, is not used as an interrupt daisy chain output.
RESETN	7	I	**Master Reset:** Active-Low. A low on this pin resets the transmitters and receivers and resets the registers shown in Table 1. Reset in asynchronous, i.e., no clock is required.
RxDA, RxDB	37, 12	I	**Channel A (B) Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified for the channel, the input is sampled on the rising edge of the clock.
TxDA, TxDB	36, 13	O	**Channel A (B) Transmitter Serial Data Output:** The least signifiicant bit is transmitted first. This output is held in the marking (High) condition when the transmitter is disabled or when the channel is operating in local loopback mode. If external transmitter clock is specified for the channel, the data is shifted on the falling edge of the clock.
RTxCA, RTxCB	39, 10	I/O	**Channel A (B) Receiver/Transmitter Clock:** As an input, it can be programmed to supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, can supply the counter/timer output, the transmitter shift clock (1X), or the receiver sampling clock (1X). The maximum external receiver/transmitter clock frequency is 4MHz.

PIN DESCRIPTION (Continued)

MNEMONIC	DIP PIN NO.	TYPE	NAME AND FUNCTION
TRxCA, TRxCB	40, 9	I/O	**Channel A (B) Transmitter/Receiver Clock:** As an input, it can supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the DPLL output, the transmitter shift clock (1X), the receiver sampling clock (1X), the transmitter BRG clock (16X), The receiver BRG clock (16X), or the internal system clock (X1/2). The maximum external receiver/transmitter clock frequency is 4MHz.
CTSA/BN, LCA/BN	32, 17	I/O	**Channel A (B) Clear-To-Send Input or Loop Control Output:** Active-Low. The signal can be programmed to act as an enable for the transmitter when not in loop mode. The DUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. When operating in the COP loop mode, this pin becomes a loop control output which is asserted and negated by DUSCC commands. This output provides the means of controlling external loop interface hardware to go on-line and off-line without disturbing operation of the loop.
DCDA/BN, SYNIA/BN	38, 11	I	**Channel A (B) Data Carrier Detected or External Sync Input:** The function of this pin is programmable. As a DCD active-Low input, it acts as an enable for the receiver or can be used as a general purpose input for the DCD function, the DUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. As an active-Low external sync input, it is used in COP modes to obtain character synchronization without receipt of a SYN character. This mode can be used in disc or tape controller applications or for the optional byte timing lead in X.21.
RTxDRQA/BN, GPO1A/BN	34, 15	O	**Channel A (B) Receiver/Transmitter DMA Service Request or General Purpose Output:** Active-Low. For half-duplex DMA operation, this output indicates to the DMA controller that one or more characters are available in the receiver FIFO (when the receiver is enabled) or that the transmit FIFO is not full (when the transmitter is enabled). For full-duplex DMA operation, this output indicates to the DMA controller that data is available in the receiver FIFO. In non-DMA mode, this pin is a general purpose output that can be asserted and negated under program control.
TxDRQA/BN, GPO2A/BN, RTSA/BN	33, 16	O	**Channel A (B) Transmitter DMA Service Request, General Purpose Output, or Request-to-Send:** Active-Low. For full-duplex DMA operation, this output indicates to the DMA controller that the transmit FIFO is not full and can accept more data. When not in full-duplex DMA mode, this pin can be programmed as a general purpose or a Request-to-Send output, which can be asserted and negated under program control (see Detailed Operation).
RTxDAKA/BN, GPI1A/BN	44, 5	I	**Channel A (B) Receiver/Transmitter DMA Acknowledge or General Purpose Input:** Active-Low. For half-duplex single address DMA operation, this input indicates to the DUSCC that the DMA controller has acquired the bus and that the requested bus cycle (read receiver FIFO or load transmitter FIFO) is beginning. For full-duplex single address DMA operation, this input indicates to the DUSCC that the DMA controller has acquired the bus and that the requested read receiver FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in single address DMA mode.
TxDAKA/BN, GP12A/BN	35, 14	I	**Channel A (B) Transmitter DMA Acknowledge or General Purpose Input:** Active-Low. When the channel is programmed for full-duplex single address DMA operation, this input is asserted to indicate to the DUSCC that the DMA controller has acquired the bus and that the requested load transmitter FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in full-duplex single address DMA mode.
DTCN	23	I	**Device Transfer Complete:** Active-Low. DTCN is asserted by the DMA controller to indicate that the requested data transfer is complete.
DONEN	27	I/O	**Done:** Active-Low, open-drain. See Detailed Operation for a description of the function of this pin.
RTSA/BN, SYNOUTA/BN	41, 8	O	**Channel A (B) Sync Detect or Request-to-Send:** Active-Low. If programmed as a sync output, it is asserted one bit time after the specified sync character (COP or BISYNC modes) or a FLAG (BOP modes) is detected by the receiver. As a Request-to-Send modem control signal, it functions as described previously for the TxDRQN/RTSN pin.
V_{DD}	48	I	+5V ± 10% power input.
GND	24	I	Signal and power ground input.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature[2]	0 to +70	°C
T_{STG}	Storage Temperature	-65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	-0.5 to +7.0	V
V_S	Voltage from any pin to ground[3]	-0.5 to V_{CC} +0.5	V

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 40°C/W for plastic DIP and 42°C/W for PLCC.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

DC ELECTRICAL CHARACTERISTICS[1, 4]

T_A = 0 to +70°C, V_{CC} = 5.0V ± 5%

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage:					
	All except X1/CLK				0.8	V
	X1/CLK				0.4	V
V_{IH}	Input high voltage:					
	All except X1/CLK		2.0			V
	X1/CLK		2.4		V_{CC}	V
V_{OL}	Output low voltage:					
	All except IRQN, DONEN	I_{OL} = 5.3mA			0.5	V
	IRQN, DONEN	I_{OL} = 8.8mA			0.5	V
V_{OH}	Output high voltage: (Except open drain outputs)	I_{OH} = -400µA	2.4			V
I_{ILX1}	X1/CLK input low current[3]	V_{IN} = 0, X2 = GND	-5.5		0.0	mA
I_{IHX1}	X1/CLK input high current[3]	V_{IN} = V_{CC}, X2 = GND			1.0	mA
I_{ILX2}	X2 input low current[3]	V_{IN} = 0, X1 = open	-100			µA
I_{IHX2}	X2 input high current[3]	V_{IN} = V_{CC}, X1 = open			100	µA
I_{IL}	Input low current DTCN, TxDAKA/BN, RTxDAKA/BN	V_{IN} = 0	-40			µA
I_L	Input leakage current	V_{IN} = 0 to V_{CC}	-5		5	µA
I_{OZH}	Output off current high, 3-State data bus	V_{IN} = V_{CC}			5	µA
I_{OZL}	Output off current low, 3-State data bus	V_{IN} = 0	-5			µA
I^{ODL}	Open drain output low current in off	V_{IN} = 0				
	state: DONEN		-120		-25	µA
	IRQN, DTACKN		-5			µA
I_{ODH}	Open drain output high current in off	V_{IN} = V_{CC}				
	state: DONEN, IRQN, DTACKN				5	µA
I_{CC}	Power supply current	V_O = 0 to V_{CC}			275	mA
C_{IN}	Input capacitance[2]	V_{CC} = GND = 0			10	pF
C_{OUT}	Output capacitance[2]	V_{CC} = GND = 0			15	pF
$C_{I/O}$	Input/output capacitance[2]	V_{CC} = GND = 0			20	pF

NOTES:
1. Parameters are valid over specified temperature and voltage range.
2. These values were not explicitly tested; they are guaranteed by design and characterization data.
3. X1/CLK and X2 are not tested with a crystal installed.
4. This specification applies to revision D, revision E and later revisions.

AC ELECTRICAL CHARACTERISTICS[1, 2, 3, 4] T_A = -55 to +110°c, V_{CC} = 5V ± 10%

NO.	FIGURE	PARAMETER	LIMITS Min	Typ	Max	UNIT
1	1	RESETN pulse width	1.2			µS
2	2,4	A1 - A6 set-up time to CSN Low	10			nS
3	2,4	A1 - A6 hold time from CSN High	0			nS
4	2,4	RWN set-up time to CSN Low	0			nS
5	2,4	RWN hold time to CSN High	0			nS
6	2,4	CSN High pulse width[4]	160			nS
7	2,5	CSN or IACKN High from DTACKN Low	30			nS
7A	5	IACKN High to DTACKN High			200	nS
8	2,5	Data valid from CSN or IACKN Low			300	nS
9	2	Data bus floating from CSN High[7]			100	nS
10	4	Data hold time from DTACKN Low[5]	0			nS
11	2,4	DTACKN Low from read data ready	0			nS
12	2,4	DTACKN Low from CSN Low			560	nS
12A	4	CSN Low to write data valid			50	nS
13	2,4	DTACKN High from CSN High			150	nS
14	2,4	DTACKN high impedance from CSN High			185	nS
15	5	DTACKN Low from IACKN Low			550	nS
16	6	GPI input set-up time to CSN Low	20			nS
17	6	GPI input hold time from CSN Low	100			nS
18	6	GPO output valid from DTACKN Low			300	nS
19	7	IRQN High from:				
		Read RxFIFO (RxRDY interrupt)			450	nS
		Write TxFIFO (TxRDY interrupt)[8]			450	nS
		Write RSR (Rx condition interrupt)[8]			400	nS
		Write TRSR (Rx/Tx interrupt)[8]			400	nS
		Write ICTSR (port change and CT int.)[8]			400	nS
20	8	X1/CLK High or Low time	25			nS
		X1/CLK frequency	2.0	14.745	16	MHz
		CTCLK High or Low time	100	6		nS
		CTCLK frequency	0		4	MHz
		RxC High or Low time	110			nS
		RxC frequency (16X or 1X)[9]	0		4	MHz
		TxC High or Low time	110			nS
		TxC frequency (16X or 1X)	0		4	MHz
21	9	TxD output from TxC input Low (1X)			240	nS
		(16X)			435	nS
22	9	TxD output from TxC output Low			50	nS
23	10	RxD data set-up time to RxC High	50			nS
24	10	RxD data hold time from RxC High	50			nS
25	11	IACKN Low to daisy chain Low			200	nS
26	13	Data valid from receive DMA ACKN			300	nS
27	12,13	DTCN width	100			nS
28	12,13	RDYN Low to DTCN Low	80			nS
29	13	Data bus float from DTCN Low[7]			200	nS
30	12,13	DMA ACKN Low to RDYN (DTACKN) Low			360	nS
31	12,13	RDYN High from DTCN Low			230	nS
32	12,13	RDYN High impedance from DTCN Low			250	nS
33	13	Receive DMA REQN High from DMA ACKN Low			325	nS
34	13	Receive DMA ACKN width	150			nS
35	12,13	Receive DMA ACKN Low to DONEN Low			250	nS
36	12	Data set-up to DTCN Low	50			nS
37	12	Data hold from DTCN Low[6]	50			nS
38	12	Transmit DMA REQN High from ACKN Low			340	nS
39	12	Transmit DMA ACKN width	150			nS
40	12	Transmit DMA ACKN Low to DONEN Low output			250	nS
40A	12	DTCN Low DONEN output High			260	nS
41	14	CSN Low to transmit DONEN Low output			300	nS
42	14	CSN Low to transmit DMA REQ negated			400	nS
43	14	CSN Low to receive DONEN Low			300	nS
44	14	CSN Low to receive DMA REQ negated			400	nS

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For DC and functional testing, all inputs except X1/CLK swing between 0.8V and 2.0V with a transition time of 20ns maximum. For X1/CLK, this swing is between 0.4V and 2.4V All time measurements are referenced at input voltages of 0.4V and 2.4V for all inputs. Output levels are referenced at 1.2V and 2.0V, as appropriate.
3. Test conditions for outputs: C_L = 150pF, except open-drain outputs. Test condition for open-drain outputs: C_L = 50pF to GND, R_L = 2.7kΩ to V_{CC} except DTACKN whose R_L = 820Ω to V_{CC} and C_L = 150pF to GND and DONEN which requires C_L = 50pF to GND and R_L = 1kΩ to V_{CC}.
4. This specification will impose maximum 68000 CPU CLK to 6MHz. Higher CPU CLK can be used if repeating bus cycles are not performed.
5. Execution of the valid command (after it is latched) requires three falling edges of X1 (see Figure 14).
6. In single address DMA mode write operation, data is latched by the falling edge of DTCN.
7. These values were not explicitly tested, they are guaranteed by design and characterization data.
8. These timings are from the falling edge of DTACKN (not CSN rising).
9. X1/CLK frequency must be at least four times the receiver serial data rate.

REGISTERS

The addressable registers of the DUSCC are shown in Table 1. The following rules apply to all registers:

1. A read from a reserved location in the map results in a read from the 'null register'. The null register returns all ones for data and results in a normal bus cycle. A write to one of these locations results in a normal bus cycle without a write being performed.
2. Unused bits of a defined register are read as zeros, unless ones have been loaded after master reset.
3. Bits that are unused in the chosen mode but are used in others are readable and writable but their contents are ignored in the chosen mode.
4. All registers are addressable as 8-bit quantities. To facilitate operation with the 68000 MOVEP instruction, addresses are ordered such that certain sets of registers may also be accessed as words or long words.

The operation of the DUSCC is programmmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The contents of certain control registers are initialized on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems, e.g., changing the channel mode at an inappropriate time may cause the reception or transmission of an incorrect character. In general, the contents of registers which control transmitter or receiver operation, or the counter/timer, should be changed only when they are not enabled.

The DUSCC registers can be separated into five groups to facilitate their usage:

1. Channel mode configuration and pin description registers.
2. Transmitter and receiver parameter and timing registers.
3. Counter/timer control and value registers.
4. Interrupt control and status registers.
5. Command register.

This arrangement is used in the following description of the DUSCC registers.

Table 1. DUSCC Register Address Map

ADDRESS BITS* 6 5 4 3 2 1	ACRONYM	REGSITER NAME	MODE	AFFECTED BY RESET
c 0 0 0 0 0	CMR1	Channel Mode Register 1	R/W	Yes—00
c 0 0 0 0 1	CMR2	Channel Mode Register 2	R/W	Yes—00
c 0 0 0 1 0	S1R	SYN 1/Secondary Address 1 Register	R/W	No
c 0 0 0 1 1	S2R	SYN 2/Secondary Address 2 Register	R/W	No
c 0 0 1 0 0	TPR	Transmitter Parameter Register	R/W	Yes—00
c 0 0 1 0 1	TTR	Transmitter Timing Register	R/W	No
c 0 0 1 1 0	RPR	Receiver Parameter Register	R/W	Yes—00
c 0 0 1 1 1	RTR	Receiver Timing Register	R/W	No
c 0 1 0 0 0	CTPRH	Counter/Timer Preset Register High	R/W	No
c 0 1 0 0 1	CTPRL	Counter/Timer Preset Register Low	R/W	No
c 0 1 0 1 0	CTCR	Counter/Timer Control Register	R/W	Yes—00
c 0 1 0 1 1	OMR	Output and Miscellaneous Register	R/W	Yes—00
c 0 1 1 0 0	CTH	Counter/Timer High	R	No
c 0 1 1 0 1	CTL	Counter/Timer Low	R	No
c 0 1 1 1 0	PCR	Pin Configuration Register	R/W	Yes—00
c 0 1 1 1 1	CCR	Channel Command Register	R/W	No
c 1 0 0 X X	TxFIFO	Transmitter FIFO	W	No
c 1 0 1 X X	RxFIFO	Receiver FIFO	R	No
c 1 1 0 0 0	RSR	Receiver Status Register	R/W**	Yes—00
c 1 1 0 0 1	TRSR	Transmitter and Receiver Status Register	R/W**	Yes—00
c 1 1 0 1 0	ICTSR	Input and Counter/TImer Status Register	R/W**	Yes
d 1 1 0 1 1	GSR	General Status Register	R/W**	Yes—00
c 1 1 1 0 0	IER	Interrupt Enable Register	R/W	Yes—00
c 1 1 1 0 1		Not used		
0 1 1 1 1 0	IVR	Interrupt Vector Register— Unmodified	R/W	Yes—0F
1 1 1 1 1 0	IVRM	Interrupt Vector Register— Modified	R	Yes—0F
0 1 1 1 1 1	ICR	Interrupt Control Register	R/W	Yes—00
1 1 1 1 1 1		Not used		

NOTES:

* c = 0 for Channel A, c = 1 for Channel B.
d = don't care — register may be accessed as either channel.
x = don't care — FIFOs are addressable at any of four adjacent addresses to allow them to be addressed as byte/word/long word with the 68000 MOVEP instruction.

** A write to this register may perform a status resetting operation.

Table 2. Channel Configuration/Pin Definition Registers Bit Formats

CHANNEL MODE REGISTER 1

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	Data Encoding		Extended Control	Address Mode (BOP)		Channel Protocol Mode		
(CMR1A, CMR1B)	00 — NRZ/Manchester 01 — NRZI 10 — FM0 11 — FM1		BOP only 0 — no 1 — yes	00 — 8-bit 01 — extended address 10 — 16-bit 11 — 16-bit w/group		000 — BOP primary 001 — BOP secondary 010 — BOP loop 011 — BOP loop – no adr. comp.		
			Parity*	Parity Mode (COP/ASYNC)				
			0 — even 1 — odd	00 — no parity 01 — reserved 10 — with parity 11 — force parity		100 — COP dual SYN 101 — COP dual SYN (BISYNC) 110 — COP single SYN 111 — asynchronous		

NOTE:

* In BISYNC protocol mode, 0 = EBCDIC, 1 = ASCII coding.

Table 2. Channel Configuration/Pin Definition Registers Bit Formats (Continued)

CHANNEL MODE REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	Channel Connection		**Data Transfer Interface**			**Frame Check Sequence Select**		
(CMR2A, CMR2B)	00 — normal 01 — auto echo 10 — local loop 11 — reserved		000 — half-duplex single address DMA 001 — half-duplex dual address DMA 010 — full-duplex single address DMA 011 — full-duplex dual address DMA 100 — wait on Rx only 101 — wait on Tx only 110 — wait on Rx or Tx 111 — polled or interrupt			000 — none 001 — reserved 010 — LRC8 preset 0s 011 — LRC8 preset 1s 100 — CRC 16 preset 0s 101 — CRC 16 preset 1s 110 — CRC CCITT preset 0s 111 — CRC CCITT preset 1s		

SYN1/SECONDARY ADDRESS REGISTER 1

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(S1RA, S1RB)	ASYNC — Character compare (5 – 8 bits) COP — SYN1 (5 – 8 bits) BOP — First address octet							

SYN2/SECONDARY ADDRESS REGISTER 2

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(S2RA, S2RB)	ASYNC — not used COP — SYN2 (5 – 8 bits) BOP — Second address octet							

PIN CONFIGURATION REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	X2/IDS	**GPO2/RTS**	**SYNOUT/RTS**	**RTxC Pin**		**TRxC Pin**		
(PCRA, PCRB)	* 0 — X2 1 — IDC	0 — GPO2 1 — RTS	0 — SYNOUT 1 — RTS	00 — input 01 — C/T 10 — TxCLK 1X 11 — RxCLK 1X		000 — input 001 — XTAL/2 010 — DPLL 011 — C/T	100 — TxCLK 16X 101 — RxCLK 16X 110 — TxCLK 1X 111 — RxCLK 1X	

NOTE:
* PCRA only. Not used in PCRB.

Table 3. Transmitter and Receiver Parameter and Timing Register Bit Format

TRANSMITTER PARAMETER REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(TPRA, TPRB)	Underrun Control		Idle	TEOM on Zero Cnt or Done	Tx RTS Control	CTS Enable Tx	Tx Character Length	
COP	00 — FCS-idle 01 — reserved 10 — MARKs 11 — SYNs		0 — MARKs 1 — SYNs	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	00 — 5 bits 01 — 6 bits 10 — 7 bits 11 — 8 bits	
	Underrun Control		Idle	TEOM on Zero Cnt or Done				
BOP	00 — FCS-FLAG-idle 01 — reserved 10 — ABORT-MARKs 11 — ABORT-FLAGs		0 — MARKs 1 — FLAGs	0 — no 1 — yes				
	Stop Bits Per Character							
ASYNC	9/16 to 1, 17/16 to 1.5, 25/16 to 2 programmable in 1/16-bit increments (See Table 4)							

TRANSMITTER TIMING REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(TTRA, TTRB)	External Source	Transmitter Clock Select			Bit Rate Select			
	0 — RTxC 1 — TRxC	000 — 1X external 001 — 16X external 010 — DPLL 011 — BRG 100 — 2X other channel C/T 101 — 32X other channel C/T 110 — 2X own channel C/T 111 — 32X own channel C/T			one of sixteen rates from BRG (See Table 5)			

RECEIVER PARAMETER REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(RPRA, RPRB)	not used	not used	not used	Rx RTS Control	Strip Parity	DCD Enable Rx	Rx Character Length	
ASYNC				0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	00 — 5 bits 01 — 6 bits	
COP	SYN Strip	FCS to FIFO	Auto Hunt & Pad Chk	Ext Sync	Strip Parity		10 — 7 bits 11 — 8 bits	
	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes			
	not used	FCS to FIFO	Overrun Mode	not used	All Parity Address			
BOP		0 — no 1 — yes	0 — hunt 1 — cont		0 — no 1 — yes			

Table 3. Transmitter and Receiver Parameter and Timing Register Bit Format (Continued)

RECEIVER TIMING REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(RTRA, RTRB)	External Source	Receiver Clock Select			Bit Rate Select			
	0 — RTxC 1 — TRxC	000 — 1X external 001 — 16X external 010 — BRG 011 — C/T of channel 100 — DPLL, source = 64X X1/CLK 101 — DPLL, source = 32X External 110 — DPLL, source = 32X BRG 111 — DPLL, source = 32X C/T			ASYNC protocol mode only	one of sixteen rates from BRG (See Table 5)			

OUTPUT AND MISC REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(OMRA, OMRB)	Tx Residual Character Length			TxRDY Activate	RxRDY Activate	OUT 2	OUT 1	RTS
	000 — 1 bit 001 — 2 bits 010 — 3 bits 011 — 4 bits 100 — 5 bits 101 — 6 bits 110 — 7 bits 111 — same as TPR[1:0]			0 — FIFO not full 1 — FIFO empty	0 — FIFO not empty 1 — FIFO full	Bit Pin 0 — H 1 — L	Bit Pin 0 — H 1 — L	Bit Pin 0 — H 1 — L

Table 4. Stop Bits — Transmitted Character

[7:4]	5 BITS/ CHAR	6, 7 or 8 BITS/CHAR
0000	1.063	0.563
0001	1.125	0.625
0010	1.188	0.688
0011	1.250	0.750
0100	1.313	0.813
0101	1.375	0.875
0110	1.438	0.938
0111	1.500	1.000
1000	1.563	1.563
1001	1.625	1.625
1010	1.688	1.688
1011	1.750	1.750
1100	1.813	1.813
1101	1.875	1.875
1110	1.938	1.938
1111	2.000	2.000

Table 5. Receiver/Transmitter Baud Rates

[3:0]	BIT RATE	[3:0]	BIT RATE
0000	50	1000	1050
0001	75	1001	1200
0010	110	1010	2000
0011	134.5	1011	2400
0100	150	1100	4800
0101	200	1101	9600
0110	300	1110	19.2K
0111	600	1111	38.4K

Table 6. Counter/Timer Control and Value Register Bit Formats

COUNTER/TIMER CONTROL REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(CTCRA, CTCRB)	Zero Detect Interrupt	Zero Detect Control	Output Control	Prescaler		Clock Source		
	0 — disable 1 — enabled	0 — preset 1 — continue	0 — square 1 — pulse	00 — 1 01 — 16 10 — 32 11 — 64		000 — RTxC pin 001 — TRxC pin 010 — X1/CLK divided by 4 011 — X1/CLK divided by 4 gated by RxD 100 — Rx BRG 101 — Tx BRG 110 — Rx characters 111 — Tx characters		

COUNTER/TIMER PRESET REGISTER HIGH

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(CTPRHA, CTPRHB)	Most significant bits of counter/timer preset value.							

COUNTER/TIMER PRESET REGISTER LOW

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(CTPRLA, CTPRLB)	Least significant bits of counter/timer preset value.							

COUNTER/TIMER REGISTER HIGH

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(CTHA, CTHB)	Most significant bits of counter/timer.							

COUNTER/TIMER REGISTER LOW

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(CTLA, CTLB)	Least significant bits of counter/timer.							

Table 7. Interrupt Control and Status Register Bit Format

RECEIVER STATUS REGISTER

	*BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(RSRA, RSRB) ASYNC	# Char compare	RTS negated	Overrun error	not used	BRK end detect	BRK start detect	# Framing error	# Parity error
COP	# EOM detect +	PAD error +	Overrun error	not used	not used	Syn detect	# CRC error	# Parity error
BOP	# EOM detect	Abort detect	Overrun error	Short frame detect	Idle detect	Flag detect	# CRC error	# RCL not zero
LOOP	# EOM detect	Abort/EOP detect	Overrun error	Short frame detect	Turn-around detect	Flag detect	# CRC error	# RCL not zero

NOTES:
Status bit is FIFOed.
+ COP BISYNC mode only
* All modes indicate character count complete.

Table 7. Interrupt Control and Status Register Bit Format (Continued)

TRANSMITTER AND RECEIVER STATUS REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(TRSRA, TRSRB) ASYNC	Transmitter empty	CTS underrun	not used	Send break ack	DPLL error	not used	not used	not used
COP	Transmitter empty	CTS underrun	Frame complete	Send SOM ack	DPLL error	not used	Rx hunt mode	Rx xpnt mode
BOP	Transmitter empty	CTS underrun	Frame complete	Send SOM/ abort ack	DPLL error	Rx Residual Character Length		
		Loop sending*				000 — 0 bit 001 — 1 bits 010 — 2 bits 011 — 3 bits	100 — 4 bits 101 — 5 bits 110 — 6 bits 111 — 7 bits	

NOTE:
* Loop mode only.

INPUT AND COUNTER/TIMER STATUS REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(ICTSRA, ICTSRB)	C/T running	C/T zero count	Delta DCD	Delta CTS/LC	DCD	CTS/LC	GPI2	GPI1

INTERRUPT ENABLE REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(IERA, IERB)	DCD/CTS	TxRDY	TRSR [7:3]	RxRDY	RSR[7:6]	RSR [5:4]	RSR [3:2]	RSR [1:0]
	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes

INTERRUPT VECTOR REGISTER AND INTERRUPT VECTOR MODIFIED REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(IVR, IVRM)	8-bit interrupt vector							

GENERAL STATUS REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(GSR)	Channel B				Channel A			
	External or C/T Status	Rx/Tx status	TxRDY	RxRDY	External or C/T status	Rx/Tx status	TxRDY	RxRDY

INTERRUPT CONTROL REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(ICR)	Channel A/B Interrupt Priority		Vector Mode		Bits to Modify	Vector Includes Status	Channel A Master Int Enable	Channel B Master Int Enable
	00 — Channel A 01 — Channel B 10 — interleaved A 11 — interleaved B		00 — vectored 01 — vectored 10 — vectored 11 — non vectored		0 — 2:0 1 — 4:2	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes

Table 8. Command Register Bit Format

CHANNEL COMMAND REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(CCRA, CCRB)					**Transmitter Command**			
	00 = Transmitter CMD		don't care	don't care	0000 — reset Tx 0001 — reset TxCRC* 0010 — enable Tx 0011 — disable Tx 0100 — transmit SOM (TSOM) 0101 — transmit SOM with PAD (TSOMP) 0110 — transmit EOM (TEOM)* 0111 — transmit ABORT/BREAK (TABRK) 1000 — transmit DLE (TDLE)* 1001 — go active on poll 1010 — reset go active on poll 1011 — go on-loop 1100 — go off-loop 1101 — exclude form CRC*			
					Receiver Command			
	01 = Receiver CMD		don't care	don't care	0000 — reset Rx 0001 — reserved 0010 — enable Rx 0011 — disable Rx			
					Counter/Timer Command			
	10 = C/T CMD		don't care	don't care	0000 — start 0001 — stop 0010 — preset to FFFF 0011 — preset from CTPRH/CTPRL			
					DPLL Command			
	11 = DPLL CMD		don't care	don't care	oooo — enter search mode 0001 — disable DPLL 0010 — set FM mode 0011 — set NRZI mode 0100 — reserved for test 0101 — reserved for test			

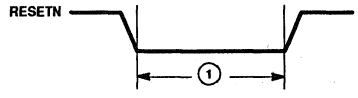


Figure 1. Reset Timing

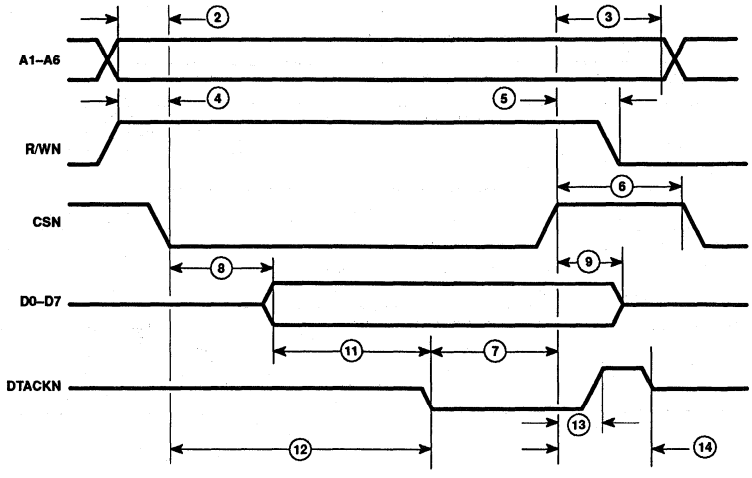


Figure 2. Bus Timing (Read Cycle)

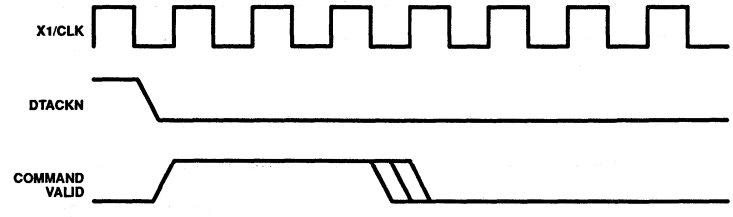


Figure 3. Command Timing

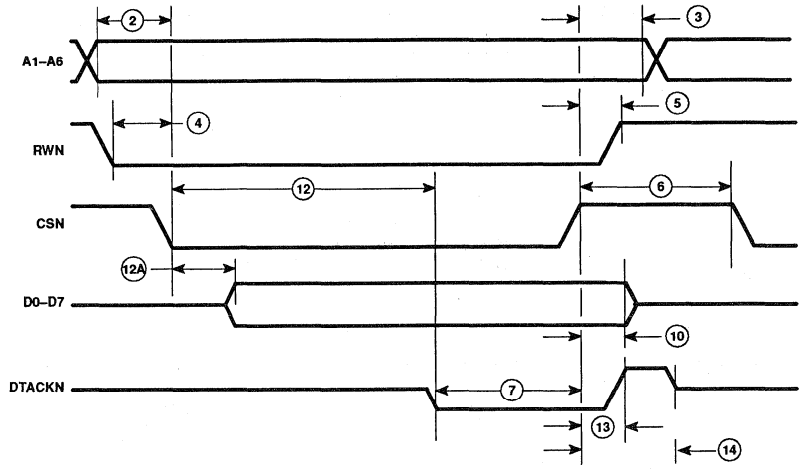


Figure 4. Bus Timing (Write Cycle)

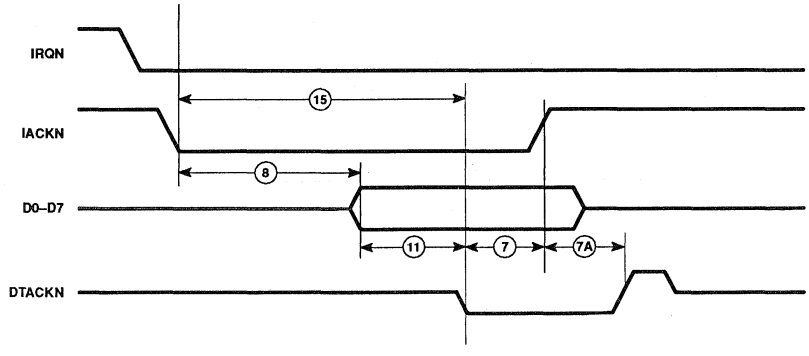


Figure 5. Interrupt Cycle Timing

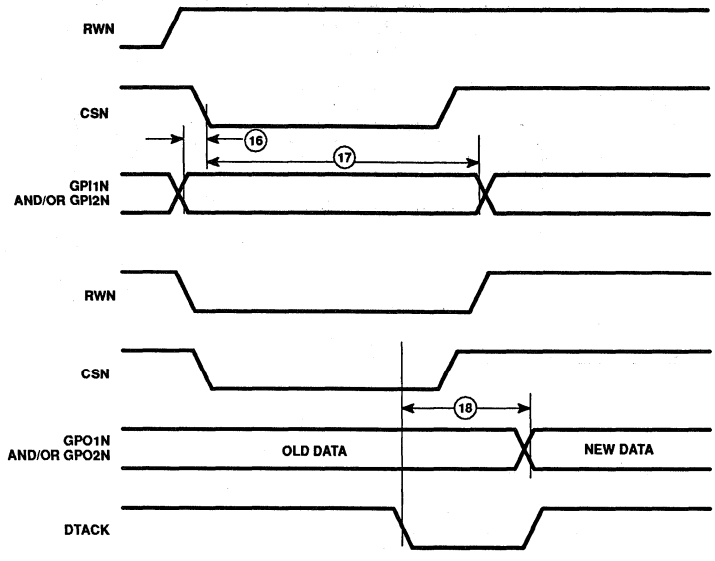


Figure 6. Port Timing

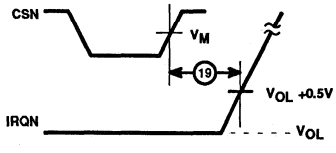


Figure 7. Interrupt Timing

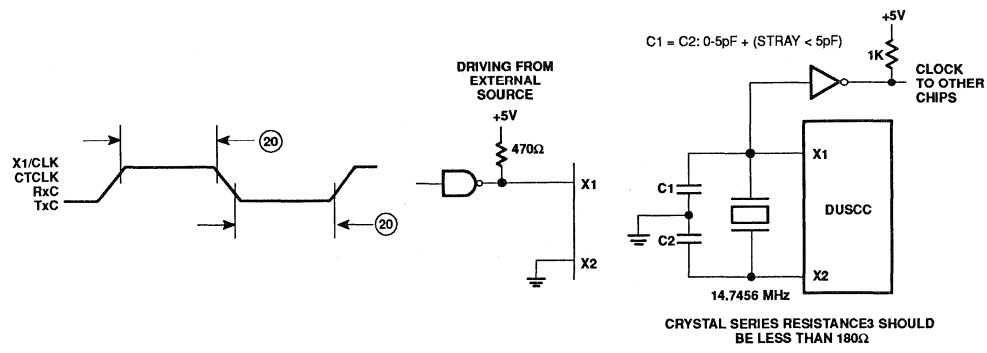


Figure 8. Clock Timing

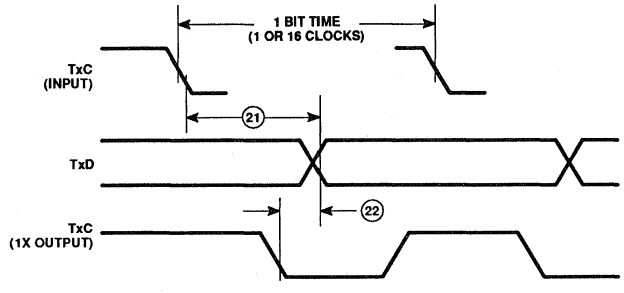


Figure 9. Transmit Timing

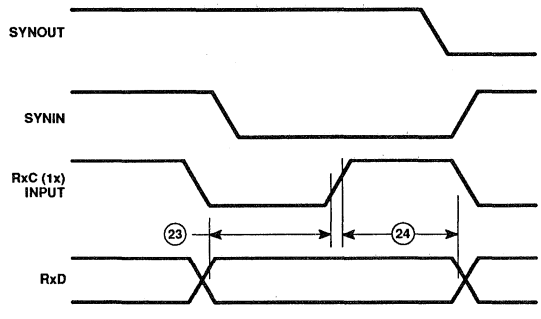


Figure 10. Receive Timing

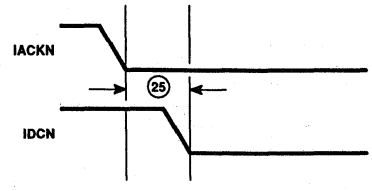


Figure 11. Interrupt Daisy Chain Timing

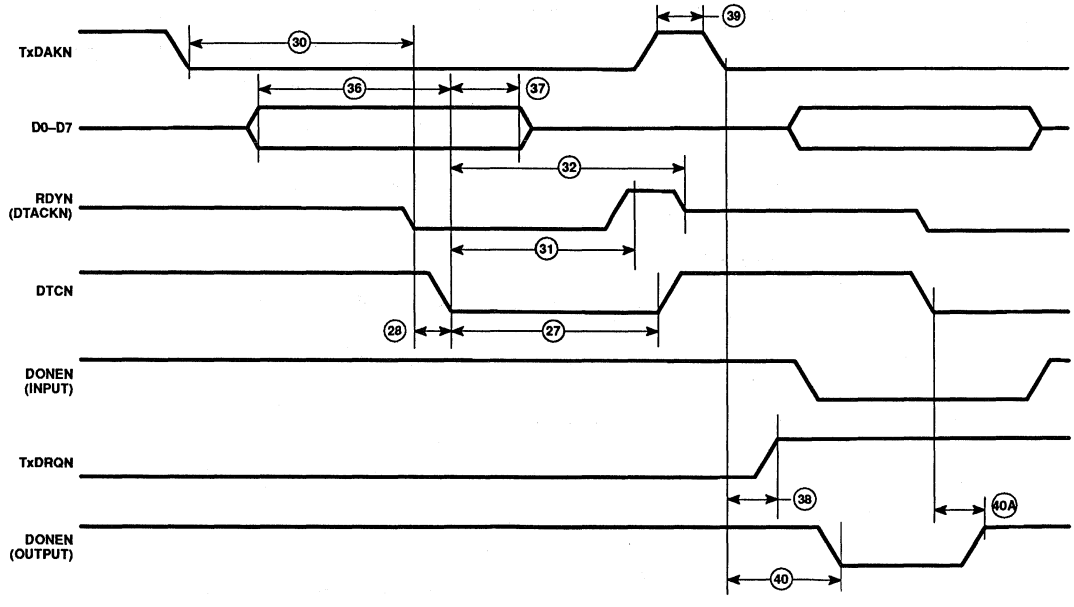


Figure 12. DMA Transmit Write Timing — Single Adress DMA Mode

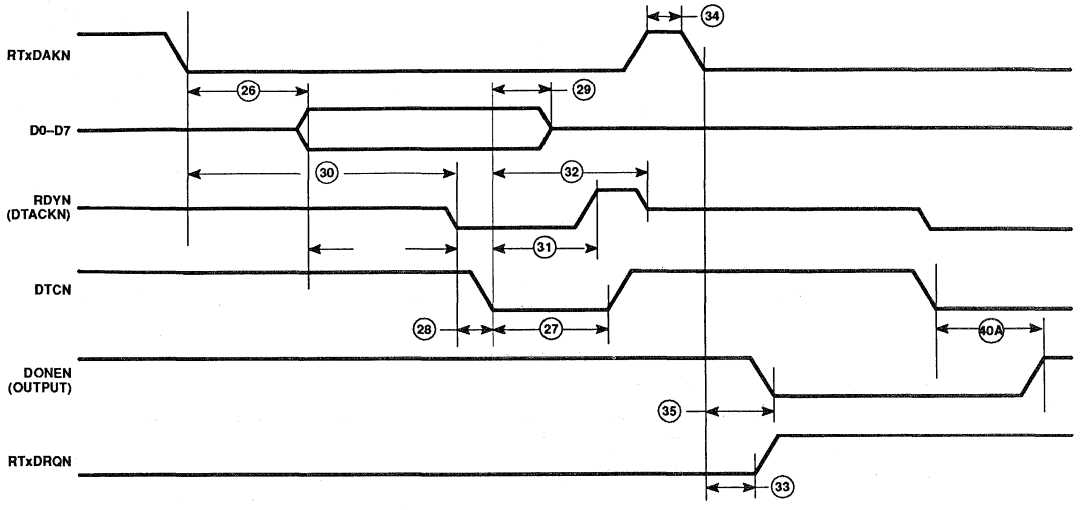


Figure 13. DMA Receive Read Timing — Single Adress DMA Mode

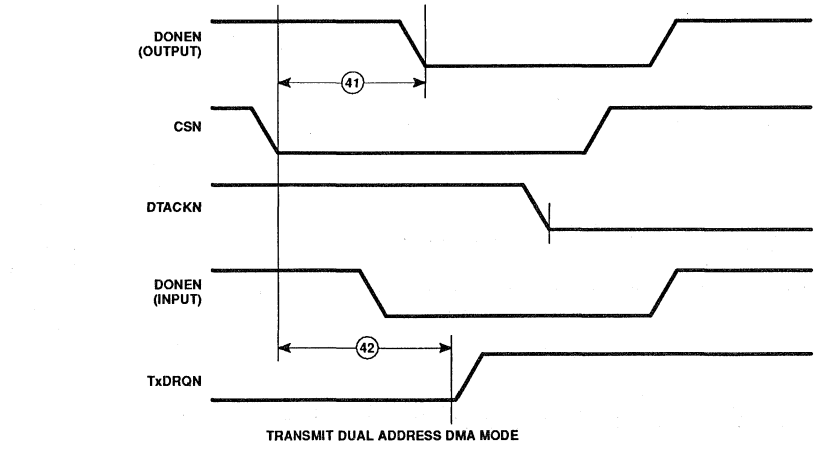


Figure 14. Dual Address DMA Mode Timing

Input/output processor (IOP) SC26C460

DESCRIPTION

The Signetics SC26C460 I/O Processor (IOP) is a co-processor that greatly reduces the CPU overhead required to service a large number of I/O devices. It can inspect, modify or delete the data it transfers. Each channel can have its own channel program, which can branch depending on device status or a data test.

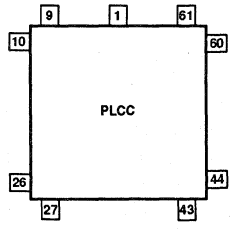
The IOP includes the features of a 32-channel Direct Memory Access (DMA) controller. This helps in handling multi-channel devices such as the Signetics 2698 OCT-ART. It can create a data buffer chain in memory to transfer sequential blocks, greatly reducing the number of times the CPU needs to be interrupted.

The IOP can be attached directly to the system bus, or for higher performance, can support an additional local I/O bus.

FEATURES

- 32 channel DMA processor
- Separate memory address and length for each channel
- Separate I/O device address for each channel
- Separate channel program entry point for each channel
- Programmable to handle virtually all types of peripherals
- Custom instruction set
- Can interpret peripheral status for channel selection, error checking
- Can interpret data characters for buffer termination checking, control sequence transformation
- 8- or 16-bit data transfers
- 24-bit memory addresses: 16Mbyte address space
- 2-level interrupt queue minimizes host microprocessor overhead
- Stores and fetches data similar to Intel processors
- Can transfer multiple blocks without interrupting the CPU
- High-speed CMOS technology
- 68-pin PLCC

PIN CONFIGURATION

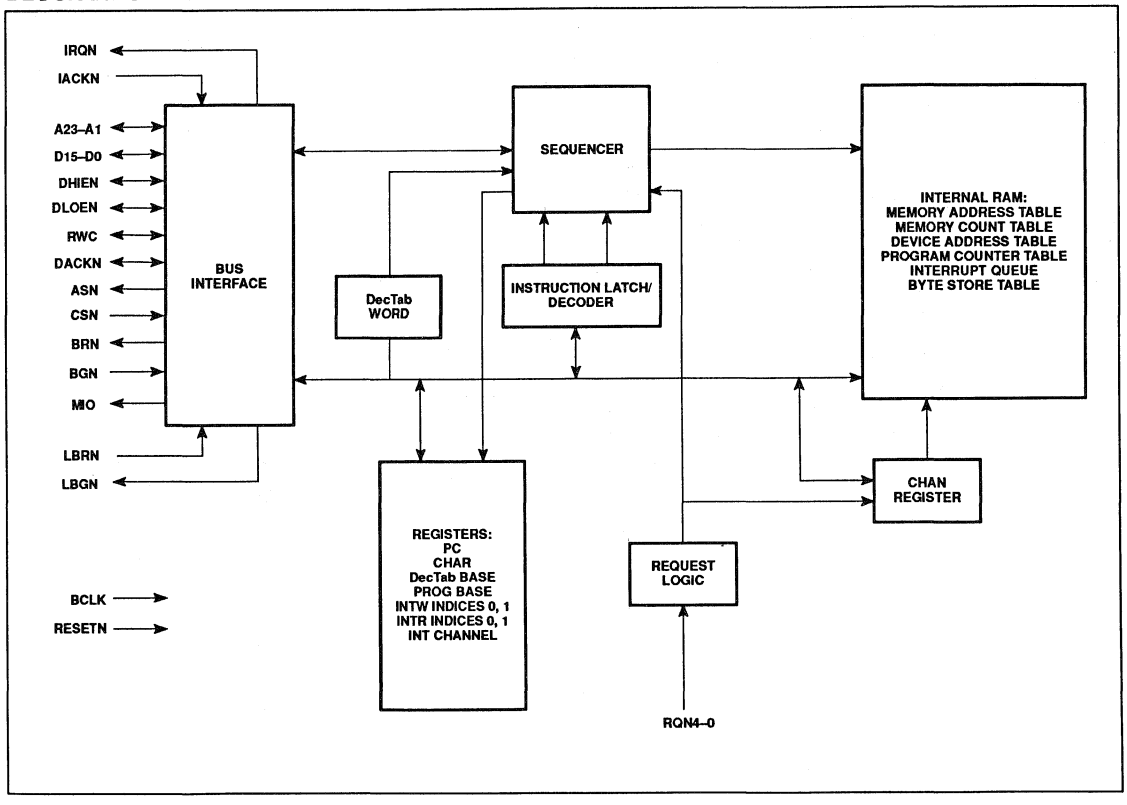


Pin	Function	Pin	Function
1	D10	35	A21
2	D9	36	V_{SS}
3	D8	37	A20
4	D7	38	A19
5	D6	39	A18
6	D5	40	A17
7	D4	41	A16
8	D3	42	A15
9	D2	43	A14
10	D1	44	A13
11	D0	45	A12
12	RQ0N	46	A11
13	RQ1N	47	V_{SS}
14	RQ2N	48	A10
15	RQ3N	49	A9
16	RQ4N	50	A8
17	BRN	51	A7
18	V_{SS}	52	A6
19	V_{CC}	53	V_{SS}
20	BGN	54	V_{CC}
21	LBRN	55	A5
22	IRQN	56	A4
23	IACKN	57	A3
24	CSN	58	A2
25	V_{SS}	59	A1
26	LBGN	60	D15
27	DACKN	61	D14
28	M/IO	62	D13
29	RWC	63	D12
30	DHIEN	64	D11
31	DLOEN	65	V_{SS}
32	ASN	66	BCLK
33	A23	67	RESETN
34	A22	68	V_{CC}

ORDERING INFORMATION

PACKAGE	V_{CC} = 5V ± 10%, T_A = 0°C to 70°C
Plastic PLCC	SC26C460C6A

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
RQ4N–RQ0N	16–12	I	**Request Lines:** A set of active-low inputs from external peripheral devices handled by the IOP. Typically, these will be the "interrupt request" lines from the peripherals. If there are 5 peripheral lines or less, they can be directly connected to these pins. Otherwise, the lines must be externally encoded. The IOP interprets the "all high" state on these lines as "no request". These input request lines are internally synchronized. When the IOP is idle, and it detects the stable active state on these lines on two consecutive falling edges of BCLK, it begins activity for the indicated channel.
CSN	24	I	**Chip Select:** An active-low input indicating that the host MPU is trying to access a register or RAM location on the IOP. CSN is not asserted until all of the signals, A8–A1, DHIEN, DLOEN, and RWC are valid (this eliminates signalling differences among host MPUs). This, in turn, implies that in a system in which IOP has its own "local bus", CSN should be qualified with LBGN.
A23–A1	33–35, 37–46, 48, 49, 50–52, 55–59	O O O I/O I/O	**Address Lines:** When the IOP is a bus master, these lines carry the address to be accessed, which may be in memory or in a peripheral device. When the IOP is a bus slave, A8–A1 selects an internal location in the IOP to be read or written by the host MPU.

PIN DESCRIPTION (Continued)

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
D15–D0	60–64, 1–11	I/O	**Bidirectional Data Bus:** 16-bit data bus for the IOP, memory, peripherals, and the host MPU.
M/IO	28	O	**Memory/Input-Output Control:** When the IOP is a bus master, this tri-state output is driven high to indicate an access to memory, and low to indicate an access to a peripheral device. MIO has the same timing as A23–A1. When the IOP is a bus slave, this output is tri-stated.
ASN	32	O	**Address Strobe:** When the IOP is bus master, this is an output indicating that a transfer cycle is in progress on the bus, and, in particular, that a valid address has been placed on A23–A1. This signal is not driven at other times.
DHIEN, DLOEN	30, 31	I/O	**Data High/Low Enable:** When the IOP is a bus master, these pins are outputs. DHIEN low in a master read cycle indicates that the memory or peripheral selected by A23–A1 should read a byte and place its contents on D15–D8, while DLOEN low has the same meaning for the D7–D0 lines. In a master write cycle, DHIEN (DLOEN) low indicates that the IOP has placed valid data on D15–D8 (D7–D0), and that the memory or peripheral selected by A23–A1 should write the data into the appropriate byte(s). When both signals are low in a master cycle, a 16-bit word should be transferred. When the IOP is not a bus master, these lines are inputs from the host MPU. These two signals are internally ANDed. Either signal goes active, along with CSN active, will cause the IOP to be accessed.
RWC	29	I/O	**Read/Write Control:** When the IOP is a bus master, this output controls the direction of data transfer on D15–D0. On the IOP, this signal is high for a write and low for a read. and corresponds to W/$\overline{R}$ on the 80386 and to $\overline{ST}$ on the 80286. When the IOP is not the current bus master, RWC is an input from the host MPU, with the same meaning.
DACKN	27	I/O	**Data Acknowledge:** When the IOP is a bus master, this is an input signal from memory and peripherals, acknowledging that the requested bus transfer has been completed. When the IOP is a bus slave, this is an open-drain output to the host MPU, with the same meaning. This signal corresponds to $\overline{READY}$ on the 80286 and 80386.
BRN	17	O	**Bus Request:** An active-low output to the host MPU or other bus arbiter, requesting the use of the MPU bus. It must be inverted to produce HOLD in an "Intel" system. BRN is not open-drain because if the host MPU is the arbiter and the IOP is the only other master, a totem-pole output eliminates the need for a pull-up resistor. Also, if there are other masters contending with the IOP for bus grants, the arbitration mechanism needs a separate request signal from each master to decide which one is to receive each grant.
BGN	20	I	**Bus Grant:** An active-low input from the host MPU or other arbiter, granting use of the MPU bus to the IOP. If there are no bus masters other than the IOP and host MPU, BGN can be inverted from the HLDA output of an Intel processor.
LBRN	21	I	**Local Bus Request:** An active-low input used in systems in which the MPU and IOP have separate buses, whereby the MPU can request access to the use of resources on the IOP's bus, including the IOP itself. It should be wired to a logic high in a system in which the MPU and IOP share the same bus. First MPU access to the IOP without asserting this signal will lock the IOP in one bus mode until reset.
LBGN	26	O	**Local Bus Grant:** LBGN is an active-low output by means of which the IOP responds to LBRN, and grants the host MPU access to resources on the IOP's bus.
IRQN	22	O	**Interrupt Request:** An active-low open-drain output to the host MPU, indicating that a channel program has requested an interrupt for one or more of the IOP channels. It must be inverted in an Intel style system. It requires an external pull-up resistor.
IACKN	23	I	**Interrupt Acknowledge:** An active-low input indicating the the host MPU is acknowledging the interrupt requested by IRQN. The IOP responds to the assertion of this signal by placing an interrupt vector on D7–D0, asserting DTACKN, and releasing IRQN if there is no further interrupt request for any channel.
BCLK	66	I	**Bus Clock:** The clock signal for the IOP.
RESETN	67	I	**Master Reset:** Active-low reset for the IOP. Must be asserted at power-up; may be asserted at other times the system is to be reset and restarted.
V_{CC}	19, 54, 68	I	**Power**
V_{SS}	18, 25, 36, 47, 53, 65	I	**Ground**

FUNCTIONAL DESCRIPTION

The IOP has its own 256x16 RAM which holds various tables and registers.

The IOP register map is shown in Figure 1 as it appears to the host microprocessor. The individual registers and RAMs in the map are described in the following sections. All registers/RAM location must be accessed in word form.

Note that parenthesis around the name of a register or RAM location indicates "the contents of". The name of a RAM table, followed by the name of a register in brackets, indicates the location in the RAM table which is selected by indexing into it using the contents of the register as the index (e.g. PCT[CHAN]).

Decision Table Base Register (DTBR)

This 11-bit register provides the high-order address bits when a decision table is read. The IOP can use up to 16 decision tables, each having 256 words (512 bytes). Decision tables reside in external memory that is 16 x 512 (8192) bytes size.

Program Counter Base Register (PCBR)

This 13-bit register provides the high-order address bits when fetching instructions from a channel program. All channel programs used by the IOP must reside in external memory that is 1024 words (2048 bytes) size.

Memory Address Table (MAT)

MAT is an on-chip RAM containing memory addresses. There is one 24-bit entry for each channel. In addition, in 2 bus systems in which the IOP has its own local bus separate from the host processor's bus, the bit position that would correspond to A31 is used to indicate whether the memory location in question is on the local bus or the system bus. Thus, the MAT is composed of 32 x 25 (800) bits of on-chip RAM.

Memory Count Table (MCT)

MCT is an on-chip RAM containing 14-bit length counts for the memory areas addressed by MAT, plus two bits defining whether 8- or 16-bit transfers should be done for the device and memory, respectively. There is one 16-bit entry for each channel. The MCT is composed of 32 x 16 (512) bits of on-chip RAM.

The two most significant bits of the words that the host processor writes and reads for MCT are flags defining whether the peripheral device for this channel has a data width of 8- or 16-bits, and whether data should be packed or unpacked between the device and the memory, as follows:

00 Byte device, byte memory transfers
01 Byte device, word memory transfers
10 Not allowed
11 Word device, word memory transfers

The packing feature can significantly decrease the traffic generated by the IOP on the host processor's bus, as described further in a subsequent section.

Device Address Table (DAT)

DAT is an on-chip RAM containing the address of each channel's device. There is one 24-bit entry for each channel. In addition, in systems in which the IOP has its own local bus separate from the host processor's bus, the bit position that would correspond to A31 is used to indicate whether the peripheral device in question is on the local bus or the system bus. The DAT is composed of 32 x 25 (800) bits of on-chip RAM.

Program Counter Table (PCT)

PCT is an on-chip RAM containing the location of the first instruction for each channel, The contents of a PCT entry are used relative to (concatenated below) the contents of PCBR. The PCT is composed of 32 x 10 (320) bits of on-chip RAM.

Byte Store Table (BST)

BST is an on-chip RAM that can store one data byte and one flag bit (BSTO flag) for each channel. This facility provides the packing and unpacking between a 16-bit memory and an 8-bit device.

CHAN Register

This 5-bit register is used as an index into MAT, MCT, DAT, and BST. When service is started for a channel, CHAN is loaded with a number derived from the request logic, and the contents of PCT[CHAN] becomes the starting point for execution. CHAN can thereafter be modified by the INTERP instruction.

TCHAN Register

This internal register is similar to CHAN and is used by the LDPCT and RELOAD instructions.

CTRL Register

This register is programmable by the host processor to control the basic operation of the IOP. Its contents are discussed in a later section.

CHAR Register

This 8-bit register is a temporary store for characters in transit between a device and memory, or for a status value from a device.

SVCHAR, SVBST Registers

These internal registers function as stores. They are accessible by some instructions.

Force/Status Register

F	0		CHANNEL
1	1	9	5

If the host MPU write this register with F = 1, the IOP will respond by executing instructions starting at the address in the PCT entry selected by the channel number written into the 5 low order bits of this register. It is done as if a request was asserted for the channel number. Writing this register with F = 0 will update previous writing with F = 1, if the forced request has not yet been revised.

If the IOP is already executing a channel program (or has already made an internal decision to do so) when the host MPU writes this register with F = 1, response will be delayed until after the channel program has ended. In any case, service for the channel written into this register has priority over starting new service in response to the RQn lines.

When the IOP begins service for the channel, it clears the F flag. If there is any possibility that the host MPU software might want to write another channel number for this register, before service for a previously written channel could be started, then the software must read this register and check for F = 0, before writing F = 1 and the new channel number.

Bit 14 of this register must be programmed with 0.

The Interrupt FIFO

The FIFO is used to maintain an interrupt queue for the host MPU. It includes 32 entries of 13 bits each, and can be programmed in the CTRL register to function as a single FIFO with 32 entries, or it can be divided into two FIFOs with 16 entries each, corresponding to two levels of interrupt priority.

INTCHN Register

INTCHN is a 5-bit read only register accessible to the host MPU, from which the number of the current (most recent) interrupting channel can be read. See description of the INT instruction.

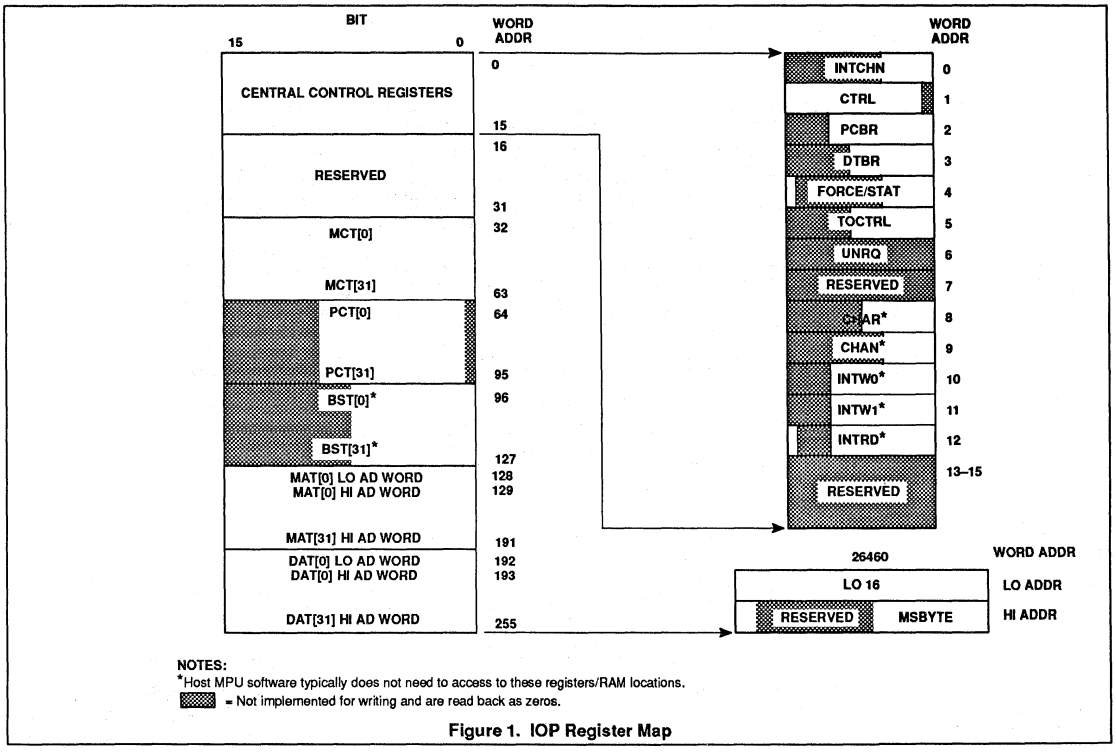


Figure 1. IOP Register Map

INTRP Register

This read only register is an interrupt polling register. It can be read by MPU software at the end of servicing an IOP interrupt, to determine whether another interrupt is pending. The data read has the following format.

V		NEXT INTCHN	NEXT VECTOR
1	2	5	8

If V bit is 1, the other two fields are valid and are supplied from the interrupt FIFO. INTRP is also used for device testing.

INTW0, INTW1 Registers

These two write-only registers are used for device testing, and allow entries to be written into the interrupt FIFO. Both register locations have the format:

	INTCHN	VECTOR
3	5	8

If the nL bit in the CTRL register is 0, indicating a signal-level interrupt queue, writing either register places the data in the 32-entry FIFO. If the nL bit is 1, writing INTW0 puts data in the lower-priority FIFO and writing INTW1 puts data in the higher-priority FIFO.

TOCTRL Register

This register control the IOP's bus time-out logic, and has the following format:

	TIMEOUT	VECTOR
5	3	8

The TIMEOUT field controls how long the IOP will wait for a DACKN response when it is running a bus cycle. If this time is exceeded, the IOP places the current channel number and the VECTOR field in the interrupt FIFO, as if an INT instruction had been executed. See Bus Timeout for further details.

UNRQ Register

This register is used to specify how many clock cycles the IOP would have to wait after finish servicing a channel and the external RQns show the same channel is still requesting for service. The register has the following format:

	COUNT
	5

The "count" field is the binary number of clocks the IOP waits. The time programmed in the register allows slow peripherals the time to clear its interrupt condition. If the request inputs RQns remain the same after the count expires, the IOP would service the channel again.

If the RQns change before the count expires (either during the count or before the count begins), the count will be stopped and the IOP will immediately service the new channel (or idle if all RQns go to 1's).

Programming this register with count = 0 means the IOP will not wait after the current channel service is completed. It is up to the user to make sure that any "request clearing" sequence performed by the IOP will not extend beyond the end of the channel service.

CTRL Register

This register is programmable by the host processor to control the basic operation of the IOP (See Figure 2). Note that the contents of the CTRL register represents system-level constants that are intended to

CTRL	dE	rE	0	MAX ON	MIN OFF	UPri	nL	0
	1	1	1	4	4	3	1	1

dE — This bit enables the overall operation of the IOP. If it is zero, the IOP ignores the RQn lines. dE resets to zero; host MPU software should set up the various registers and RAM locations in the IOP before programming this bit to 1.

rE — This bit indicates how the RQ lines are interpreted by the IOP and how the starting CHAN value for service is derived from them. If the request code on RQ4–RQ0 is externally encoded, then rE should be programmed to 0, in which case the IOP treats the RQn lines as carrying a channel number. If (5 or less) devices "interrupt request" signals are directly connected to the RQ lines, then rE should be programmed to 1, in which case the IOP encodes the state of RQ4–RQ0 to obtain a channel number. In this encoding, RQ4 has the highest priority and RQ0 the lowest. A table in the request logic section indicates the starting CHAN value for each of the five devices (RQ lines) when rE is 1.

Max On, Min Off — These fields are used only in single-bus applications. Max On controls the maximum length of time the IOP will retain control of the bus after being granted it, while Min Off controls the length of time for which the IOP will refrain from requesting the bus again, after it has given it up. Together, these two values constitute a "throttle" control on how much of the overall bus bandwidth an IOP will use. These times are measured in terms of the CLK input divided by 4. Max On = 0 indicates that the IOP will run only one bus cycle per grant. Note that in dual-bus application, the IOP will always give up control of the system bus after using it for one cycle, so that these values do not apply.

UPri — UPri assigns the starting channel number for each RQn input in the internal encoded mode (rE = 1). In this assignment, the lower the starting channel, the higher the priority. The effect of UPri on starting channel numbers is as follows:

← STARTING CHANNEL NUMBER →

INTERNALLY ENCODED RQ's

UPri	RQ4	RQ3	RQ2	RQ1	RQ0
000	8	12	16	20	24
001	0	12	16	20	24
010	0	4	16	20	24
011	0	4	8	20	24
100	0	4	8	12	24
101	0	4	8	12	16

nL — This bit controls how the interrupt FIFO is configured. If nL is 0, it is treated as a single FIFO of 32 entries, which are all at the same level of priority. If nL is 1, it is divided into 2 FIFOs each having 16 entries, representing two priority levels.

Figure 2. CTRL Register

be programmed once, at system initialization time. The only bit that can be re-programmed thereafter is dE.

Channel Reloading

The instruction set discussed in a later section provides a means for a channel program for a peripheral device to interrupt the host processor when an I/O buffer area in memory has been "exhausted". Such exhaustion may occur in one of two ways: If the byte count for the I/O buffer is decremented to zero, or if a status or data byte's value indicates that the buffer should be (prematurely) terminated.

If an I/O buffer is exhausted, but the peripheral device has or will have more data to transfer for this channel, then the MAT and MCT entries (the memory address and byte count) for each channel have to be reloaded before further data can be transferred. Such reloading can occur in one of two ways:

1. By means of the processor responding to the interrupt and directly rewriting the MAT and MCT entries in the IOP. This approach is suitable for situations in which the processor responds to an interrupt fast enough to satisfy the needs of the peripheral.

a. If the peripheral device is not subject to "underrun" or "overrun" conditions based on the response time. For example, an asynchronized comm line meets this criterion with respect to output, but not with respect to input. A synchronous comm line does not met this criterion in either direction.

b. Or, if the data rate is slow enough, and/or the device contains sufficient data buffering, to guarantee that the processor's interrupt response time will be fast enough to prevent underrun or overrun. for example, a 300 baud comm line might meet this criterion but a 19,200 baud line might not.

2. For a peripheral channel that needs faster reloading than the host processor guarantees to provide, the IOP can automatically reload the next buffer address and count. To do this, two of the IOP's channel are dedicated to the peripheral channel; one of them handles the peripheral data, while the second is used to reload addresses and counts for the first channel. Only 16 peripheral channels of this type can be handled by one IOP.

A peripheral channel, for which reloading can be handled by a host processor interrupt response, requires only one IOP channel; thus, 32 such peripheral channels can be handled by a single IOP.

Single and Dual Bus Applications

Applications of the IOP can be divided into two major categories called single and dual bus. In the single bus application shown in Figure 3, the IOP is on the same bus as the host processor, and must request and be granted the bus control before it can perform any bus cycle. This is a simple and low cost type of application, but does not yield the highest possible IOP performance.

Dual bus systems have the structure shown in Figure 4. Here, the IOP has its own local bus, on which resides the memory that contains channel programs and decision tables, and on which may also reside I/O buffers and/or peripheral devices. A set of hardware transceivers forms the interface between the IOP's local bus and the host processor's bus or an inter-board backplane bus.

The transceivers are under the control of the bus grant signal (BGN), by which the outside world grants use of the system bus to the IOP, and the local bus grant signal (LBGN), by which the IOP grants the host processor or other master use of the local bus. After a reset, the IOP detects that it is in a dual-bus system if/when LBRN goes low.

In a two-bus system, the IOP monitors the state of the LBRN input continuously. When it

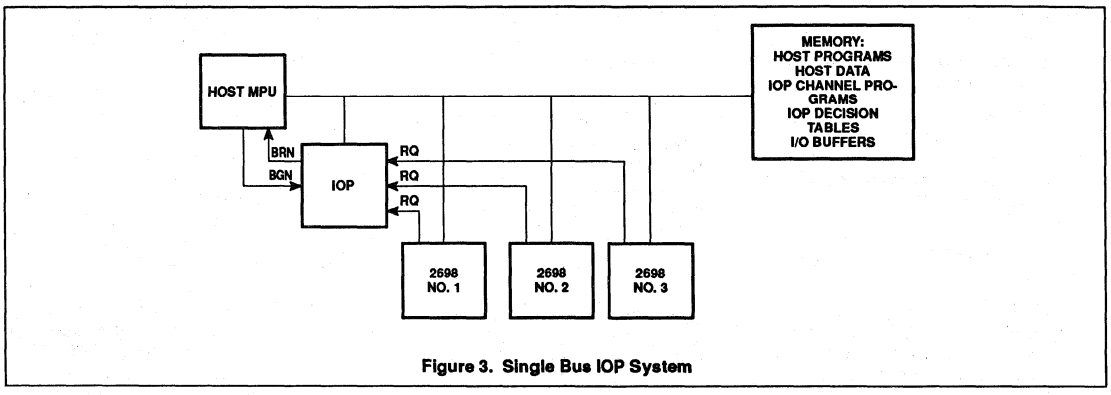


Figure 3. Single Bus IOP System

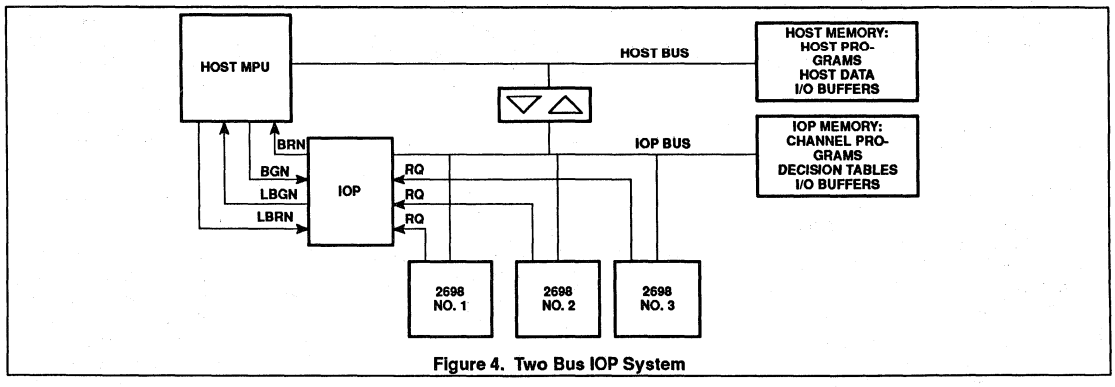


Figure 4. Two Bus IOP System

detects an LBRN asserted, it tri-states its bus signals and then asserts LBGN. This occurs immediately if the IOP is not performing a cycle on the local bus.

In a dual bus system, the IOP does not assert BRN, nor does it wait for BGN for memory accesses for instruction or decision table fetching. These are assumed to be on the local bus. It may assert BRN and wait for BGN before an access to a data buffer in memory or to a peripheral device, depending on the state of the MSB ("A31" position) of the MAT or DAT entry for the channel, respectively.

If the bit that would correspond to A31 of the MAT or DAT entry has been set to 1 by MPU software, or a RELOAD instruction, the IOP does not assert BRN, nor does it wait for BGN. If the bit is cleared to 0, the IOP asserts BRN and waits for the MPU to return BGN low before proceeding to drive ASN low. While the IOP is waiting for BGN, it remains sensitive to the LBRN input. If LBRN goes low, the IOP defers the bus cycle, tri-states A23–A1 and the other bus control pins, and responds with LBGN low. When the cycle is completed and LBRN is released, the IOP reruns its bus cycle. This feature prevents a system deadlock if the IOP and MPU both request access to resources on each other's buses.

Dual bus applications tend towards higher performance by allowing the IOP to perform most of its bus cycles without stopping host processor execution, or without using the system's backplane bus. However, in this case the host processor must request control of the local bus in order to access memory or peripherals on the local bus, or to access IOP registers/RAM.

Bus Time-Out Facility

Whenever the IOP is accessing external memory or peripheral, it waits for DACKN to be asserted. In case of certain system malfunctions, this response may never occur. Therefore, the IOP includes a time-out counter that operates whenever it is waiting for DACKN (but not when it is waiting for BGN). The time-out field of the TOCTRL register should be programmed by the host MPU before the IOP operation is enabled, to reflect a time-out longer than the longest valid DACKN response time that is possible in the system. The IOP will wait for DACKN for 2^{t+7} CLK periods, where t is the value of the 3-bit time-out field. Thus, a time-out field value of 0 will cause the IOP to wait up to 128 CLK periods. A 1 designates waiting 256 CLK periods, and so forth through the maximum time-out value of 7 which will cause the IOP to wait up to 16,384 CLK periods. At a CLK frequency of 16MHz, these correspond to a range of 8 microseconds to 1 millisecond.

If the time-out value is exceeded, the IOP internally simulates an INT instruction, using the higher priority level if there are two levels, using the vector field of the TOCTRL register as the vector value. Thus, it asserts the IRQN pin if it had not been asserted previously. After doing this, it clears the dE bit in the CTRL register so that it no longer responds to any further request signals. The vector from TOCTRL should cause the host MPU to investigate the problem and take appropriate corrective action.

Typical Execution

This section describes the IOP operation. For the instructions, the following general rules apply for channel program execution.

1. A peripheral device asserts its "interrupt request" output. This signal is either directly connected to one of the IOP's RQn inputs, or is encoded externally to make the value on RQ4–RQ0.
2. The request is serviced when no higher-priority peripheral is making a request.
3. The IOP begins service for this peripheral by transferring the encoded channel number to the CHAN and TCHAN registers, and then loads the value in the corresponding entry from the PCT RAM into its program counter (PC). It then executes the "channel program" that starts at the location in external memory.

   Note that the PCT entry for a channel is initially loaded by the host MPU, and can be changed by a channel program thereafter, in response to changing status of the peripheral device.
4. A channel program will typically start with an INTERP instruction that reads a status register on the peripheral and then uses the status byte as an index to read a word from a "decision table" in memory.
5. The contents of the word from the decision table may cause the IOP to do either, both, or neither of two things: change (add to) the value in the CHAN register, and/or branch, i.e. reload the PC with a value in the decision table word or from PCT [new CHAN].

   The two actions above correspond to the kinds of information that a peripheral status byte may convey: in a multi-channel peripheral device, it identifies which channel needs service, and/or it identifies any exceptional conditions (e.g. errors) involved in its "interrupt request".

   For example, in a peripheral with separate input and output channels, the decision table words corresponding to an "output request" might be coded to add 2 to (CHAN) and branch, while those corresponding to an "input request" might do neither of those things.

   Note that a priority between such input and output channels is determined by coding of words corresponding to "both requests". Also that while the decision table mechanism might be considered wasteful in memory, it improves performance by processing a whole status byte "in parallel" to make a decision that an MPU interrupt service routine might make by means of a series of "bit test" and "branch" instructions.
6. With some peripheral devices, several status registers may have to be read to determine what is to be done. For example, with the 2698 each DUART has an individual interrupt request line, but within each one, each UART has its own status register. In such cases, the channel program might begin with several consecutive INTERP instructions, one for each status register. The decision table words could be set up to:

   a. if the status register value indicates there is something to be done, branch to a routine to do it, or

   b. if there is nothing to be done, increment CHAN to the value that corresponds to the next status register, and don't branch.
7. After the INTERP instruction(s) have routed control to the appropriate branch of the channel program based on the peripheral status, a branch that transfers data will use an INPUT or OUTPUT instruction to transfer data between memory and (one of) the peripheral's data register(s).
8. INPUT and OUTPUT instructions can also use the decision table structure, for applications in which data byte values affect what is to be done. For example, in receiving from a datacomm line, reception of a carriage return (CR) character might mean that the current input buffer in memory is "complete" and that the host MPU should be notified.

   Decision table processing for INPUT and OUTPUT instructions is slightly different from that for INTERP. As with INTERP, certain data characters can cause a branch, but instead of CHAN adjustment, decision table words for data are coded to control whether the byte is transferred to the destination (to memory for INPUT, to the device for OUTPUT).
9. An INPUT and OUTPUT instruction will typically be written so that it ends servicing for the channel unless a decision table causes a branch, or the byte count for the I/O buffer in memory is decremented to zero.
10. When an I/O buffer is completed, the channel program will typically interrupt the host MPU. Such interrupts are stored in a queue on the IOP, so that the host MPU is interrupted once for each time any IOP channel program posts an interrupt.
11. In addition to interrupting the host when an I/O buffer is completed, the channel program can either use a RELOAD instruction to get another I/O buffer from a circular list of such buffers, or send a command byte to the device to tell it to stop asserting its "interrupt request" line for this channel, until the host MPU responds to the interrupt posted by the channel program.

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

PARAMETER	RATING	UNIT
Operating ambient temperature range	0 to +70	°C
Storage temperature range	–65 to +150	°C
Supply voltage to ground	–0.5 to +6.5	V
Power dissipation	1	W

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperature, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
V_{IL}	Input low voltage			0.8	V
V_{IH}	Input high voltage		2.0		V
V_{OL}	Output low voltage	I_{OL} = 2.4mA		0.4	V
V_{OH}	Output high voltage (except open-drain outputs)	I_{OH} = –400µA	V_{CC} – 0.5		V
I_{IL}	Input leakage current	V_{IN} = 0 to V_{CC}	–1	1	µA
I_{LL}	Data bus 3-State leakage current	V_{IN} = 0 to V_{CC}	–1	1	µA
I_{CC}	Power supply current	Freq. = 16MHz		90	mA

AC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ±10%[1]

NO.	FIGURE	PARAMETER	LIMITS		UNIT
			Min	Max	
1	5	BCLK frequency (Balanced Clock – 50%DC)		12.5	MHz
2	5	(Unbalanced Clock)		16	MHz
3	5	BCLK width high (16MHz unnbalanced Clock)	20		ns
4	5	BCLK width low (16MHz unnbalanced Clock)	40		ns
		RESETN width low	1000		ns
Master Arbitration					
5	6	BCLK high to BRN low		60	ns
6	6	BRN low to BGN low	0		ns
7[1]	6	Setup, BGN low to BCLK low	10		ns
8	6	BCLK high to drivers enabled	2		ns
9	6	BCLK high to BRN high		60	ns
10	6	BRN high to drivers disabled	0	20	ns
11	6	BRN high to BGN high	0		ns
12[1]	6	Setup, BGN high to BCLK low	10		
Master Operation					
20	7, 8	BCLK high to A23:1 change	0		ns
21	7, 8	BCLK high to A23:1 valid		60	ns
22	7, 8	BCLK high to RWC valid	0	60	ns
23	7, 8	BCLK high to M/IO valid	0	60	ns
24	7, 8	A23:1. RWC. and M/IO valid to ASN low	20		ns
25	7, 8	BCLK high to ASN low	4	45	ns
26	7, 8	BCLK high to DHIEN and/or DLOEN low	4	45	ns
27	7	D15:0 valid (read) to DACKN low	0		ns
28[1]	7, 8	Setup, DACKN low to BCLK high	10		ns
29	7, 8	BCLK low to ASN high		50	ns
30	7, 8	BCLK low to DHIEN and DLOEN high		40	ns
31	7	Hold, read data valid after DHIEN and DLOEN high	0		ns
32	7, 8	DHIEN and DLOEN high to DACKN high (to avoid acknowledging next cycle)		t_{BCLK}	ns
34	8	BCLK high to data bus drivers enabled (write)	0		ns
35	8	BCLK high to write data valid		65	ns
36	8	Write data valid to DHIEN and/or DLOEN low	10		ns
37	8	Hold, write data valid after BCLK high	5		ns

AC ELECTRICAL CHARACTERISTICS (Continued)

NO.	FIGURE	PARAMETER	LIMITS Min	LIMITS Max	UNIT
Master Operation (cont.)					
38	8	BCLK high to data bus released (end of write)		30	ns
Slave Arbitration (Two Bus System)					
39[1]	9	Setup, LBRN low to BCLK low	10		ns
40	9	BCLK high to LBGN low		45	ns
41	9	BCLK high to IOP drivers disabled		30	ns
42	9	LBGN low to IOP drivers disabled		20	ns
43[1]	9	Setup, LBRN high to BCLK low	10		ns
44	9	LBRN high to LBGN high		45	ns
45	9	BCLK high to IOP drivers enabled	10		ns
Slave Operation					
47	10, 11	Setup, A8:1 valid to CSN low	0		ns
48	10, 11	Setup, RWC valid to CSN low	0		ns
49	10, 11	Setup, DHIEN and/or DLOEN low to CSN low	0		ns
50[1]	11, 12	Setup, CSN low to BCLK low	10		ns
51[3]	10, 11, 12	IOP response latency	$3t_{BCLK}$	$11t_{BCLK}$	ns
53	10, 11	BCLK low to data bus valid (read or IACK)		70	ns
54	10, 11, 12	BCLK low to DACKN low		40	ns
55	10, 11	DACKN low to CSN high or (DHIEN and DLOEN high)	0		ns
56	10	Data bus valid after CSN high or (DHIEN and DLOEN high)	10		ns
57	10	CSN high or (DHIEN and DLOEN high) to data bus released		30	ns
58	10, 11	CSN high or (DHIEN and CLOEN high) to DACKN released		30	ns
59	10, 11	Hold, A8:1 valid after CSN high or (DHIEN and DLOEN high)	0		ns
60	10, 11	Hold, RWC valid after CSN high or (DHIEN and DLOEN high)	0		ns
61	10, 11	CSN width high (intercycle)	t_{BCLK}		ns
62	11	Setup, data bus valid (write) to CSN low	0		ns
63	12	Hold, write data valid after CSN high or (DHIEN and DLOEN high)	0		ns
64[1]	12	Setup, IACKN low to BCLK low	10		ns
65	12	BCLK low to IRQN released		70	ns
66	12	DACKN low to IACKN high	0	50	ns
67[1]	12	Setup, IACKN high to BCLK low	10		ns
68	12	Hold, data bus valid after IACKN high	10		ns
69	12	IACKN high to data bus released		30	ns
70	12	IACKN high to DACKN released		35	ns

NOTES:

1. If the subject input signal meets this setup time, the IOP is guaranteed to recognize its new state at the subject edge of BCLK. If this setup time is not met, recognition may occur at the subject clock edge, or one BCLK later.
2. The maximum rating of this parameter should be as short as is consistent with device characterization, so as to maximize the compatibility of the IOP with processors that re-arbitrate and re-grant if BR is kept low after a first grant.
3. This parameter defines the number of clock cycles (wait states) between the BCLK falling edge at which CSN or IACKN is sampled and the falling edge from which the IOP responds with DACKN low, which is a function of the IOP's internal state and activity. For accesses to DMA processor registers when the IOP is idle, 3 BCLK cycles are required. If the IOP is internally active at the same time CSN or IACKN goes low, up to 11 BCLK cycles may be needed.

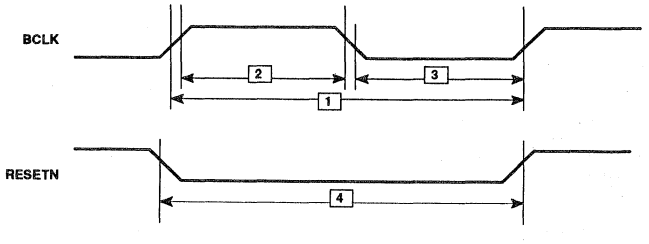


Figure 5. Clock and Reset Timing

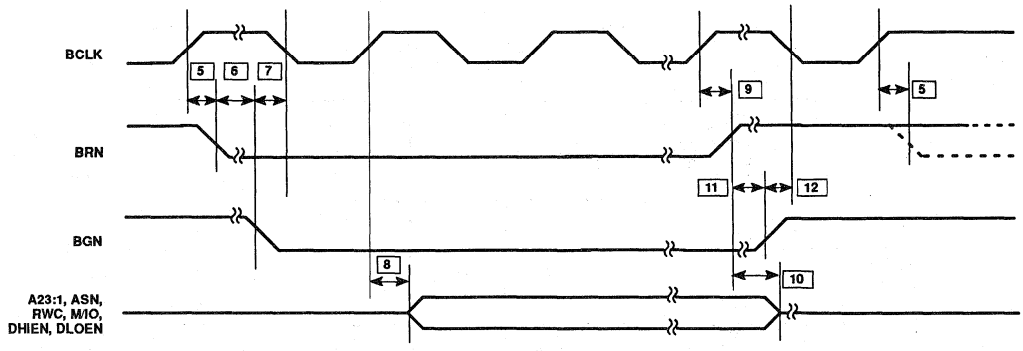


Figure 6. Two Wire Master Arbitration

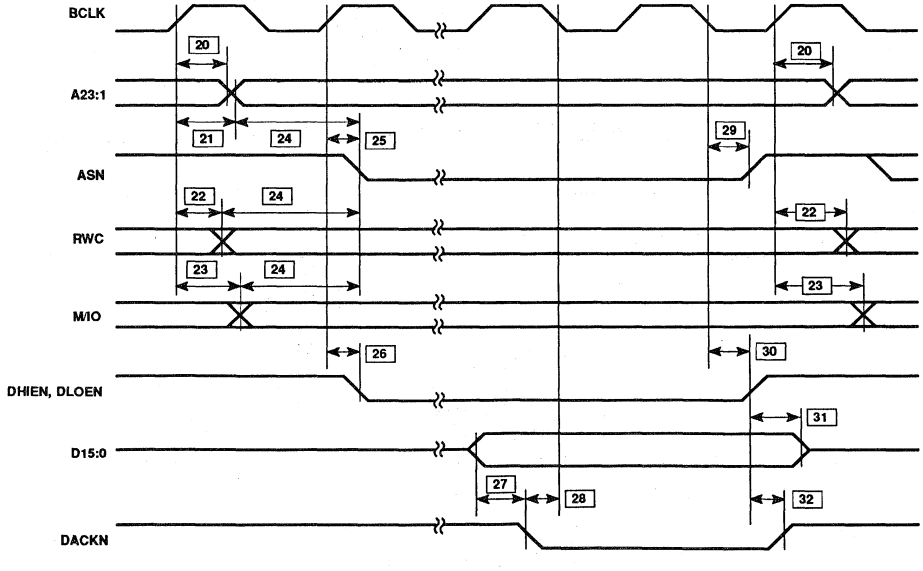


Figure 7. IOP Read From External Peripheral or Memory

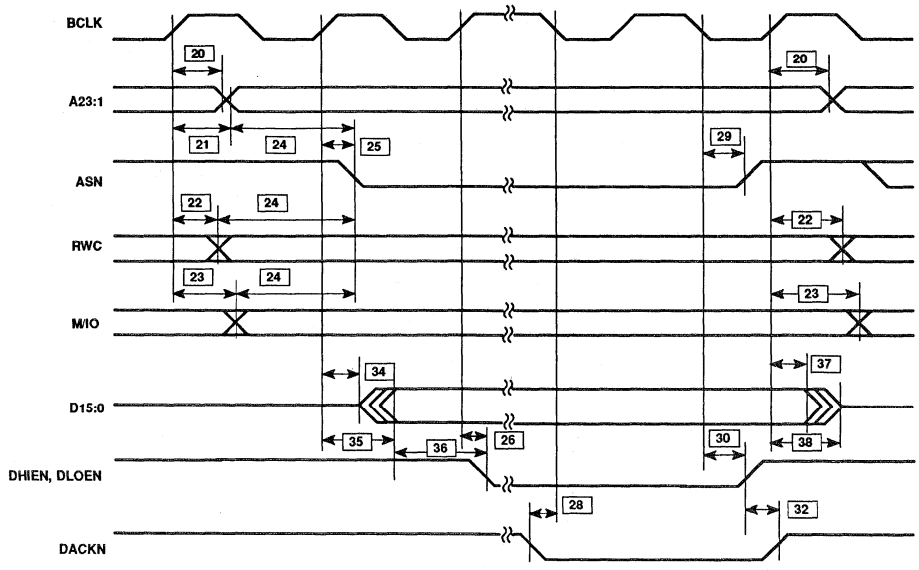


Figure 8. IOP Write to External Peripheral or Memory

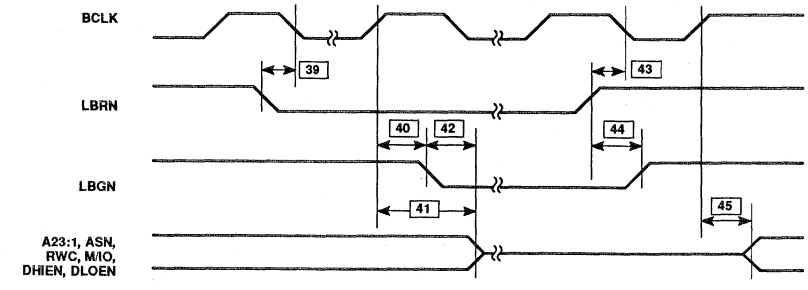


Figure 9. Dual Bus "Slave" Arbitration

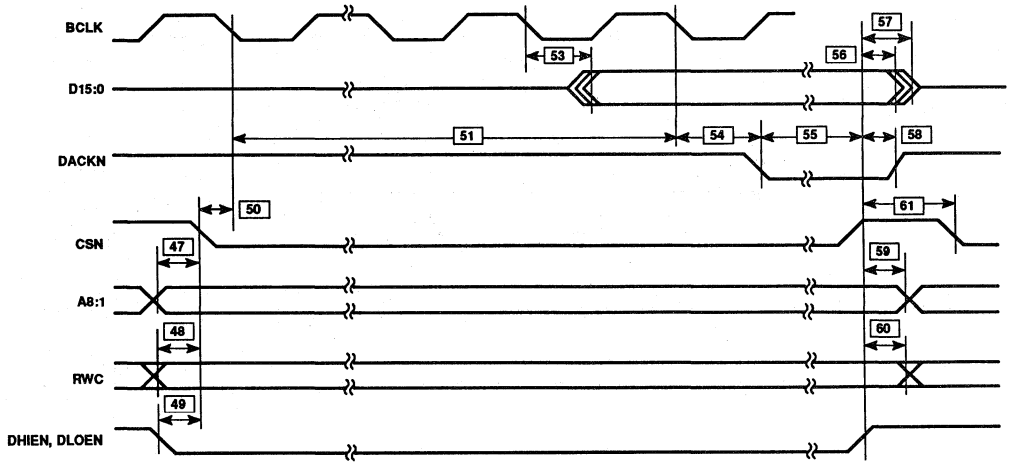


Figure 10. Host MPU Read From IOP

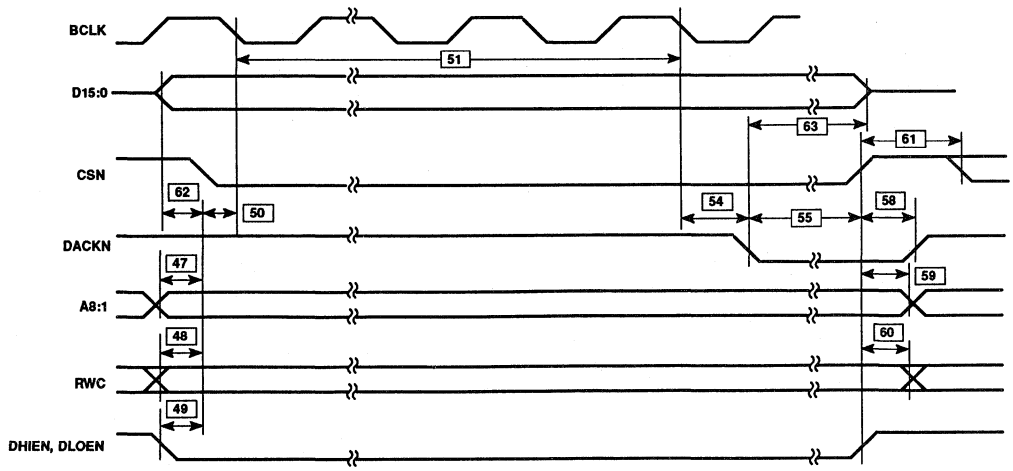


Figure 11. Host MPU Write to IOP

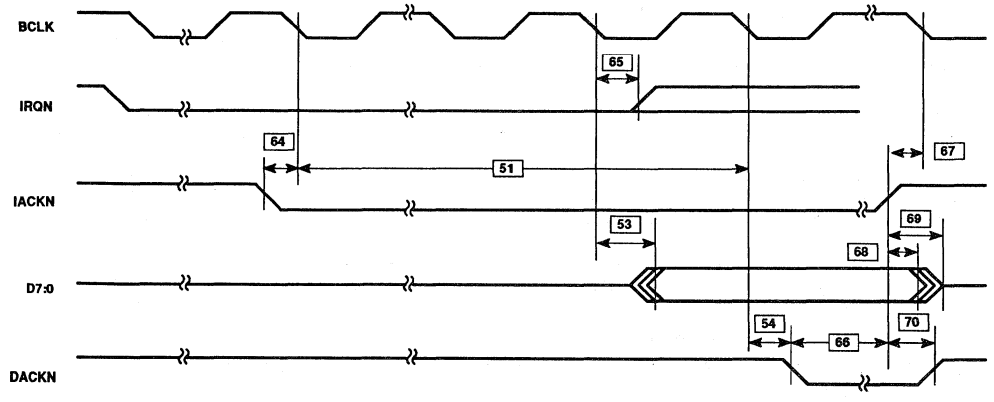


Figure 12. Interrupt Acknowledge Cycle by Host MPU

Input/output processor (IOP) SC68C460

DESCRIPTION

The Signetics SC68C460 I/O Processor (IOP) is a co-processor that greatly reduces the CPU overhead required to service a large number of I/O devices. It can inspect, modify or delete the data it transfers. Each channel can have its own channel program, which can branch depending on device status or a data test.

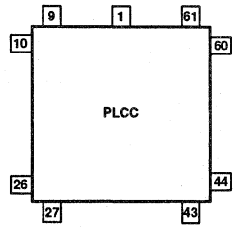
The IOP includes the features of a 32-channel Direct Memory Access (DMA) controller. This helps in handling multi-channel devices such as the Signetics 68C94 OCT-ART. It can create a data buffer chain in memory to transfer sequential blocks, greatly reducing the number of times the CPU needs to be interrupted.

The IOP can be attached directly to the system bus, or for higher performance, can support an additional local I/O bus.

FEATURES

- 32 channel DMA processor
- Separate memory address and length for each channel
- Separate I/O device address for each channel
- Separate channel program entry point for each channel
- Programmable to handle virtually all types of peripherals
- Custom instruction set
- Can interpret peripheral status for channel selection, error checking
- Can interpret data characters for buffer termination checking, control sequence transformation
- 8- or 16-bit data transfers
- 24-bit memory addresses: 16Mbyte address space
- 2-level interrupt queue minimizes host microprocessor overhead
- Stores and fetches data similar to Intel processors
- Can transfer multiple blocks without interrupting the CPU
- High-speed CMOS technology
- 68-pin PLCC

PIN CONFIGURATION

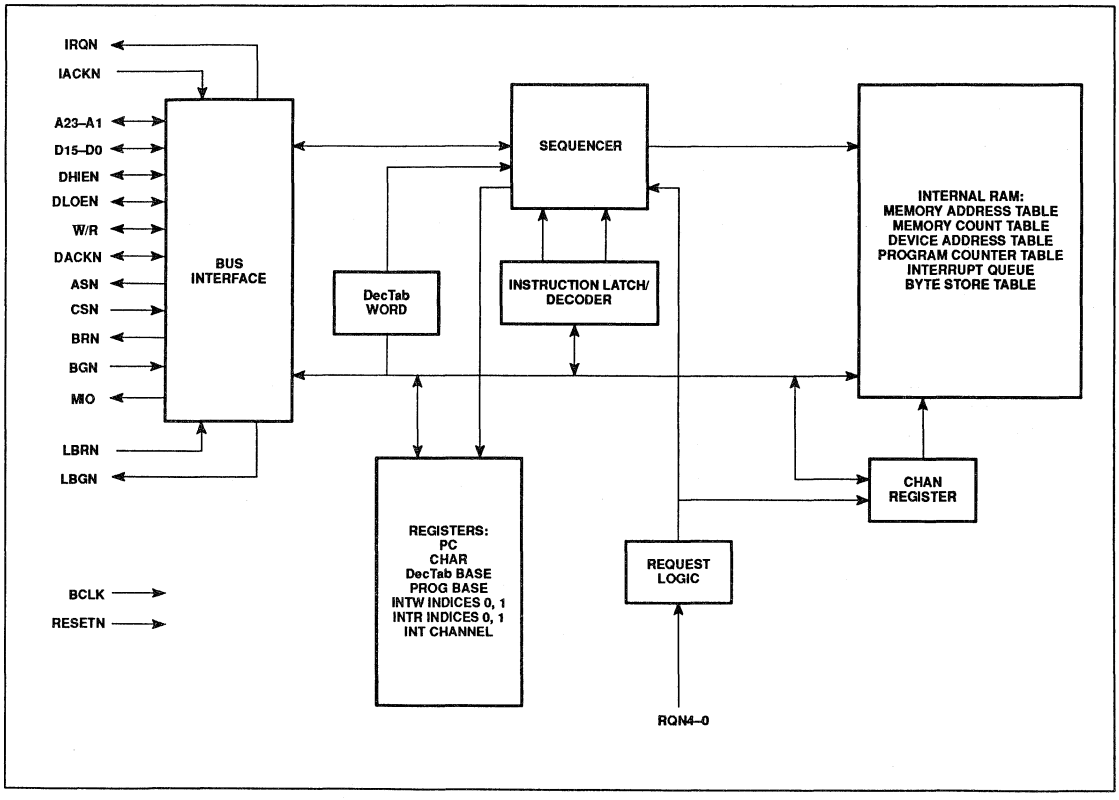


Pin	Function	Pin	Function
1	D10	35	A21
2	D9	36	V_{SS}
3	D8	37	A20
4	D7	38	A19
5	D6	39	A18
6	D5	40	A17
7	D4	41	A16
8	D3	42	A15
9	D2	43	A14
10	D1	44	A13
11	D0	45	A12
12	RQ0N	46	A11
13	RQ1N	47	V_{SS}
14	RQ2N	48	A10
15	RQ3N	49	A9
16	RQ4N	50	A8
17	BRN	51	A7
18	V_{SS}	52	A6
19	V_{CC}	53	V_{SS}
20	BGN	54	V_{CC}
21	LBRN	55	A5
22	IRQN	56	A4
23	IACKN	57	A3
24	CSN	58	A2
25	V_{SS}	59	A1
26	LBGN	60	D15
27	DACKN	61	D14
28	M/IO	62	D13
29	W/R	63	D12
30	DHIEN	64	D11
31	DLOEN	65	V_{SS}
32	ASN	66	BCLK
33	A23	67	RESETN
34	A22	68	V_{CC}

ORDERING INFORMATION

PACKAGE	V_{CC} = 5V ± 10%, T_A = 0°C to 70°C
Plastic PLCC	SC68C460C6A

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
RQ4N–RQ0N	16–12	I	**Request Lines:** A set of active-low inputs from external peripheral devices handled by the IOP. Typically, these will be the "interrupt request" lines from the peripherals. If there are 5 peripheral lines or less, they can be directly connected to these pins. Otherwise, the lines must be externally encoded. The IOP interprets the "all high" state on these lines as "no request". These input request lines are internally synchronized. When the IOP is idle, and it detects the stable active state on these lines on two consecutive falling edges of BCLK, it begins activity for the indicated channel.
CSN	24	I	**Chip Select:** An active-low input indicating that the host MPU is trying to access a register or RAM location on the IOP. CSN is not asserted until all of the signals, A8–A1, DHIEN, DLOEN, and $\overline{W}$/R are valid (this eliminates signalling differences among host MPUs). This, in turn, implies that in a system in which IOP has its own "local bus", CSN should be qualified with LBGN.
A23–A1	33–35, 37–46, 48, 49, 50–52, 55–59	O O O I/O I/O	**Address Lines:** When the IOP is a bus master, these lines carry the address to be accessed, which may be in memory or in a peripheral device. When the IOP is a bus slave, A8–A1 selects an internal location in the IOP to be read or written by the host MPU.

PIN DESCRIPTION (Continued)

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
D15–D0	60–64, 1–11	I/O	**Bidirectional Data Bus:** 16-bit data bus for the IOP, memory, peripherals, and the host MPU.
M/IO	28	O	**Memory/Input-Output Control:** When the IOP is a bus master, this tri-state output is driven high to indicate an access to memory, and low to indicate an access to a peripheral device. MIO has the same timing as A23–A1. When the IOP is a bus slave, this output is tri-stated.
ASN	32	O	**Address Strobe:** When the IOP is bus master, this is an output indicating that a transfer cycle is in progress on the bus, and, in particular, that a valid address has been placed on A23–A1. This signal is not driven at other times.
DHIEN, DLOEN	30, 31	I/O	**Data High/Low Enable:** When the IOP is a bus master, these pins are outputs. DHIEN low in a master read cycle indicates that the memory or peripheral selected by A23–A1 should read a byte and place its contents on D15–D8, while DLOEN low has the same meaning for the D7–D0 lines. In a master write cycle, DHIEN (DLOEN) low indicates that the IOP has placed valid data on D15–D8 (D7–D0), and that the memory or peripheral selected by A23–A1 should write the data into the appropriate byte(s). When both signals are low in a master cycle, a 16-bit word should be transferred. When the IOP is not a bus master, these lines are inputs from the host MPU. These two signals are internally ANDed. Either signal goes active, along with CSN active, will cause the IOP to be accessed.
$\overline{W}$/R	29	I/O	**Read/Write Control:** When the IOP is a bus master, this output controls the direction of data transfer on D15–D0. On the IOP, this signal is low for a write and high for a read. and corresponds to $\overline{W}$/R on the 68000. When the IOP is not the current bus master, W/$\overline{R}$ is an input from the host MPU, with the same meaning.
DACKN	27	I/O	**Data Acknowledge:** When the IOP is a bus master, this is an input signal from memory and peripherals, acknowledging that the requested bus transfer has been completed. When the IOP is a bus slave, this is an open-drain output to the host MPU, with the same meaning. This signal corresponds to DACKN on 68000.
BRN	17	O	**Bus Request:** An active-low output to the host MPU or other bus arbiter, requesting the use of the MPU bus. It must be inverted to produce HOLD in an "Intel" system. BRN is not open-drain because if the host MPU is the arbiter and the IOP is the only other master, a totem-pole output eliminates the need for a pull-up resistor. Also, if there are other masters contending with the IOP for bus grants, the arbitration mechanism needs a separate request signal from each master to decide which one is to receive each grant.
BGN	20	I	**Bus Grant:** An active-low input from the host MPU or other arbiter, granting use of the MPU bus to the IOP. If there are no bus masters other than the IOP and host MPU, BGN can be inverted from the HLDA output of an Intel processor.
LBRN	21	I	**Local Bus Request:** An active-low input used in systems in which the MPU and IOP have separate buses, whereby the MPU can request access to the use of resources on the IOP's bus, including the IOP itself. It should be wired to a logic high in a system in which the MPU and IOP share the same bus. First MPU access to the IOP without asserting this signal will lock the IOP in one bus mode until reset.
LBGN	26	O	**Local Bus Grant:** LBGN is an active-low output by means of which the IOP responds to LBRN, and grants the host MPU access to resources on the IOP's bus.
IRQN	22	O	**Interrupt Request:** An active-low open-drain output to the host MPU, indicating that a channel program has requested an interrupt for one or more of the IOP channels. It must be inverted in an Intel style system. It requires an external pull-up resistor.
IACKN	23	I	**Interrupt Acknowledge:** An active-low input indicating the the host MPU is acknowledging the interrupt requested by IRQN. The IOP responds to the assertion of this signal by placing an interrupt vector on D7–D0, asserting DTACKN, and releasing IRQN if there is no further interrupt request for any channel.
BCLK	66	I	**Bus Clock:** The clock signal for the IOP.
RESETN	67	I	**Master Reset:** Active-low reset for the IOP. Must be asserted at power-up; may be asserted at other times the system is to be reset and restarted.
V_{CC}	19, 54, 68	I	**Power**
V_{SS}	18, 25, 36, 47, 53, 65	I	**Ground**

FUNCTIONAL DESCRIPTION

The IOP has its own 256x16 RAM which holds various tables and registers.

The IOP register map is shown in Figure 1 as it appears to the host microprocessor. The individual registers and RAMs in the map are described in the following sections. All registers/RAM location must be accessed in word form.

Note that parenthesis around the name of a register or RAM location indicates "the contents of". The name of a RAM table, followed by the name of a register in brackets, indicates the location in the RAM table which is selected by indexing into it using the contents of the register as the index (e.g. PCT[CHAN]).

Decision Table Base Register (DTBR)

This 11-bit register provides the high-order address bits when a decision table is read. The IOP can use up to 16 decision tables, each having 256 words (512 bytes). Decision tables reside in external memory that is 16 x 512 (8192) bytes size.

Program Counter Base Register (PCBR)

This 13-bit register provides the high-order address bits when fetching instructions from a channel program. All channel programs used by the IOP must reside in external memory that is 1024 words (2048 bytes) size.

Memory Address Table (MAT)

MAT is an on-chip RAM containing memory addresses. There is one 24-bit entry for each channel. In addition, in 2 bus systems in which the IOP has its own local bus separate from the host processor's bus, the bit position that would correspond to A31 is used to indicate whether the memory location in question is on the local bus or the system bus. Thus, the MAT is composed of 32 x 25 (800) bits of on-chip RAM.

Memory Count Table (MCT)

MCT is an on-chip RAM containing 14-bit length counts for the memory areas addressed by MAT, plus two bits defining whether 8- or 16-bit transfers should be done for the device and memory, respectively. There is one 16-bit entry for each channel. The MCT is composed of 32 x 16 (512) bits of on-chip RAM.

The two most significant bits of the words that the host processor writes and reads for MCT are flags defining whether the peripheral device for this channel has a data width of 8- or 16-bits, and whether data should be packed or unpacked between the device and the memory, as follows:

00 Byte device, byte memory transfers
01 Byte device, word memory transfers
10 Not allowed
11 Word device, word memory transfers

The packing feature can significantly decrease the traffic generated by the IOP on the host processor's bus, as described further in a subsequent section.

Device Address Table (DAT)

DAT is an on-chip RAM containing the address of each channel's device. There is one 24-bit entry for each channel. In addition, in systems in which the IOP has its own local bus separate from the host processor's bus, the bit position that would correspond to A31 is used to indicate whether the peripheral device in question is on the local bus or the system bus. The DAT is composed of 32 x 25 (800) bits of on-chip RAM.

Program Counter Table (PCT)

PCT is an on-chip RAM containing the location of the first instruction for each channel, The contents of a PCT entry are used relative to (concatenated below) the contents of PCBR. The PCT is composed of 32 x 10 (320) bits of on-chip RAM.

Byte Store Table (BST)

BST is an on-chip RAM that can store one data byte and one flag bit (BSTO flag) for each channel. This facility provides the packing and unpacking between a 16-bit memory and an 8-bit device.

CHAN Register

This 5-bit register is used as an index into MAT, MCT, DAT, and BST. When service is started for a channel, CHAN is loaded with a number derived from the request logic, and the contents of PCT[CHAN] becomes the starting point for execution. CHAN can thereafter be modified by the INTERP instruction.

TCHAN Register

This internal register is similar to CHAN and is used by the LDPCT and RELOAD instructions.

CTRL Register

This register is programmable by the host processor to control the basic operation of the IOP. Its contents are discussed in a later section.

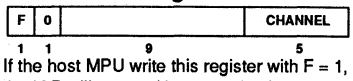
CHAR Register

This 8-bit register is a temporary store for characters in transit between a device and memory, or for a status value from a device.

SVCHAR, SVBST Registers

These internal registers function as stores. They are accessible by some instructions.

Force/Status Register



If the host MPU write this register with F = 1, the IOP will respond by executing instructions starting at the address in the PCT entry selected by the channel number written into the 5 low order bits of this register. It is done as if a request was asserted for the channel number. Writing this register with F = 0 will update previous writing with F = 1, if the forced request has not yet been revised.

If the IOP is already executing a channel program (or has already made an internal decision to do so) when the host MPU writes this register with F = 1, response will be delayed until after the channel program has ended. In any case, service for the channel written into this register has priority over starting new service in response to the RQn lines.

When the IOP begins service for the channel, it clears the F flag. If there is any possibility that the host MPU software might want to write another channel number for this register, before service for a previously written channel could be started, then the software must read this register and check for F = 0, before writing F = 1 and the new channel number.

Bit 14 of this register must be programmed with 0.

The Interrupt FIFO

The FIFO is used to maintain an interrupt queue for the host MPU. It includes 32 entries of 13 bits each, and can be programmed in the CTRL register to function as a single FIFO with 32 entries, or it can be divided into two FIFOs with 16 entries each, corresponding to two levels of interrupt priority.

INTCHN Register

INTCHN is a 5-bit read only register accessible to the host MPU, from which the number of the current (most recent) interrupting channel can be read. See description of the INT instruction.

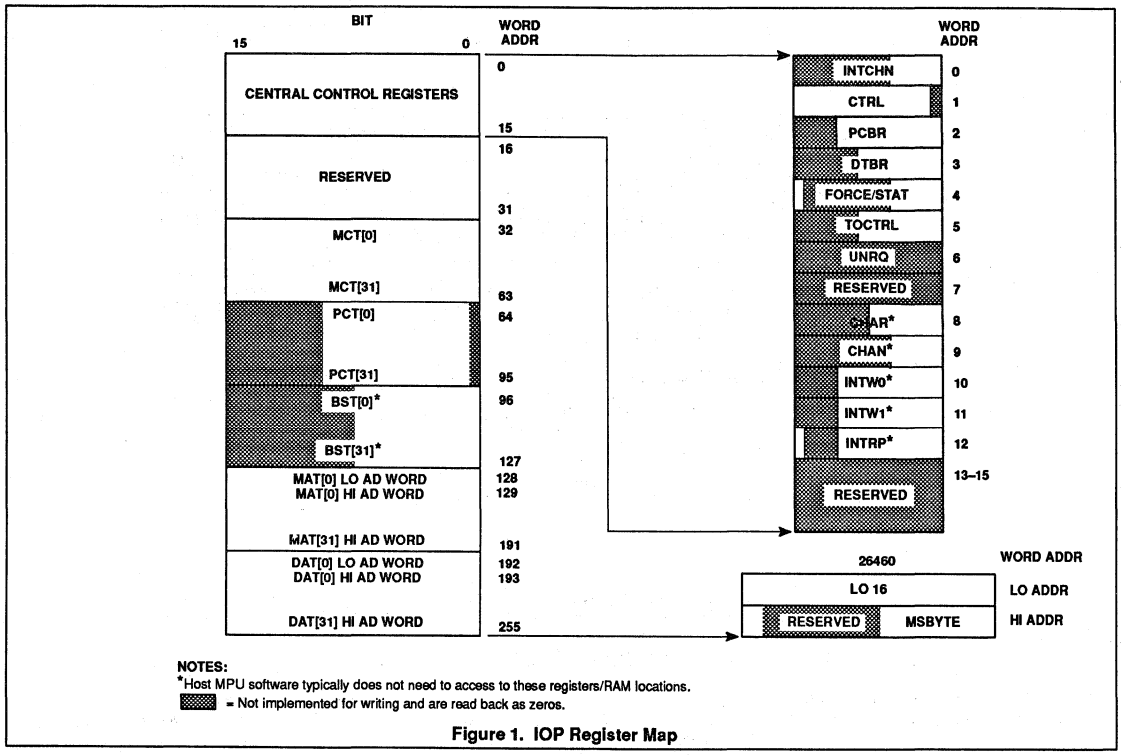


Figure 1. IOP Register Map

INTRP Register

This read only register is an interrupt polling register. It can be read by MPU software at the end of servicing an IOP interrupt, to determine whether another interrupt is pending. The data read has the following format.

V		NEXT INTCHN	NEXT VECTOR
1	2	5	8

If V bit is 1, the other two fields are valid and are supplied from the interrupt FIFO. INTRP is also used for device testing.

INTW0, INTW1 Registers

These two write-only registers are used for device testing, and allow entries to be written into the interrupt FIFO. Both register locations have the format:

	INTCHN	VECTOR
3	5	8

If the nL bit in the CTRL register is 0, indicating a signal-level interrupt queue, writing either register places the data in the 32-entry FIFO. If the nL bit is 1, writing INTW0 puts data in the lower-priority FIFO and writing INTW1 puts data in the higher-priority FIFO.

TOCTRL Register

This register control the IOP's bus time-out logic, and has the following format:

	TIMEOUT	VECTOR
5	3	8

The TIMEOUT field controls how long the IOP will wait for a DACKN response when it is running a bus cycle. If this time is exceeded, the IOP places the current channel number and the VECTOR field in the interrupt FIFO, as if an INT instruction had been executed. See Bus Timeout for further details.

UNRQ Register

This register is used to specify how many clock cycles the IOP would have to wait after finish servicing a channel and the external RQns show the same channel is still requesting for service. The register has the following format:

	COUNT
	5

The "count" field is the binary number of clocks the IOP waits. The time programmed in the register allows slow peripherals the time to clear its interrupt condition. If the request inputs RQns remain the same after the count expires, the IOP would service the channel again.

If the RQns change before the count expires (either during the count or before the count begins), the count will be stopped and the IOP will immediately service the new channel (or idle if all RQns go to 1's).

Programming this register with count = 0 means the IOP will not wait after the current channel service is completed. It is up to the user to make sure that any "request clearing" sequence performed by the IOP will not extend beyond the end of the channel service.

CTRL Register

This register is programmable by the host processor to control the basic operation of the IOP (See Figure 2). Note that the contents of the CTRL register represents system-level constants that are intended to

CTRL	dE	rE	0	MAX ON	MIN OFF	UPri	nL	0
	1	1	1	4	4	3	1	1

dE — This bit enables the overall operation of the IOP. If it is zero, the IOP ignores the RQn lines. dE resets to zero; host MPU software should set up the various registers and RAM locations in the IOP before programming this bit to 1.

rE — This bit indicates how the RQ lines are interpreted by the IOP and how the starting CHAN value for service is derived from them. If the request code on RQ4–RQ0 is externally encoded, then rE should be programmed to 0, in which case the IOP treats the RQn lines as carrying a channel number. If (5 or less) devices "interrupt request" signals are directly connected to the RQ lines, then rE should be programmed to 1, in which case the IOP encodes the state of RQ4–RQ0 to obtain a channel number. In this encoding, RQ4 has the highest priority and RQ0 the lowest. A table in the request logic section indicates the starting CHAN value for each of the five devices (RQ lines) when rE is 1.

Max On, Min Off — These fields are used only in single-bus applications. Max On controls the maximum length of time the IOP will retain control of the bus after being granted it, while Min Off controls the length of time for which the IOP will refrain from requesting the bus again, after it has given it up. Together, these two values constitute a "throttle" control on how much of the overall bus bandwidth an IOP will use. These times are measured in terms of the CLK input divided by 4. Max On = 0 indicates that the IOP will run only one bus cycle per grant. Note that in dual-bus application, the IOP will always give up control of the system bus after using it for one cycle, so that these values do not apply.

UPri — UPri assigns the starting channel number for each RQn input in the internal encoded mode (rE = 1). In this assignment, the lower the starting channel, the higher the priority. The effect of UPri on starting channel numbers is as follows:

← STARTING CHANNEL NUMBER →

INTERNALLY ENCODED RQ's

UPri	RQ4	RQ3	RQ2	RQ1	RQ0
000	8	12	16	20	24
001	0	12	16	20	24
010	0	4	16	20	24
011	0	4	8	20	24
100	0	4	8	12	24
101	0	4	8	12	16

nL — This bit controls how the interrupt FIFO is configured. If nL is 0, it is treated as a single FIFO of 32 entries, which are all at the same level of priority. If nL is 1, it is divided into 2 FIFOs each having 16 entries, representing two priority levels.

Figure 2. CTRL Register

be programmed once, at system initialization time. The only bit that can be re-programmed thereafter is dE.

Channel Reloading

The instruction set discussed in a later section provides a means for a channel program for a peripheral device to interrupt the host processor when an I/O buffer area in memory has been "exhausted". Such exhaustion may occur in one of two ways: If the byte count for the I/O buffer is decremented to zero, or if a status or data byte's value indicates that the buffer should be (prematurely) terminated.

If an I/O buffer is exhausted, but the peripheral device has or will have more data to transfer for this channel, then the MAT and MCT entries (the memory address and byte count) for each channel have to be reloaded before further data can be transferred. Such reloading can occur in one of two ways:

1. By means of the processor responding to the interrupt and directly rewriting the MAT and MCT entries in the IOP. This approach is suitable for situations in which the processor responds to an interrupt fast enough to satisfy the needs of the peripheral.

a. If the peripheral device is not subject to "underrun" or "overrun" conditions based on the response time. For example, an asynchronized comm line meets this criterion with respect to output, but not with respect to input. A synchronous comm line does not met this criterion in either direction.

b. Or, if the data rate is slow enough, and/or the device contains sufficient data buffering, to guarantee that the processor's interrupt response time will be fast enough to prevent underrun or overrun. for example, a 300 baud comm line might meet this criterion but a 19,200 baud line might not.

2. For a peripheral channel that needs faster reloading than the host processor guarantees to provide, the IOP can automatically reload the next buffer address and count. To do this, two of the IOP's channel are dedicated to the peripheral channel; one of them handles the peripheral data, while the second is used to reload addresses and counts for the first channel. Only 16 peripheral channels of this type can be handled by one IOP.

A peripheral channel, for which reloading can be handled by a host processor interrupt response, requires only one IOP channel; thus, 32 such peripheral channels can be handled by a single IOP.

Single and Dual Bus Applications

Applications of the IOP can be divided into two major categories called single and dual bus. In the single bus application shown in Figure 3, the IOP is on the same bus as the host processor, and must request and be granted the bus control before it can perform any bus cycle. This is a simple and low cost type of application, but does not yield the highest possible IOP performance.

Dual bus systems have the structure shown in Figure 4. Here, the IOP has its own local bus, on which resides the memory that contains channel programs and decision tables, and on which may also reside I/O buffers and/or peripheral devices. A set of hardware transceivers forms the interface between the IOP's local bus and the host processor's bus or an inter-board backplane bus.

The transceivers are under the control of the bus grant signal (BGN), by which the outside world grants use of the system bus to the IOP, and the local bus grant signal (LBGN), by which the IOP grants the host processor or other master use of the local bus. After a reset, the IOP detects that it is in a dual-bus system if/when LBRN goes low.

In a two-bus system, the IOP monitors the state of the LBRN input continuously. When it

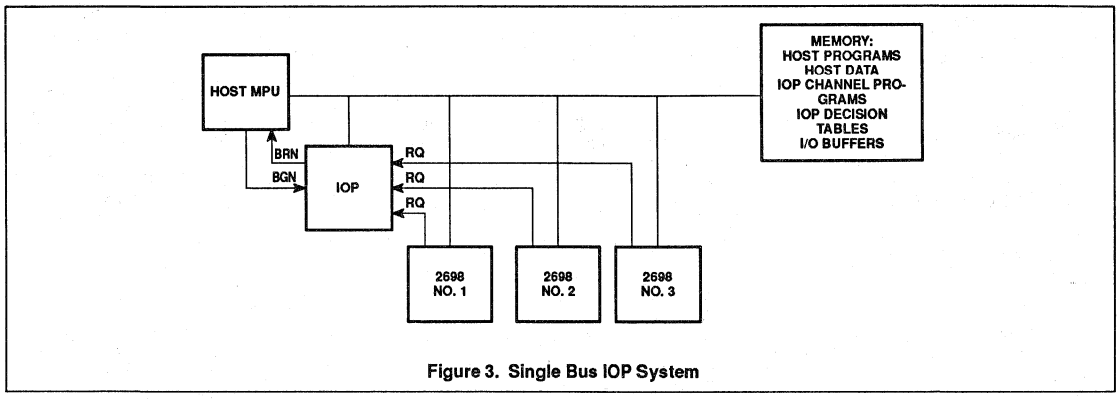


Figure 3. Single Bus IOP System

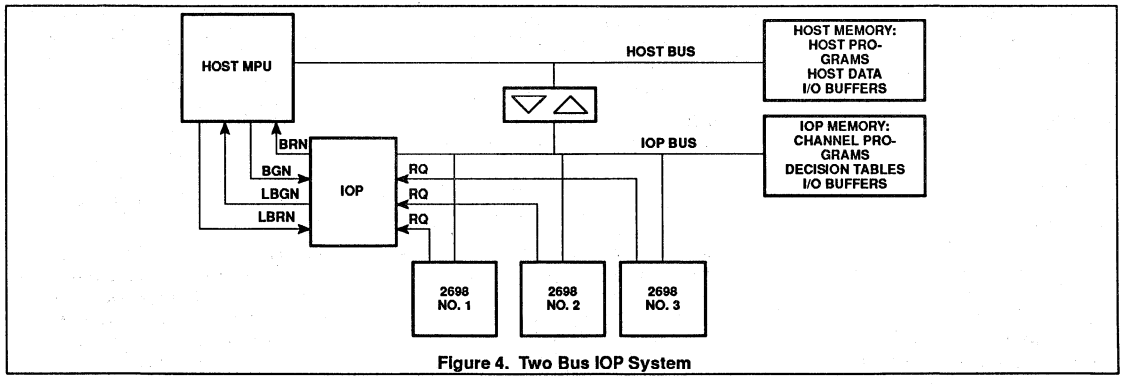


Figure 4. Two Bus IOP System

detects an LBRN asserted, it tri-states its bus signals and then asserts LBGN. This occurs immediately if the IOP is not performing a cycle on the local bus.

In a dual bus system, the IOP does not assert BRN, nor does it wait for BGN for memory accesses for instruction or decision table fetching. These are assumed to be on the local bus. It may assert BRN and wait for BGN before an access to a data buffer in memory or to a peripheral device, depending on the state of the MSB ("A31" position) of the MAT or DAT entry for the channel, respectively.

If the bit that would correspond to A31 of the MAT or DAT entry has been set to 1 by MPU software, or a RELOAD instruction, the IOP does not assert BRN, nor does it wait for BGN. If the bit is cleared to 0, the IOP asserts BRN and waits for the MPU to return BGN low before proceeding to drive ASN low. While the IOP is waiting for BGN, it remains sensitive to the LBRN input. If LBRN goes low, the IOP defers the bus cycle, tri-states A23–A1 and the other bus control pins, and responds with LBGN low. When the cycle is completed and LBRN is released, the IOP reruns its bus cycle. This feature prevents a system deadlock if the IOP and MPU both request access to resources on each other's buses.

Dual bus applications tend towards higher performance by allowing the IOP to perform most of its bus cycles without stopping host processor execution, or without using the system's backplane bus. However, in this case the host processor must request control of the local bus in order to access memory or peripherals on the local bus, or to access IOP registers/RAM.

Bus Time-Out Facility

Whenever the IOP is accessing external memory or peripheral, it waits for DACKN to be asserted. In case of certain system malfunctions, this response may never occur. Therefore, the IOP includes a time-out counter that operates whenever it is waiting for DACKN (but not when it is waiting for BGN). The time-out field of the TOCTRL register should be programmed by the host MPU before the IOP operation is enabled, to reflect a time-out longer than the longest valid DACKN response time that is possible in the system. The IOP will wait for DACKN for 2^{t+7} CLK periods, where t is the value of the 3-bit time-out field. Thus, a time-out field value of 0 will cause the IOP to wait up to 128 CLK periods. A 1 designates waiting 256 CLK periods, and so forth through the maximum time-out value of 7 which will cause the IOP to wait up to 16,384 CLK periods. At a CLK frequency of 16MHz, these correspond to a range of 8 microseconds to 1 millisecond.

If the time-out value is exceeded, the IOP internally simulates an INT instruction, using the higher priority level if there are two levels, using the vector field of the TOCTRL register as the vector value. Thus, it asserts the IRQN pin if it had not been asserted previously. After doing this, it clears the dE bit in the CTRL register so that it no longer responds to any further request signals. The vector from TOCTRL should cause the host MPU to investigate the problem and take appropriate corrective action.

Typical Execution

This section describes the IOP operation. For the instructions, the following general rules apply for channel program execution.

1. A peripheral device asserts its "interrupt request" output. This signal is either directly connected to one of the IOP's RQn inputs, or is encoded externally to make the value on RQ4–RQ0.
2. The request is serviced when no higher-priority peripheral is making a request.
3. The IOP begins service for this peripheral by transferring the encoded channel number to the CHAN and TCHAN registers, and then loads the value in the corresponding entry from the PCT RAM into its program counter (PC). It then executes the "channel program" that starts at the location in external memory.

   Note that the PCT entry for a channel is initially loaded by the host MPU, and can be changed by a channel program thereafter, in response to changing status of the peripheral device.
4. A channel program will typically start with an INTERP instruction that reads a status register on the peripheral and then uses the status byte as an index to read a word from a "decision table" in memory.
5. The contents of the word from the decision table may cause the IOP to do either, both, or neither of two things: change (add to) the value in the CHAN register, and/or branch, i.e. reload the PC with a value in the decision table word or from PCT [new CHAN].

   The two actions above correspond to the kinds of information that a peripheral status byte may convey: in a multi-channel peripheral device, it identifies which channel needs service, and/or it identifies any exceptional conditions (e.g. errors) involved in its "interrupt request".

   For example, in a peripheral with separate input and output channels, the decision table words corresponding to an "output request" might be coded to add 2 to (CHAN) and branch, while those corresponding to an "input request" might do neither of those things.

   Note that a priority between such input and output channels is determined by coding of words corresponding to "both requests". Also that while the decision table mechanism might be considered wasteful in memory, it improves performance by processing a whole status byte "in parallel" to make a decision that an MPU interrupt service routine might make by means of a series of "bit test" and "branch" instructions.
6. With some peripheral devices, several status registers may have to be read to determine what is to be done. For example, with the 2698 each DUART has an individual interrupt request line, but within each one, each UART has its own status register. In such cases, the channel program might begin with several consecutive INTERP instructions, one for each status register. The decision table words could be set up to:

   a. if the status register value indicates there is something to be done, branch to a routine to do it, or

   b. if there is nothing to be done, increment CHAN to the value that corresponds to the next status register, and don't branch.
7. After the INTERP instruction(s) have routed control to the appropriate branch of the channel program based on the peripheral status, a branch that transfers data will use an INPUT or OUTPUT instruction to transfer data between memory and (one of) the peripheral's data register(s).
8. INPUT and OUTPUT instructions can also use the decision table structure, for applications in which data byte values affect what is to be done. For example, in receiving from a datacomm line, reception of a carriage return (CR) character might mean that the current input buffer in memory is "complete" and that the host MPU should be notified.

   Decision table processing for INPUT and OUTPUT instructions is slightly different from that for INTERP. As with INTERP, certain data characters can cause a branch, but instead of CHAN adjustment, decision table words for data are coded to control whether the byte is transferred to the destination (to memory for INPUT, to the device for OUTPUT).
9. An INPUT and OUTPUT instruction will typically be written so that it ends servicing for the channel unless a decision table causes a branch, or the byte count for the I/O buffer in memory is decremented to zero.
10. When an I/O buffer is completed, the channel program will typically interrupt the host MPU. Such interrupts are stored in a queue on the IOP, so that the host MPU is interrupted once for each time any IOP channel program posts an interrupt.
11. In addition to interrupting the host when an I/O buffer is completed, the channel program can either use a RELOAD instruction to get another I/O buffer from a circular list of such buffers, or send a command byte to the device to tell it to stop asserting its "interrupt request" line for this channel, until the host MPU responds to the interrupt posted by the channel program.

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

PARAMETER	RATING	UNIT
Operating ambient temperature range	0 to +70	°C
Storage temperature range	–65 to +150	°C
Supply voltage to ground	–0.5 to +6.5	V
Power dissipation	1	W

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperature, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
V_{IL}	Input low voltage			0.8	V
V_{IH}	Input high voltage		2.0		V
V_{OL}	Output low voltage	I_{OL} = 2.4mA		0.4	V
V_{OH}	Output high voltage (except open-drain outputs)	I_{OH} = –400µA	V_{CC} – 0.5		V
I_{IL}	Input leakage current	V_{IN} = 0 to V_{CC}	–1	1	µA
I_{LL}	Data bus 3-State leakage current	V_{IN} = 0 to V_{CC}	–1	1	µA
I_{CC}	Power supply current	Freq. = 16MHz		90	mA

AC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ±10%[1]

NO.	FIGURE	PARAMETER	LIMITS		UNIT
			Min	Max	
1	5	BCLK frequency (Balanced Clock – 50%DC)		12.5	MHz
2	5	(Unbalanced Clock)		16	MHz
3	5	BCLK width high (16MHz unnbalanced Clock)	20		ns
4	5	BCLK width low (16MHz unnbalanced Clock)	40		ns
		RESETN width low	1000		ns
Master Arbitration					
5	6	BCLK high to BRN low		60	ns
6	6	BRN low to BGN low	0		ns
7[1]	6	Setup, BGN low to BCLK low	10		ns
8	6	BCLK high to drivers enabled	2		ns
9	6	BCLK high to BRN high		60	ns
10	6	BRN high to drivers disabled	0	20	ns
11	6	BRN high to BGN high	0		ns
12[1]	6	Setup, BGN high to BCLK low	10		
Master Operation					
20	7, 8	BCLK high to A23:1 change	0		ns
21	7, 8	BCLK high to A23:1 valid		60	ns
22	7, 8	BCLK high to $\overline{W}$/R valid	0	60	ns
23	7, 8	BCLK high to M/IO valid	0	60	ns
24	7, 8	A23:1. $\overline{W}$/R. and M/IO valid to ASN low	20		ns
25	7, 8	BCLK high to ASN low	4	45	ns
26	7, 8	BCLK high to DHIEN and/or DLOEN low	4	45	ns
27	7	D15:0 valid (read) to DACKN low	0		ns
28[1]	7, 8	Setup, DACKN low to BCLK high	10		ns
29	7, 8	BCLK low to ASN high		50	ns
30	7, 8	BCLK low to DHIEN and DLOEN high		40	ns
31	7	Hold, read data valid after DHIEN and DLOEN high	0		ns
32	7, 8	DHIEN and DLOEN high to DACKN high (to avoid acknowledging next cycle)		t_{BCLK}	ns
34	8	BCLK high to data bus drivers enabled (write)	0		ns
35	8	BCLK high to write data valid		65	ns
36	8	Write data valid to DHIEN and/or DLOEN low	10		ns
37	8	Hold, write data valid after BCLK high	5		ns

AC ELECTRICAL CHARACTERISTICS (Continued)

NO.	FIGURE	PARAMETER	LIMITS Min	LIMITS Max	UNIT
Master Operation (cont.)					
38	8	BCLK high to data bus released (end of write)		30	ns
Slave Arbitration (Two Bus System)					
39[1]	9	Setup, LBRN low to BCLK low	10		ns
40	9	BCLK high to LBGN low		45	ns
41	9	BCLK high to IOP drivers disabled		30	ns
42	9	LBGN low to IOP drivers disabled		20	ns
43[1]	9	Setup, LBRN high to BCLK low	10		ns
44	9	LBRN high to LBGN high		45	ns
45	9	BCLK high to IOP drivers enabled	10		ns
Slave Operation					
47	10, 11	Setup, A8:1 valid to CSN low	0		ns
48	10, 11	Setup, $\overline{W}$/R valid to CSN low	0		ns
49	10, 11	Setup, DHIEN and/or DLOEN low to CSN low	0		ns
50[1]	11, 12	Setup, CSN low to BCLK low	10		ns
51[3]	10, 11, 12	IOP response latency	$3t_{BCLK}$	$11t_{BCLK}$	ns
53	10, 11	BCLK low to data bus valid (read or IACK)		70	ns
54	10, 11, 12	BCLK low to DACKN low		40	ns
55	10, 11	DACKN low to CSN high or (DHIEN and DLOEN high)	0		ns
56	10	Data bus valid after CSN high or (DHIEN and DLOEN high)	10		ns
57	10	CSN high or (DHIEN and DLOEN high) to data bus released		30	ns
58	10, 11	CSN high or (DHIEN and CLOEN high) to DACKN released		30	ns
59	10, 11	Hold, A8:1 valid after CSN high or (DHIEN and DLOEN high)	0		ns
60	10, 11	Hold, $\overline{W}$/R valid after CSN high or (DHIEN and DLOEN high)	0		ns
61	10, 11	CSN width high (intercycle)	t_{BCLK}		ns
62	11	Setup, data bus valid (write) to CSN low	0		ns
63	12	Hold, write data valid after CSN high or (DHIEN and DLOEN high)	0		ns
64[1]	12	Setup, IACKN low to BCLK low	10		ns
65	12	BCLK low to IRQN released		70	ns
66	12	DACKN low to IACKN high	0	50	ns
67[1]	12	Setup, IACKN high to BCLK low	10		ns
68	12	Hold, data bus valid after IACKN high	10		ns
69	12	IACKN high to data bus released		30	ns
70	12	IACKN high to DACKN released		35	ns

NOTES:

1. If the subject input signal meets this setup time, the IOP is guaranteed to recognize its new state at the subject edge of BCLK. If this setup time is not met, recognition may occur at the subject clock edge, or one BCLK later.
2. The maximum rating of this parameter should be as short as is consistent with device characterization, so as to maximize the compatibility of the IOP with processors that re-arbitrate and re-grant if BR is kept low after a first grant.
3. This parameter defines the number of clock cycles (wait states) between the BCLK falling edge at which CSN or IACKN is sampled and the falling edge from which the IOP responds with DACKN low, which is a function of the IOP's internal state and activity. For accesses to DMA processor registers when the IOP is idle, 3 BCLK cycles are required. If the IOP is internally active at the same time CSN or IACKN goes low, up to 11 BCLK cycles may be needed.

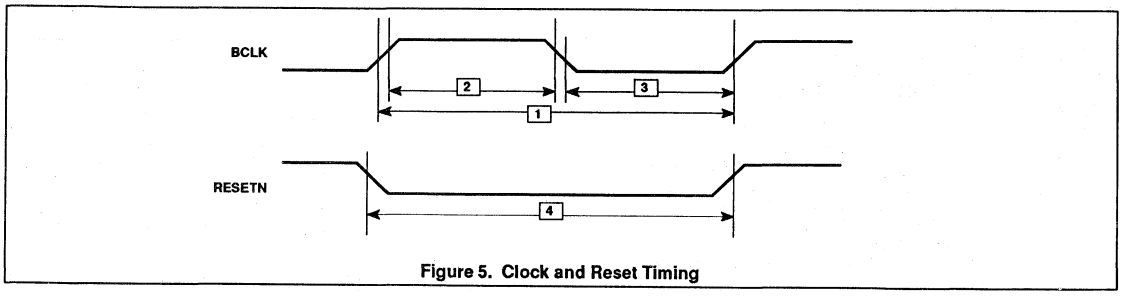


Figure 5. Clock and Reset Timing

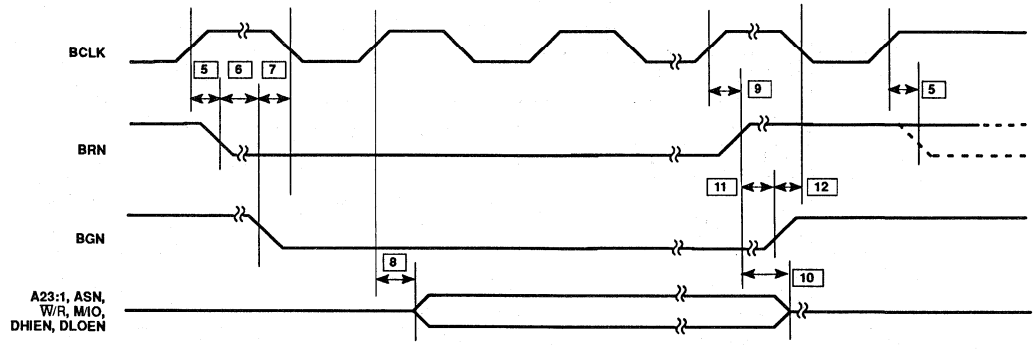


Figure 6. Two Wire Master Arbitration

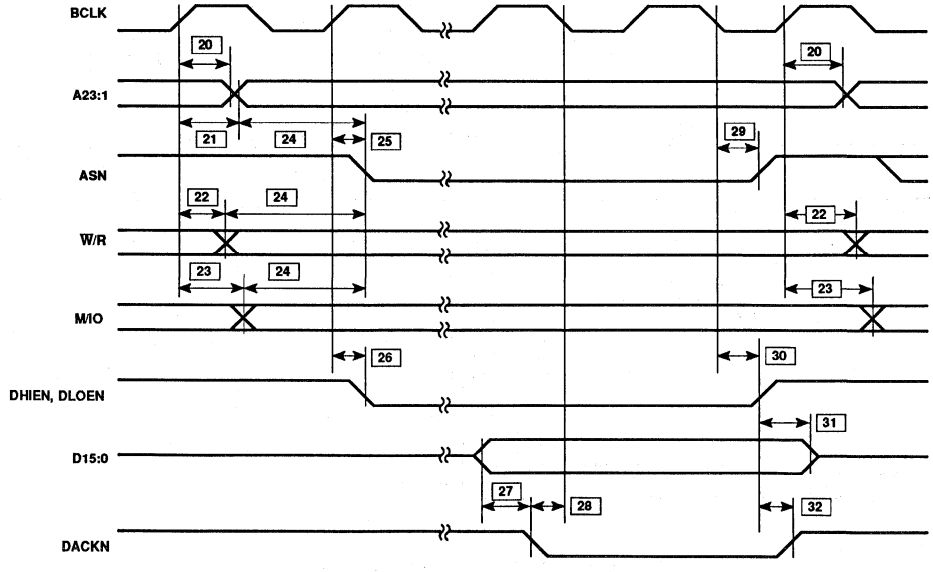


Figure 7. IOP Read From External Peripheral or Memory

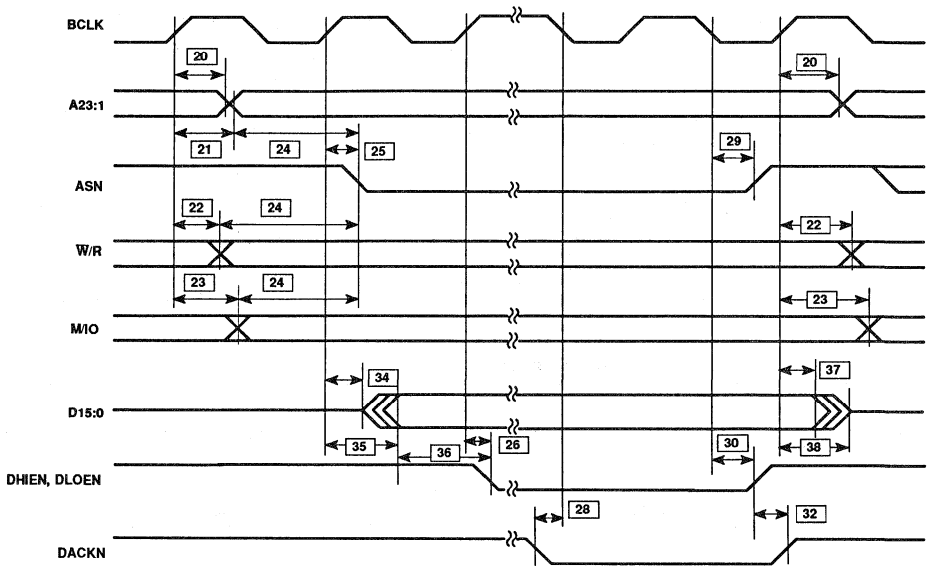


Figure 8. IOP Write to External Peripheral or Memory

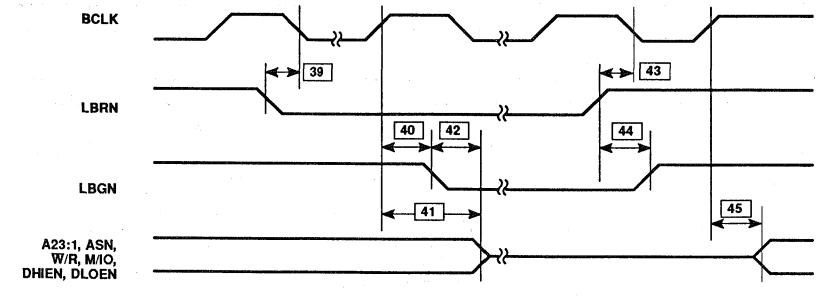


Figure 9. Dual Bus "Slave" Arbitration

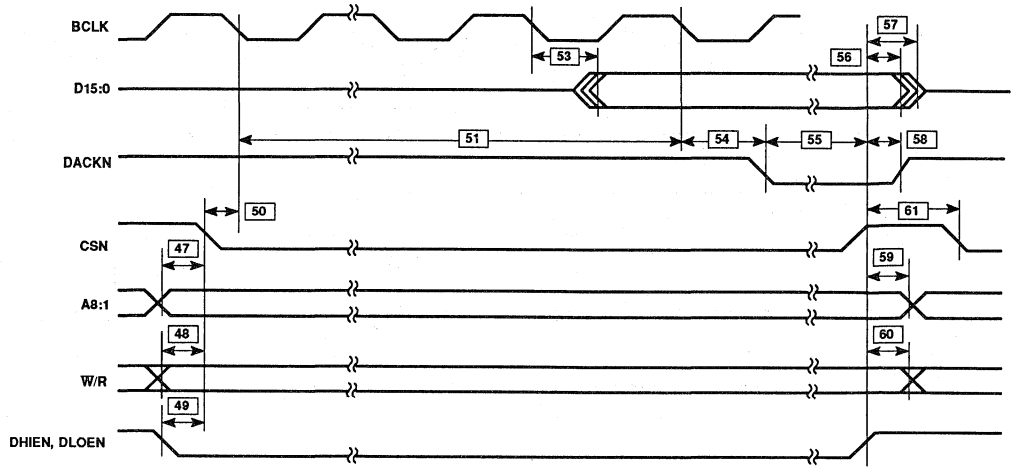


Figure 10. Host MPU Read From IOP

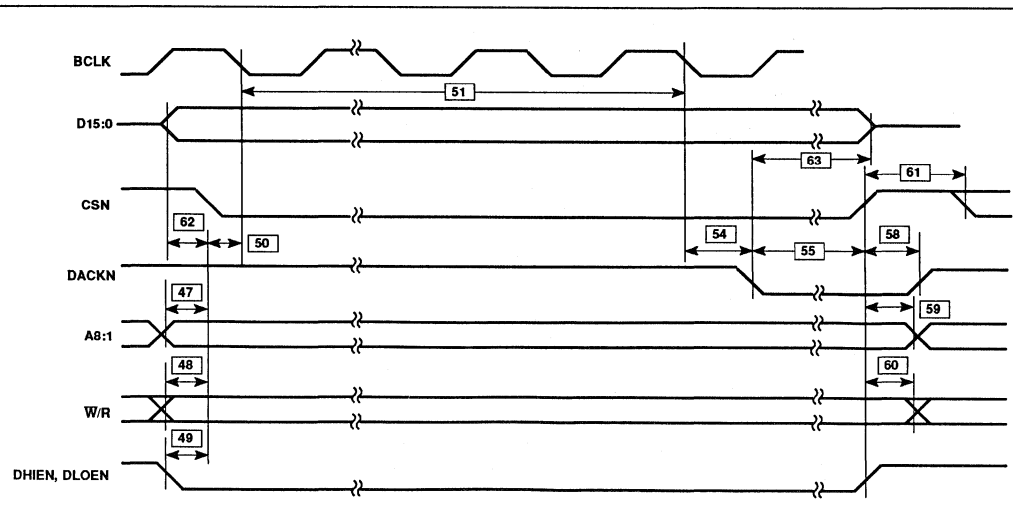


Figure 11. Host MPU Write to IOP

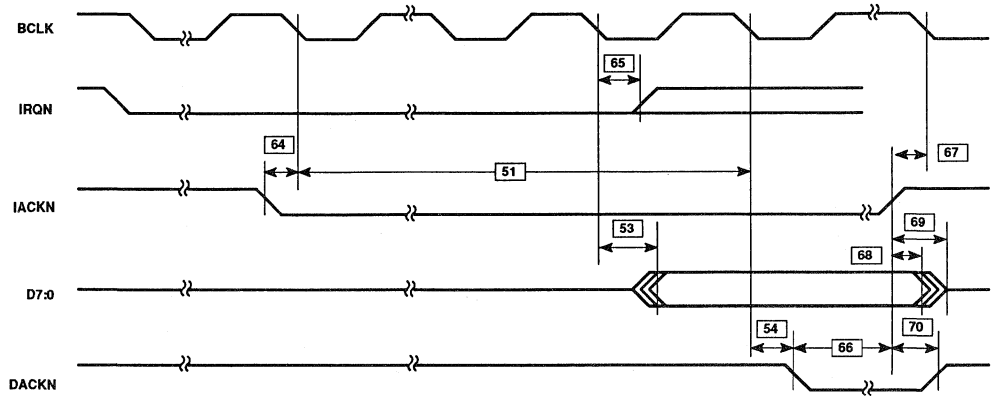


Figure 12. Interrupt Acknowledge Cycle by Host MPU

Section 3
Linear Data Communications Data Sheets

INDEX

EIA-232-D/V.28 driver/receiver | MC145406

DESCRIPTION

The MC145406 is a silicon-gate CMOS IC that combines 3 drivers and 3 receivers to fulfill the electrical specifications of standards EIA-232-D and CCITT V.28. The drivers feature true TTL input compatibility, slew-rate limited output, 300Ω power-off source impedance, and output typically switching to within 25% of the supply rails. The receivers can handle up to ±25V while presenting 3 to 7kΩ impedance. Hysteresis in the receiver aids reception of noisy signals. By combining both drivers and receivers in a single CMOS chip, the MC145406 provides efficient, low-power solutions for EIA-232-D and V.28 applications.

FEATURES

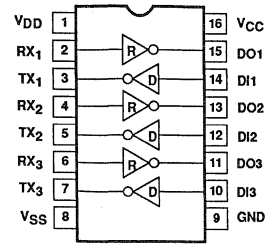
- **Drivers**
- ±5 to ±12V supply range
- 300Ω power-off source impedance
- Output current limiting
- TTL compatible
- Maximum slew rate = 30V/μs
- **Receivers**
- ±25V input voltage range over the full supply range
- 3 to 7kΩ input impedance
- Hystersis on input switchpoint
- **General**
- Very low supply currents for long battery life
- Operation is independent of power supply sequencing

APPLICATIONS

- Modem interface
- Voice/data telephone interface
- Lap-top computers
- UART interface

PIN CONFIGURATION

D and N Packages

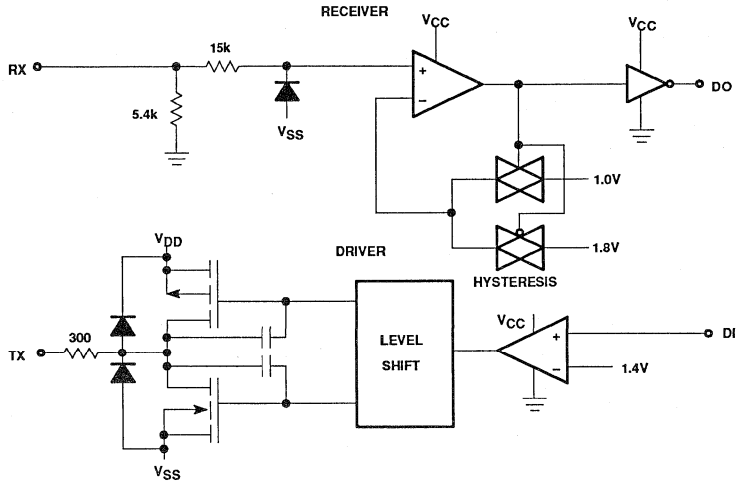


NOTE:
D = Driver
R = Receiver

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	MC145406N
16-Pin SOL	0 to +70°C	MC145406D

BLOCK DIAGRAM



PIN #	SYMBOL	PIN DESCRIPTION
1	V_{DD}	**Positive power supply**. The most positive power supply pin, which is typically 5 to 12 volts.
8	V_{SS}	**Negative power supply.** The most negative power supply pin, which is typically -5 to -12 volts.
16	V_{CC}	**Digital power supply**. The digital supply pin, which is connected to the logic power supply (maximum +5.5V).
9	GND	**Ground.** Ground return pin is typically connected to the signal ground pin of the EIA-232-D connector (Pin 7) as well as to the logic power supply ground.
2, 4, 6	RX_1, RX_2, RX_3	**Receive Data Input.** These are the EIA-232-D receive signal inputs whose voltages can range from +25 to -25V. A voltage between +3 and +25 is decoded as a space and causes the corresponding DO pin to swing to ground (0V); a voltage between -3 and -25V is decoded as a mark and causes the DO pin to swing up to V_{CC}. The actual turn-on input switchpoint is typically biased at 1.8V above ground, and includes 800mV of hysteresis for noise rejection. The nominal input impedance is 5kΩ. An open or grounded input pin is interpreted as a mark, forcing the DO pin to V_{CC}.
11, 13, 15	DO1, DO2, DO3	**Data Output.** These are the receiver digital output pins, which swing from V_{CC} to GND. A space on the RX pin causes DO to produce a logic zero; a mark produces a logic one. Each output pin is capable of driving one LSTTL input load.
10, 12, 14	DI1, DI2, DI3	**Data Input.** These are the high-impedance digital input pins to the drivers. TTL compatibility is accomplished by biasing the input switchpoint at 1.4V above ground. However, 5V CMOS compatibility is maintained as well. Input voltage levels on these pins must be between V_{CC} and GND.
3, 5, 7	TX1, TX2, TX3	**Transmit Data Output.** These are the EIA-232-D transmit signal output pins, which swing toward V_{DD} and V_{SS}. A logic one at a DI input causes the corresponding TX output to swing toward V_{SS}. A logic zero causes the output to swing toward V_{DD} (the output voltages will be slightly less than V_{DD} or V_{SS} depending upon the output load). Output slew rates are limited to a maximum of 30V/μs. When the MC145406 is off (V_{DD} = V_{SS} = V_{CC} = GND), the minimum output impedance is 300Ω.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +6.0	V
V_{DD}	Supply voltage	-0.5 to +13.5	V
V_{SS}	Supply voltage	+0.5 to -13.5	V
V_{IR}	Input voltage range RX_{1-3} inputs DI_{1-3} inputs	 $(V_{SS} - 15)$ to $(V_{DD} + 15)$ -0.5 to $(V_{CC} + 0.5)$	V
	DC current per pin	±100	mA
P_D	Power dissipation (package)	1.0	W
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
θ_{JA}	Thermal impedance N package D package	80 105	°C/W

NOTE: This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that the voltages at the DI and DO pins be constrained to the range GND ≤ V_{DI} ≤ V_{DD} and GND ≤ V_{DO} ≤ V_{CC}. Also, the voltage at the RX pin should be constrained to ±25V, and TX should be constrained to V_{SS} ≤ V_{TX1-3} ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., GND or V_{CC} for DI, and V_{SS} or V_{DD} for RX).

DC ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 0 to 70°C; GND = 0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
DC supply voltage						
V_{DD}			4.5	5 to 12	13.2	V
V_{SS}			-4.5	-5 to -12	-13.2	V
V_{CC}			4.5	5.0	5.5	V
Quiescent supply current (outputs unloaded, inputs low)						
I_{DD}		V_{DD} = +12V		20	400	µA
I_{SS}		V_{SS} = -12V		280	600	µA
I_{CC}		V_{CC} = +5V		260	450	µA

RECEIVER ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 0 to 70°C; GND = 0V; V_{DD} = +5 to +12V; V_{SS} = -5 to -12V; V_{CC} = +5V ±5%, unless otherwise specified.

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNITS
				MIN	TYP	MAX	
V_{ON}	Input turn-on threshold	RX_{1-3}	V_{DO1-3} = V_{OL}, V_{CC} = 5.0V ±5%	1.35	1.80	2.35	V
V_{OFF}	Input turn-off threshold	RX_{1-3}	V_{DO1-3} = V_{OH}, V_{CC} = 5.0V ±5%	0.75	1.00	1.25	V
V_{ON}-V_{OFF}	Input threshold hysteresis	RX_{1-3}	V_{CC} = 5.0V ±5%	0.6	0.8		V
R_{IN}	Input resistance	RX_{1-3}	$(V_{SS}$-15V) ≤ V_{RX1-3} ≤ $(V_{DD}$+15V)	3.0	5.0	7.0	kΩ
V_{OH}	High level output voltage	DO_{1-3}	I_{OH} = -20µA, V_{CC} = +5.0V	4.9	5.0		V
	V_{RX1-3} = -3V to $(V_{SS}$-15V)[1]		I_{OH} = -1mA, V_{CC} = +5.0V	3.8	4.4		V
V_{OL}	Low level output voltage	DO_{1-3}	I_{OL} = +20µA, V_{CC} = +5.0V		0.005	0.1	V
	V_{RX1-3} = +3V to $(V_{DD}$+15V)[1]		I_{OL} = +2mA, V_{CC} = +5.0V		0.15	0.5	V
			I_{OL} = +4mA, V_{CC} = +5.0V		0.3	0.7	V

NOTE:
1. This is the range of input voltages as specified by EIA-232-D to cause a receiver to be in the high or low logic state.

DRIVER ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 0 to 70°C; GND = 0V; V_{CC} = +5V ±5%, unless otherwise specified.

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNITS
				MIN	TYP	MAX	
V_{IL}	Digital input voltage	DI_{1-3}	Logic 0			0.8	V
V_{IH}	Digital input voltage	DI_{1-3}	Logic 1	2.0			V
I_{IN}	Input current	DI_{1-3}	$V_{DI1-3} = V_{CC}$			±1.0	µA
V_{OH}	Output high voltage V_{DI1-3} = Logic 0, R_L = 3.0kΩ	TX_{1-3}	V_{DD} = +5.0V, V_{SS} = -5.0V	3.5	4.1		V
			V_{DD} = +6.0V, V_{SS} = -6.0V	4.3	5.0		V
			V_{DD} = +12.0V, V_{SS} = -12.0V	9.2	10.4		V
V_{OL}	Output low voltage[1] V_{DI1-3} = Logic 0, R_L = 3.0kΩ	TX_{1-3}	V_{DD} = +5.0V, V_{SS} = -5.0V	-4.0	-4.3		V
			V_{DD} = +6.0V, V_{SS} = -6.0V	-4.5	-5.2		V
			V_{DD} = +12.0V, V_{SS} = -12.0V	-10.0	-10.3		V
	Off source resistance Figure 1	TX_{1-3}	V_{DD}=V_{SS}=GND=0V, V_{TX1-3} = ±2.0V	300			Ω
I_{SC}	Output short-circuit current V_{DD} = +12.0V, V_{SS} = -12.0V	TX_{1-3}	TX_{1-3} shorted to GND[2]		±22	+60	mA
			TX_{1-3} shorted to ±15.0V[3]		±60	±100	mA

NOTE:
1. The voltage specifications are in terms of absolute values.
2. Specification is for one TX output pin to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits will be exceeded.
3. This condition could exceed package limitations.

SWITCHING CHARACTERISTICS

Typical values are at T_A = 0 to 70°C; V_{CC} = +5V ±5%, unless otherwise specified. (See Figures 2 and 3)

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNITS
				MIN	TYP	MAX	
Drivers							
t_{PLH}	Propagation delay time	TX_{1-3}	Low-to-High R_L = 3kΩ, C_L = 50pF		300	500	ns
t_{PHL}	Propagation delay time	TX_{1-3}	High-to-Low R_L = 3kΩ, C_L = 50pF		300	500	ns
SR	Output slew rate (minimum load)	TX_{1-3}	R_L = 7kΩ, C_L = 0pF, V_{DD} = 6 to 12.0V, V_{SS} = -6 to -12V		±6	±30	V/µs
	Output slew rate (maximum load)	TX_{1-3}	R_L = 7kΩ, C_L = 2500pF, V_{DD} = 12V, V_{SS} = -12V		±3.0		V/µs
Receivers (C_L = 50pF)							
t_{PLH}	Propagation delay time	DO_{1-3}	Low-to-High		150	425	ns
t_{PHL}	Propagation delay time	DO_{1-3}	High-to-Low		150	425	ns
t_R	Output rise time	DO_{1-3}			120	400	ns
t_F	Output fall time	DO_{1-3}			40	100	ns

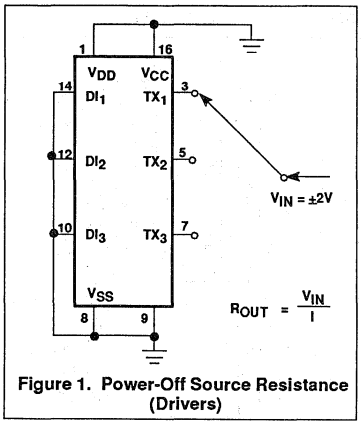


Figure 1. Power-Off Source Resistance (Drivers)

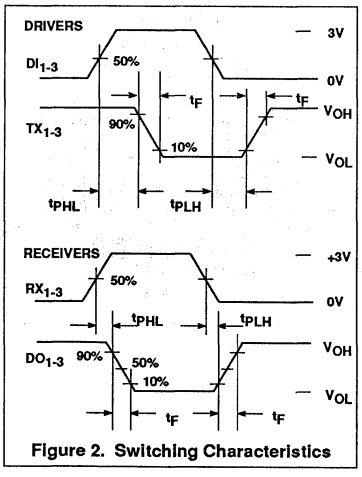


Figure 2. Switching Characteristics

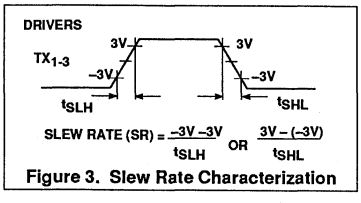


Figure 3. Slew Rate Characterization

APPLICATIONS INFORMATION

The MC145406 has been designed to meet the electrical specifications of standards EIA-232-D/CCITT V.28 and as such, defines the elctrical and physical interface between Data Communication Equipment (DCE) and Data Terminal Equipment (DTE). A DCE is connected to a DTE using a cable that typically carries up to 25 leads, which allow the transfer of timing, data, control, and test signals. The MC145406 provides the necessary level shifting between the TTL/CMOS logic levels and the high voltage levels of EIA-232-D (ranging from ±3 to ±25V).

DRIVERS

As defined by the specification, an EIA-232-D driver presents a voltage of between ±5 to ±15V into a load of between 3 to 7kΩ. A logic one at the driver input results in a voltage of between -5 to -15V. A logic zero results in a voltage between ±5 to ±15V. When operating at ±7 to ±12V, the MC145406 meets this requirement. When operating at ±5V, the MC145406 drivers produce less than ±5V at the output (when terminated), which does not meet the EIA-232-D specification. However, the output voltages when using a ±5V power supply are high enough (around ±4V) to permit proper reception by an EIA-232-D receiver, and can be used in applications where strict compliance to EIA-232-D is not required.

Another requirement of the MC145406 drivers is that they withstand a short to another driver in the EIA-232-D cable. The worst-case condition that is permitted by EIA-232-D is a ±15V source that is current limited to 500mA. The MC145406 drivers can withstand this condition momentarily. In most short circuit conditions the source driver will have a series 300Ω output impedance needed to satisfy the EIA-232-D driver requirements. This will reduce the short circuit current to under 40mA which is an acceptable level for the MC145406 to withstand.

Unlike some other drivers, the MC145406 drivers feature an internally-limited output slew rate that does not exceed 30V/µs.

RECEIVERS

The job of an EIA-232-D receiver is to level-shift voltages in the range of -25 to +25V down to TTL/CMOS logic levels (0 to +5V). A voltage of between -3 and -25V on RX_1 is defined as a mark and produces a logic one at DO_1. A voltage between +3 and +25V is a space and produces a logic zero. While receiving these signals, the RX inputs must present a resistance between 3 and 7kΩ. Nominally, the input resistance of the RX_{1-3} inputs is 5.0kΩ.

The input threshold of the RX_{1-3} inputs is typically biased at 1.8V above ground (GND) with typically 800mV of hysteresis included to improve noise immunity. The 1.8V bias forces the appropriate DO pin to a logic one when its RX input is open or grounded as called for in EIA-232-D specification. Notice that TTL logic levels can be applied to the RX inputs in lieu of normal EIA-232-D signal levels. This might be helpful in situations where access to the modem or computer through the EIA-232-D connector is necessary with TTL devices. However, it is important not to connect the EIA-232-D outputs (TX_1) to TTL inputs since TTL operates off +5V only, and may be damaged by the high output voltage of the MC145406.

The DO outputs are to be connected to a TTL or CMOS input (such as an input to a modem chip). These outputs will swing from V_{CC} to ground, allowing the designer to operate the DO and DI pins from the digital power supply. The TX and RX sections are independently powered by V_{DD} and V_{SS} so that one may run logic at +5V and the EIA-232-D signals at ±12V.

Octal line driver

NE5170

DESCRIPTION

The NE5170 is an octal line driver which is designed for digital communications with data rates up to 100kb/s. This device meets all the requirements of EIA standards RS-232C/RS-423A and CCITT recommendations V.10/X.26. Three programmable features:
(1) output slew rate, (2) output voltage level, and (3) three-state control (high-impedance) are provided so that output characteristics may be modified to meet the requirements of specific applications.

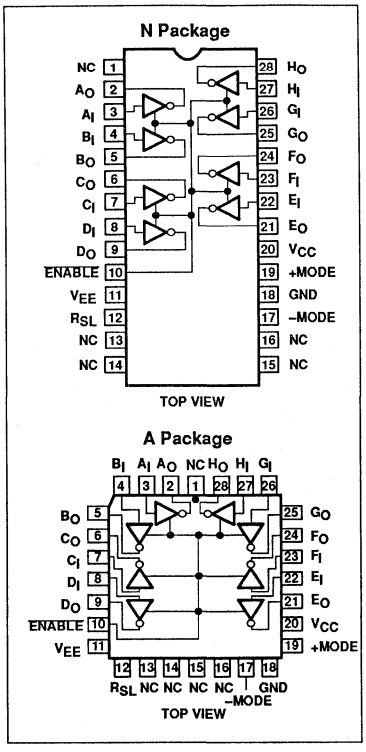
FEATURES

- Meets EIA RS-232C/423A and CCITT V.10/X.26
- Simple slew rate programming with a single external resistor
- 0.1 to 10V/μs slew rate range
- High/low programmable voltage output modes
- TTL compatible inputs

APPLICATIONS

- High-speed modems
- High-speed parallel communications
- Computer I/O ports
- Logic level translation

PIN CONFIGURATION



FUNCTION TABLE

ENABLE	Logic Input	OUTPUT VOLTAGE (V)		
		RS-423A[1]	RS-232C	
			Low Output Mode[1]	High Output Mode[3]
L	L	5 to 6V	5 to 6V	≥ 9V
L	H	–5 to 6V	–5 to 6V	≤ –9V
H	X	High-Z	High-Z	High-Z

NOTES:
1. V_{CC} = +10V and V_{EE} = –10V; R_L = 3kΩ
2. V_{CC} = +12V and V_{EE} = –12V; R_L = 3kΩ

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP	0 to +70°C	NE5170N
28-Pin PLCC	0 to +70°C	NE5170A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage and + MODE	15	V
V_{EE}	Supply voltage and – MODE	–15	V
I_{OUT}	Output current[1]	±150	mA
V_{IN}	Input voltage ($\overline{\text{Enable}}$, Data)	–1.5 to +7	V
V_{OUT}	Output voltage[2]	±15	V
	Minimum slew resistor[3]	1	kΩ
P_D	Power dissipation	1200	mW

NOTES:
1. Maximum current per driver. Do not exceed maximum power dissipation if more than one output is on.
2. High impedance mode.
3. Minimum value of the resistor used to set the slew rate.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 10V ±10%; V_{EE} = –10V ±10%; ±MODES = 0V; R_{SL} = 2kΩ, 0°C ≤ T_A ≤ 70°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
V_{OH}	Output high voltage	V_{IN} = 0.8V R_L = 3kΩ[2]	5	6	V
		R_L = 450Ω[2]	4.5	6	
		R_L = 3kΩ[3], C_L = 2500pF	V_{CC}–3		
V_{OL}	Output low voltage	V_{IN} = 2.0V R_L = 3kΩ[2]	–6	–5	V
		R_L = 450Ω[2]	–6	–4.5	
		R_L = 3kΩ[3], C_L = 2500pF		V_{EE}+3	
V_{OU}	Output unbalance voltage	V_{CC} = |V_{EE}|, R_L = 450Ω[2]		0.4	V
I_{CEX}	Output leakage current	|V_O| = 6V, ENABLE = 2V or V_{CC} = V_{EE} = 0V	–100	100	µA
V_{IH}	Input high voltage		2.0		V
V_{IL}	Input low voltage			0.8	V
I_{IL}	Logic "0" input current	V_{IN} = 0.4V	–400	0	µA
I_{IH}	Logic "1" input current	V_{IN} = 2.4V	0	40	µA
I_{OS}	Output short circuit current[1]	V_O = 0V	–150	150	mA
V_{CL}	Input clamp voltage	I_{IN} = –15mA	–1.5		V
I_{CC}	Supply current	NO LOAD		35	mA
I_{EE}		NO LOAD	–45		mA

NOTES:
1. Maximum current per driver. Do not exceed maximum power dissipation if more than one output is on.
2. V_{OH}, V_{OL} at R_L = 450Ω will be ≥ 90% of V_{OH}, V_{OL} at R_L = ∞.
3. High Output Mode; +MODE pin = V_{CC}; –MODE pin = V_{EE}; 9V ≤ V_{CC} ≤ 13V; –9V ≥ V_{EE} ≥ –13V.

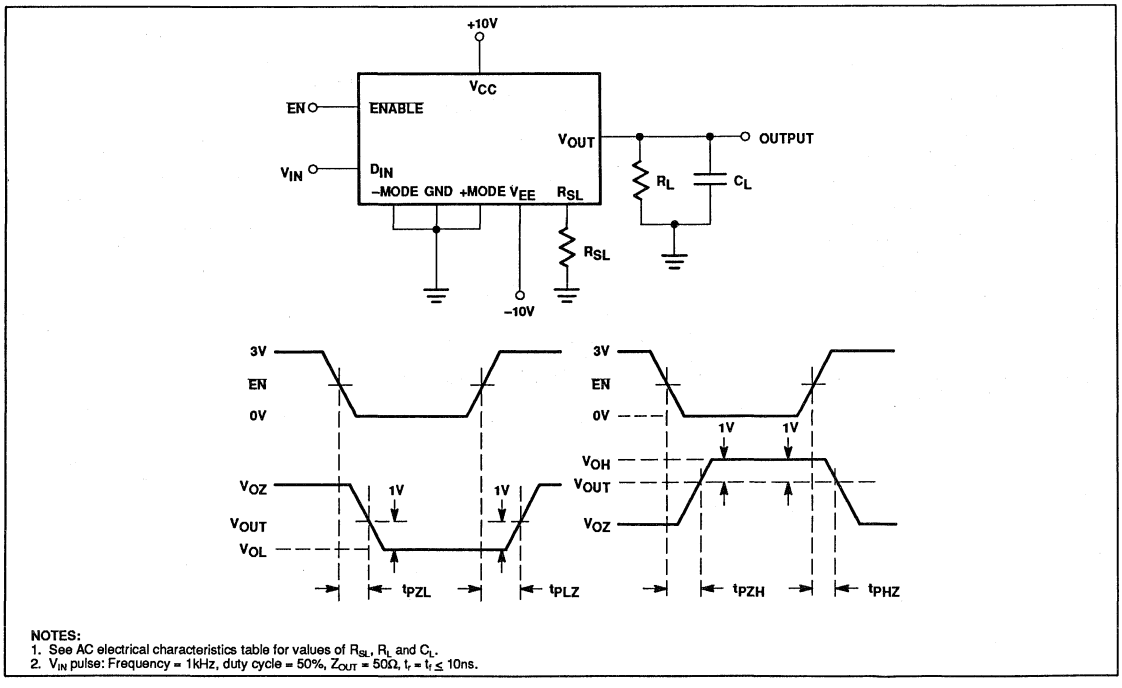
AC ELECTRICAL CHARACTERISTICS

V_{CC} = +10V; V_{EE} = −10V; Mode = GND, 0°C ≤ T_A ≤ 70°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_{PHZ}	Propagation delay output high to high impedance	R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		5	µs
t_{PLZ}	Propagation delay output low to high impedance	R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		5	µs
t_{PZH}	Propagation delay high impedance to high output	R_{SL} = 200k R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		150	µs
t_{PZL}	Propagation delay high impedance to low output	R_{SL} = 200k R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		150	µs
SR	Output slew rate[1]	R_{SL} = 2k	8	12	V/µs
		R_{SL} = 20k	0.8	1.2	
		R_{SL} = 200k	0.06	0.14	

NOTE:
SR: Load condition. (A) For R_{SL} < 4kΩ use R_L = 450Ω; C_L = 50pF; (B) for R_{SL} > 4kΩ use either R_L = 450Ω, C_L = 50pF or R_L = 3kΩ, C_L = 2500pF.

AC PARAMETER TEST CIRCUIT AND WAVEFORMS



NOTES:
1. See AC electrical characteristics table for values of R_{SL}, R_L and C_L.
2. V_{IN} pulse: Frequency = 1kHz, duty cycle = 50%, Z_{OUT} = 50Ω, $t_r = t_f \leq$ 10ns.

SLEW RATE PROGRAMMING

Slew rate for the NE5170 is set using a single external resistor connected between the R_{SL} pin and ground. Adjustment is made according to the formula:

$$R_{SL}\ (\text{in k}\Omega) = \frac{20}{\text{Slew Rate}}$$

where the slew rate is in V/μs. The slew resistor can vary between 2 and 200kΩ which gives a slew rate range of 10 to 0.1V/μs. This adjustment of the slew rate allows tailoring output characteristics to recommendations for cable length and data rate found in EIA standard RS–423A. Approximations for cable length and data rate are given by:

Max. data rate (in kb/s) = 300/t

Cable length (in feet) = 100×t

where t is the rise time in microseconds. The absolute maximum data rate is 100kb/s and the absolute maximum cable length is 4000 feet.

OUTPUT MODE PROGRAMMING

The NE5170 has two programmable output modes which provide different output voltage levels. The low output mode meets the specifications of EIA standards RS–423A and RS–232C. The high output mode meets the specifications of RS–232C only, since higher output voltages result from programming this mode. The high output mode provides the greater output voltages where higher attenuation levels must be tolerated. Programming the high output mode is accomplished by connecting the +MODE pin to V_{CC} and the –MODE pin to V_{EE}. The low output mode results when both of these pins are connected to ground.

APPLICATION

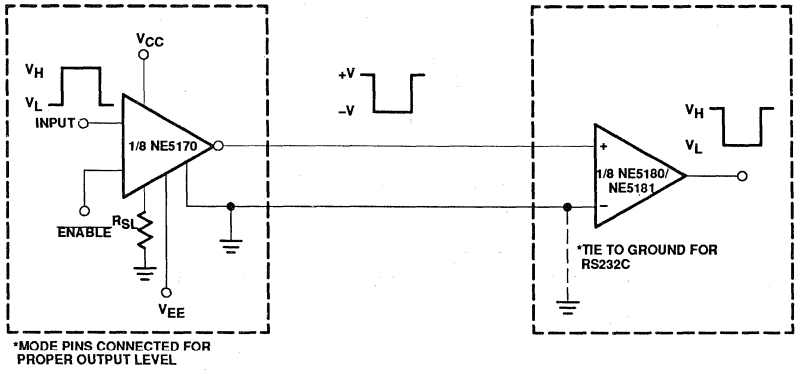


Figure 1. RS-232C/RS-423A Data Transmission

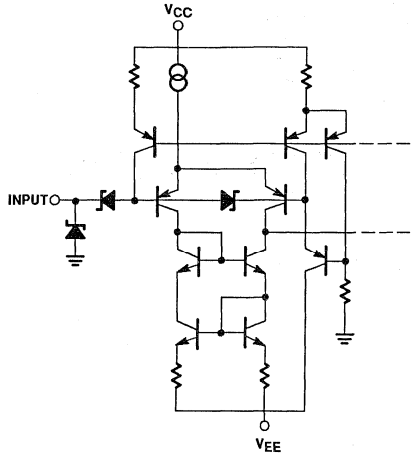


Figure 2. Input Stage Schematic

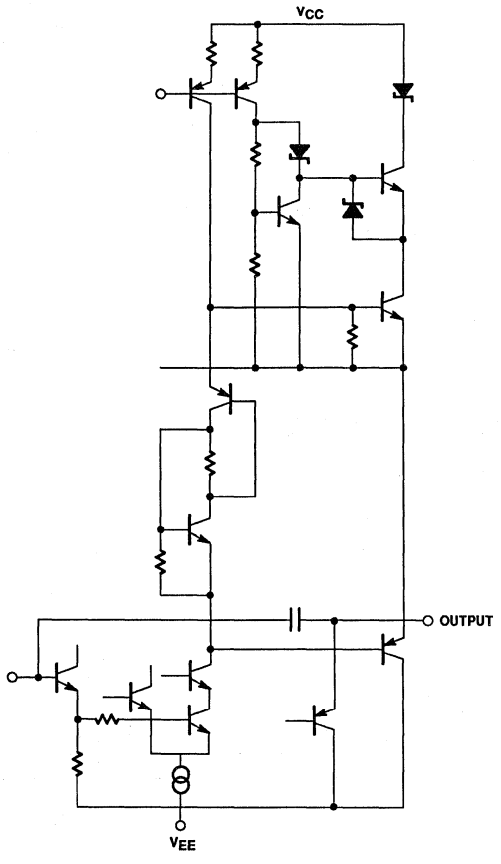


Figure 3. Output Stage Schematic

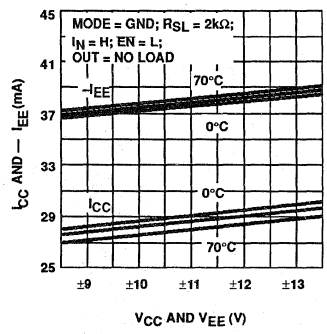


Figure 4. Typical I_{CC} and I_{EE} vs Supply Voltages

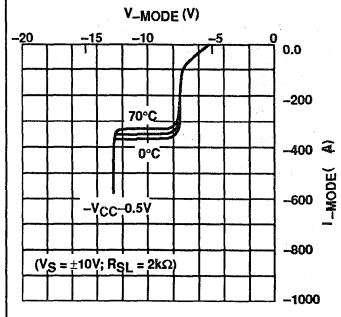


Figure 7. Typical –MODE Current vs –MODE Voltage

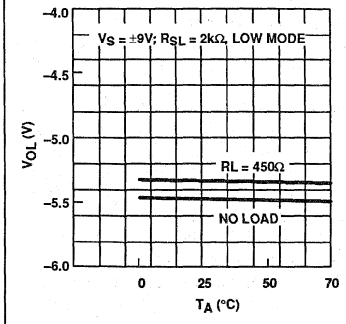


Figure 10. Typical Output Low Voltage vs Temperature

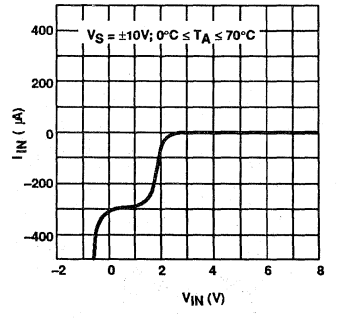


Figure 5. Typical Input Current vs Input Voltage

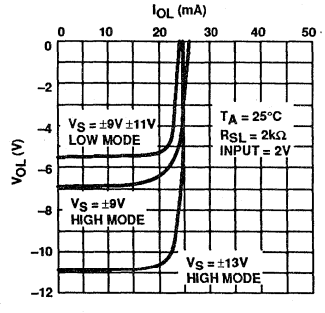


Figure 8. Typical Output Low Voltage vs Load Current

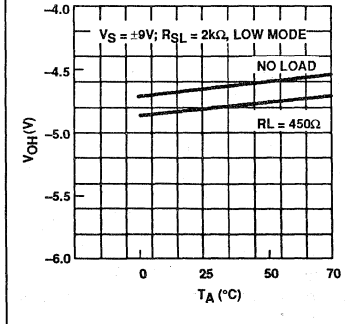


Figure 11. Typical Output High Voltage vs Temperature

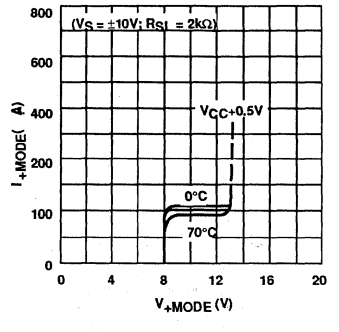


Figure 6. Typical +MODE Current vs +MODE Voltage

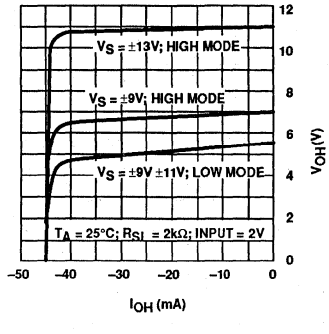


figure 9. Typical Output High Voltage vs Load Current

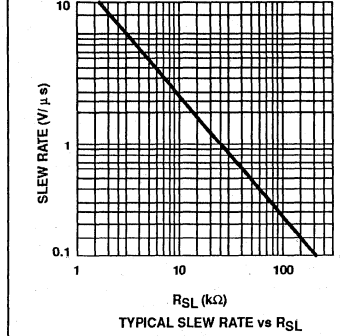


Figure 12. Typical Slew Rate vs R_{SL}

Octal differential line receiver

NE5180/NE5181

DESCRIPTION

The NE5180 and NE5181 are octal line receivers designed to interface data terminal equipment with data communications equipment. These devices meet the requirements of EIA standards RS-232C, RS-423A, RS-422A, and CCITT V.10, V.11, V.28, X.26 and X.27. The NE5180 is intended for use where the data transmission rate is up to 200 kb/s. The NE5181 covers the entire range of data rates up to 10 Mb/s. The difference in data rates for the two devices results from the input filtering of the NE5180. These devices also provide a failsafe feature which protects against certain input fault conditions.

FEATURES

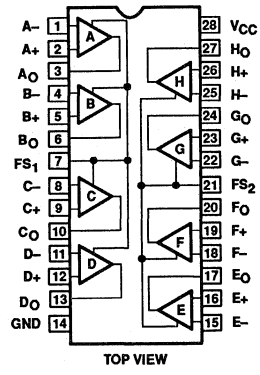
- Meets EIA RS-232C/423A/422A and CCITT V.10, V.11, V.28
- Single +5V supply—TTL compatible outputs
- Differential inputs withstand ±25V
- Failsafe feature
- Input noise filter (NE5180 only)
- Internal hysteresis
- Available in SMD PLCC

APPLICATIONS

- High-speed modems
- High-speed parallel communications
- Computer I/O ports
- Logic level translation

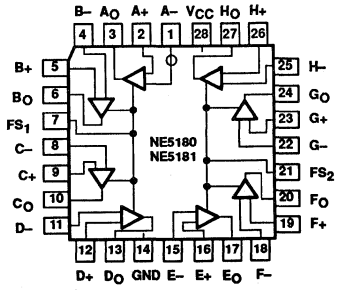
PIN CONFIGURATION

N Package



TOP VIEW

A Package



TOP VIEW

FUNCTION TABLE

INPUT	FAILSAFE INPUT	LOGIC OUTPUT
$V_{ID} < 200mV^1$	X	H
$V_{ID} < -200mV^1$	X	L
Both inputs open or grounded	0V	L
	V_{CC}	H

NOTE:
1. V_{ID} is defined as the non-inverting terminal input voltage minus the inverting terminal input voltage.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP	0 to +70°C	NE5180N
28-Pin Plastic DIP	0 to +70°C	NE5181N
28-Pin PLCC	0 to +70°C	NE5180A
28-Pin PLCC	0 to +70°C	NE5181A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
P_D	Power dissipation	800	mW
V_{CC}	Supply voltage	7	V
V_{CM}	Common mode range	±15	V
V_{ID}	Differential input voltage	±25	V
I_{SINK}	Outputsink current	50	mV
V_{FS}	Failsafe voltage	–0.3 to V_{CC}	V
J_{OS}	Output short-circuit time	1	sec

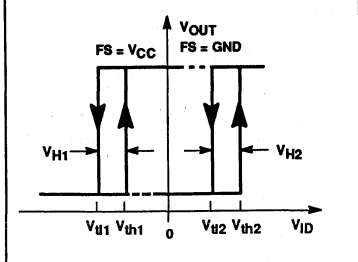


Figure 1. V_{tl}, V_{th}, V_H Definitions

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V ±5%, 0°C ≤ T_A ≤ +70°C, input common-mode range ±7V

SYMBOL	PARAMETER	TEST CONDITIONS		NE5180 Min	NE5180 Max	NE5181 Min	NE5181 Max	UNIT
R_{IN}	DC input resistance	3V ≤ $\|V_{IN}\|$ ≤ 25V		3	7	3	7	kΩ
V_{OFS}	Failsafe output voltage	Inputs open or shorted to GND	0 ≤ I_{OUT} ≤ 8mA, $V_{failsafe}$ = 0V		0.45		0.45	V
			0 ≥ I_{OUT} ≥ −400µA, $V_{failsafe}$ = V_{CC}	2.7		2.7		
V_{th}	Differential input high[4] threshold	V_{OUT} ≥ 2.7V, I_{OUT} = −440µA	R_S = 0[1]		0.2		0.2	V
			R_S = 500[1]		0.4		0.4	
V_{tl}	Differential input low[4] threshold	V_{OUT} ≤ 0.45V, I_{OUT} = 8mA	R_S = 0[1]	−0.2		−0.2		V
			R_S = 500[1]	−0.4		−0.4		
V_H	Hysteresis[4]	FS = 0V or V_{CC} (See Figure 1)		50	140	50	140	mV
V_{IOC}	Open-circuit input voltage				2		2	V
C_I	Input capacitance				30		30	pF
V_{OH}	High level output voltage	V_{ID} = 1V, I_{OUT} = −440µA		2.7		2.7		V
V_{OL}	Low level output voltage	V_{ID} = −1V	I_{OUT} = 4mA[2]		0.4		0.4	V
			I_{OUT} = 8mA[2]		0.45		0.45	
I_{OS}	Short-circuit output current	V_{ID} = 1V, Note 3		20	100	20	100	mA
I_{CC}	Supply current	4.75V ≤ V_{CC} ≤ 5.25V, V_{ID} = −1V; FS = 0V			100		100	mA
I_{IN}	Input current	Other inputs grounded	V_{IN} = +10V		3.25		3.25	mA
			V_{IN} = −10V	−3.25		−3.25		

NOTES:
1. R_S is a resistor in series with each input.
2. Measured after 100ms warm-up (at 0°C).
3. Only 1 output may be shorted at a time and then only for a maximum of 1 second.
4. See Figure 1 for threshold and hysteresis definitions.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V ±5%, 0°C ≤ T_A ≤ +70°C

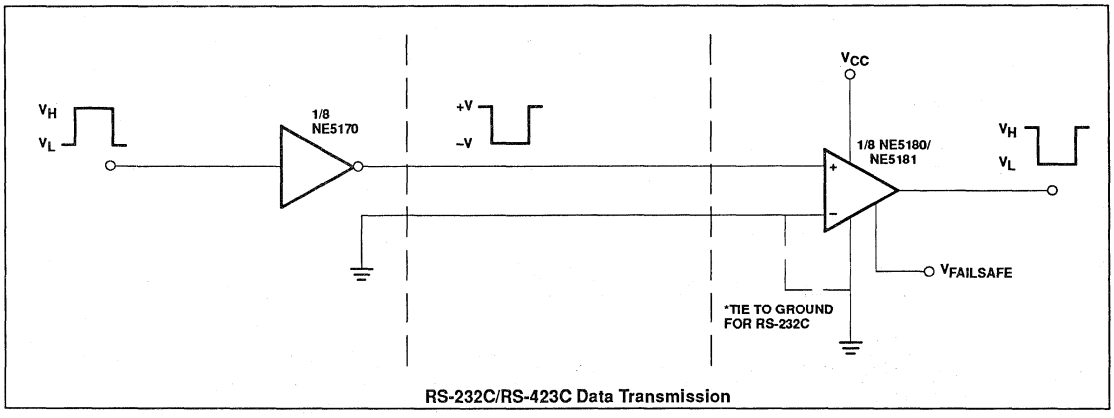
SYMBOL	PARAMETER	TEST CONDITIONS	NE5180 Min	NE5180 Max	NE5181 Min	NE5181 Max	UNIT
t_{PLH}	Propagation delay—low to high	C_L = 50pF, V_{ID} = ±1V		500		100	ns
t_{PHL}	Propagation delay—high to low	C_L = 50pF, V_{ID} = ±1V		500		100	ns
f_a	Acceptable input frequency	Unused input grounded, V_{ID} = ±200mV[1]		0.1		5.0	MHz
f_r	Rejectable input frequency	Unused input grounded, V_{ID} = ±500mV	5.5		NA		MHz

NOTE:
1. V_{ID} = ±1V for NE5181.

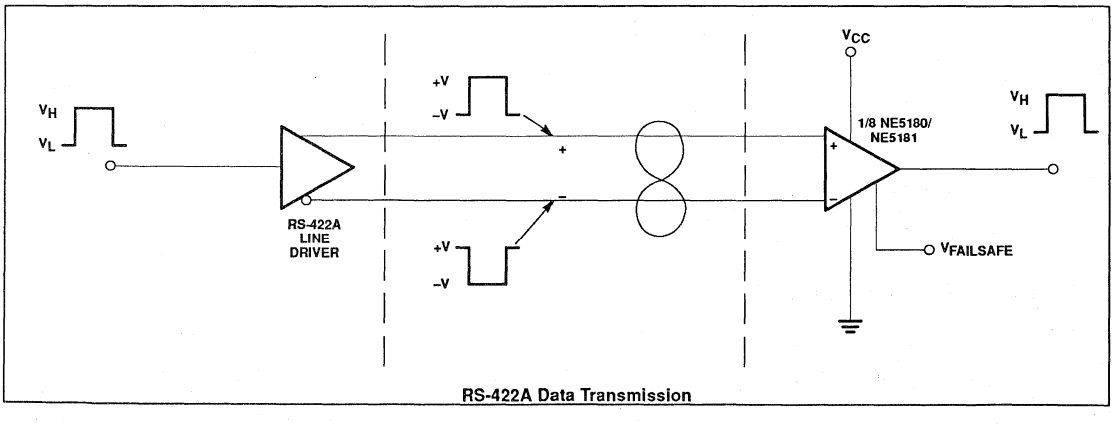
FAILSAFE OPERATION

These devices provide a failsafe operating mode to guard against input fault conditions as defined in RS-422A and RS-423A standards. These fault conditions are (1) driver in power-off condition, (2) receiver not interconnected with driver, (3) open-circuited interconnecting cable, and (4) short-circuited interconnecting cable. If one of these four fault conditions occurs at the inputs of a receiver, then the output of that receiver is driven to a known logic level. The receiver is programmed by connecting the failsafe input to V_{CC} or ground. A connection to

APPLICATIONS

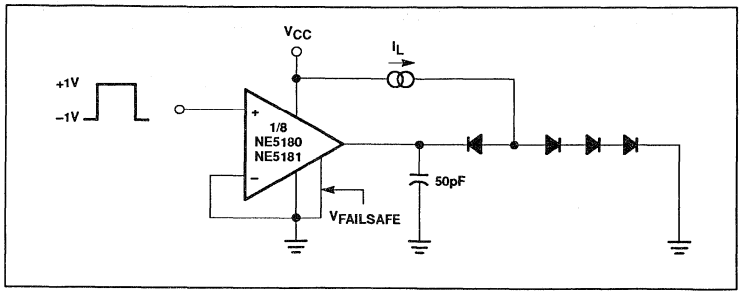


RS-232C/RS-423C Data Transmission

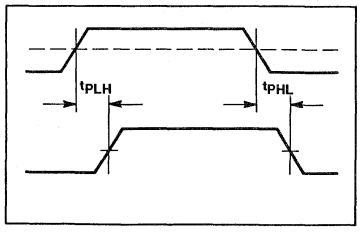


RS-422A Data Transmission

AC TEST CIRCUIT



VOLTAGE WAVEFORMS



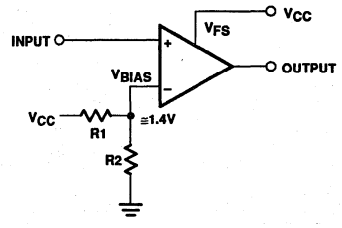
V_{CC} provides a logic "1" output under fault conditions, while a connection to ground provides a logic "0". There are two failsafe pins (F_{S1} and F_{S2}) on the NE5180 or NE5181 where each provides common failsafe control for four receivers.

RS-232 FAILSAFING

The internal failsafe circuitry works by providing a small input offset voltage which can be polarity-switched by using the failsafe control pins. This offset is kept small (approximately 80mV) to avoid degradation of the ±200mV input threshold for RS-423 or RS-422 operation. If the positive and negative inputs to any receiver are both shorted to ground or open circuited, the internal offset drives that output to the programmed failsafe state. If only one input open circuits (as may be the case for RS-232 operation), that input will rise to the "input open circuit voltage" (approximately 700mV). Since this is much greater than the 200mV threshold, the output will be driven to a state that is independent of the failsafe programming. Failsafe programming can be achieved for non-inverting single-ended applications by raising or lowering the unused input bias voltage as shown in Figure 2. For $V_{BIAS} \cong 1.4$, an open (or grounded) INPUT line will be approximately 700mV (0V) and the output will failsafe low. If the resistor divider is not used and V_{BIAS} is connected to ground, the output will failsafe high due to the internal failsafe offset for the INPUT grounded and the 700mV "open circuit input voltage" for the INPUT open circuited. Similar operation holds for an inverting configuration, with V_{BIAS} applied to the positive input and V_{FS} = ground.

INPUT FILTERING (NE5180)

The NE5180 has input filtering for additional noise rejection. This filtering is a function of both signal level and frequency. For the specified input (5.5MHz at ±500mV) the input stage filter attenuates the signal such that the output stage threshold levels are not exceeded and no change of state occurs at the output. As the signal amplitude decreases (increases) the rejected frequency decreases (increases).



NOTE:
Two silicon diodes may be used in place of R2.

Figure 2. Single-Input Failsafe Programming

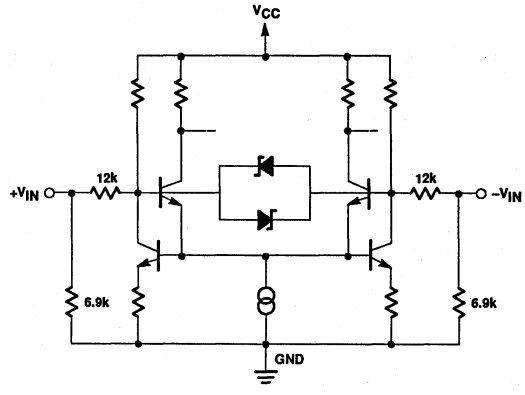


Figure 3. Differential Input Stage

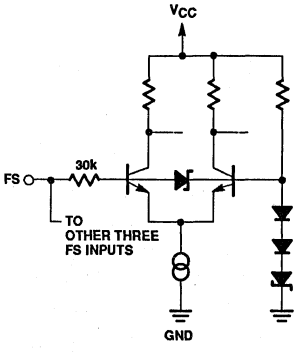


Figure 4. Failsafe Input Stage

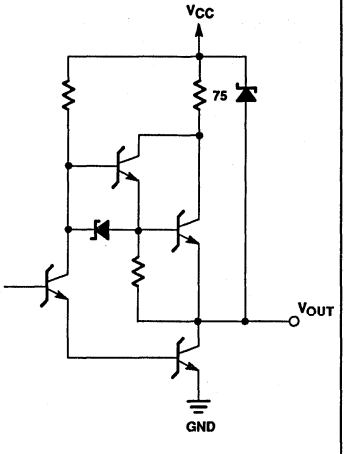


Figure 5. Output Stage

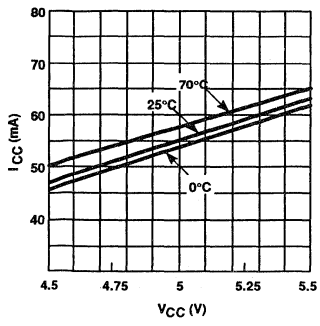


Figure 6. Typical Supply Current vs Supply Voltage

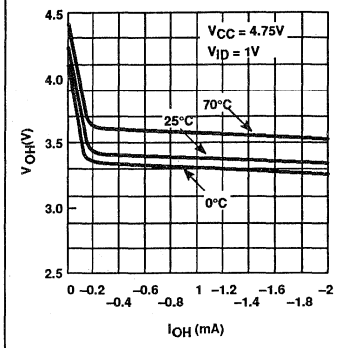


Figure 7. Typical High Level Output Voltage vs Output Current

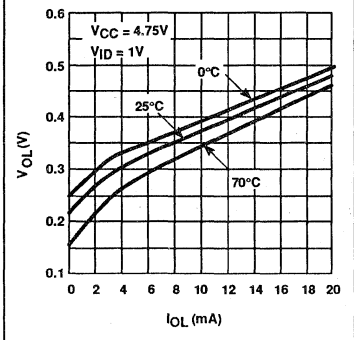
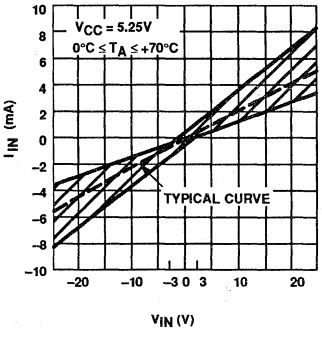


Figure 8. Typical Low Level Output Voltage vs Output Current



*This graph applies for all receiver inputs, provided that the opposite polarity input of the amplifier being measured is grounded.

Figure 9. Input Current vs Input Applied Voltage*

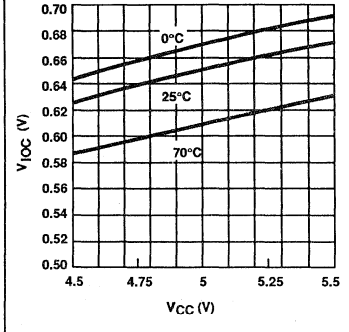


Figure 10. Typical V_{IOC} vs V_{CC}

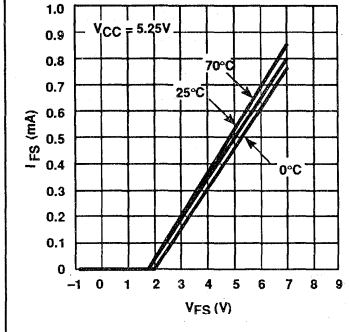


Figure 11. Typical FS Input Current vs FS Applied Voltage

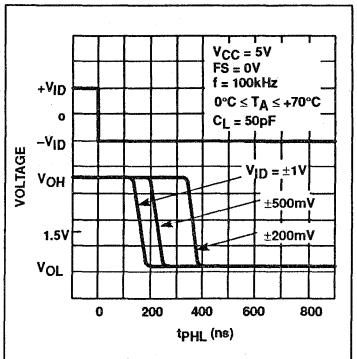


Figure 12. NE5180: Propagation Delay at Various Input Amplitudes

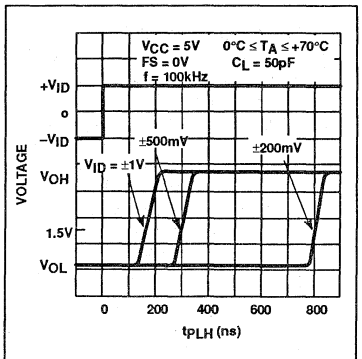


Figure 13. NE5180: Propagation Delay at Various Input Amplitude

Quad high-speed differential line driver — AM26LS31

DESCRIPTION

The AM26LS31 is a quad differential line driver, designed for digital data transmission over balanced lines. The AM26LS31 meets all the requirements of EIA standard RS-422 and Federal standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines. The circuit provides an enable and disable function common to all four drivers. The AM26LS31 features 3-State outputs and logical ORed complementary enable inputs. The inputs are all LS compatible and are all one unit load.

The AM26LS31 is constructed using advanced Low Power Schottky processing.

FEATURES

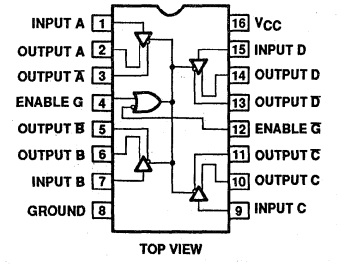
- Output skew of 2.0ns typical
- Input to output delay: 12ns
- Operation from single +5V
- 16-pin DIP and SO packages
- Four line drivers in one package
- Output short-circuit protection
- Complementary outputs
- Meets EIA standard RS-422
- High output drive capability for 100Ω terminated transmission lines
- Available in military and commercial temperature range
- Advanced low power Schottky processing
- Outputs won't load line when V_{CC} = 0V

APPLICATIONS

- Data communications equipment
- Computer peripherals
- Workstations
- Automatic test equipment

PIN CONFIGURATION

D, F, and N Packages



TOP VIEW

FUNCTION TABLE (Each Driver)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	A	$\overline{A}$
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

NOTES:
H = High level
L = Low level
X = Irrelevant
Z = High-impedance (OFF)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0°C to +70°C	AM26LS31CN
16-Pin SO	0°C to +70°C	AM26LS31CD
16-Pin Plastic DIP	–40°C to +85°C	AM26LS31IN
16-Pin SO	–40°C to +85°C	AM26LS31ID
16-Pin Plastic DIP	–55°C to +125°C	AM26LS31MN

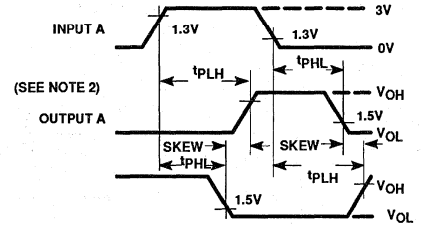
DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%, T_A = –55 to +125°C for AM26LS31MF and AM26LS31MN; V_{CC} = 5V ±5%, T_A = –40 to +85°C for AM26LS31IN and AM26LS31ID; V_{CC} = 5V ±5%, T_A = 0 to +70°C for AM26LS31CN and AM26LS31CD, unless otherwise specified.

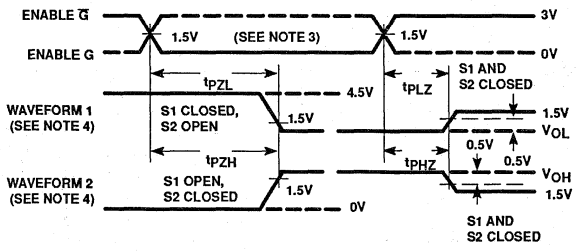
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[1]	Max	
V_{OH}	Output High voltage	V_{CC} = Min., I_{OH} = –20mA	2.5	3.0		V
V_{OL}	Output Low voltage	V_{CC} = Min., I_{OL} = 20mA		0.3	0.5	V
V_{IH}	Input High voltage	V_{CC} = Min.	2.0			V
V_{IL}	Input Low voltage	V_{CC} = Max.			0.8	V
I_{IL}	Input Low current	V_{CC} = Max., V_{IN} = 0.4V		–0.26	–0.36	mA
I_{IH}	Input High current	V_{CC} = Max., V_{IN} = 2.7V		0.001	20	µA
I_I	Input reverse current	V_{CC} = Max., V_{IN} = 7.0V		0.001	0.1	mA
I_O	OFF-state (high-impedance) output current	V_{CC} = Max., V_O = 5.5V V_O = 0.5V		0.6 –0.050	20 –20	µA µA
V_I	Input clamp voltage	V_{CC} = Min., I_{IN} = –18mA		–0.8	–1.5	V
I_{SC}	Output short-circuit current	V_{CC} = Max.	–30		–150	mA
I_{CC}	Power supply current	V_{CC} = Max; all outputs disabled		40	80	mA
t_{PLH}	Input to output	T_A = 25°C, load[2]		9	20	ns
t_{PHL}	Input to output	T_A = 25°C, load[2]		9	20	ns
SKEW	Output to output	T_A = 25°C, load[2]		2	6	ns
t_{LZ}	Enable to output	T_A = 25°C, C_L = 10pF		17	35	ns
t_{HZ}	Enable to output	T_A = 25°C, C_L = 10pF		12	30	ns
t_{ZL}	Enable to output	T_A = 25°C, load[2]		14	45	ns
t_{ZH}	Enable to output	T_A = 25°C, load[2]		12	40	ns

NOTES:
1. All typical values are T_A = +25°C; V_{CC} = 5.0V.
2. C_L = 30pF; V_{IN} = 1.3V to V_{OUT} = 1.3V; V_{PULSE} = 0V to 3.0V.

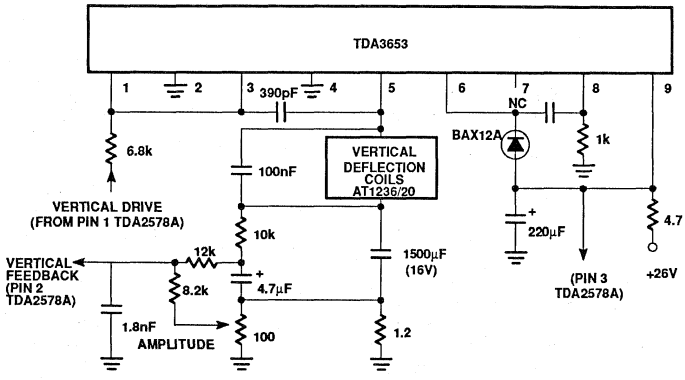
TIMING DIAGRAMS



Propagation Delay Times and Skew



Enable and Disable Times



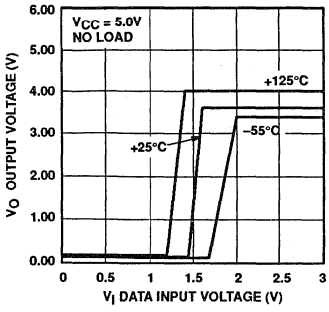
Test Circuit

NOTES:

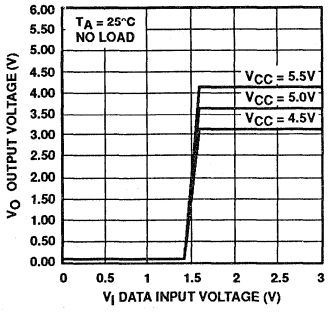
1. All pauses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_{OUT} = 50W, 1R ≤ 15ns, 1F ≤ 6ns
2. When measuring propagation delay times and skew, switches S1 and S2 are open.
3. Each enable is tested separately.
4. Waveform 1 is for an output with internal condition such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal condition such that the output is high except when disabled by the output control.
5. C_L includes probe and jig coapacitance.

TYPICAL PERFORMANCE CHARACTERISTICS

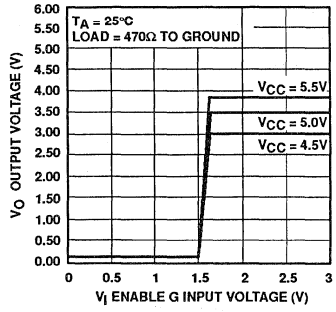
Output Voltage vs Data Input Voltage



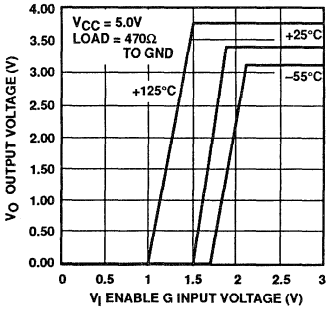
Output Voltage vs Data Input Voltage



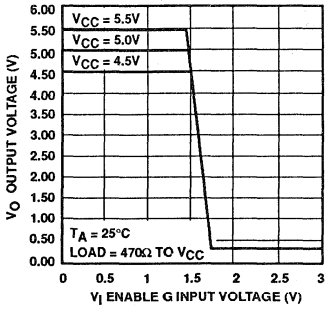
Output Voltage vs Enable G Input Voltage



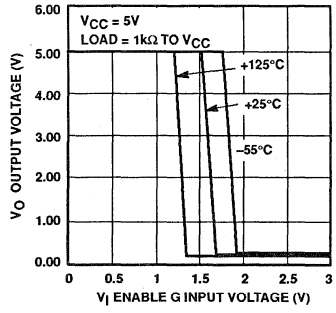
Output Voltage vs Enable G Input Voltage



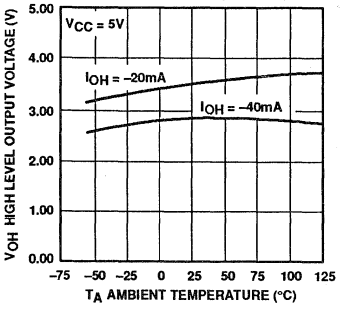
Output Voltage vs Enable G Input Voltage



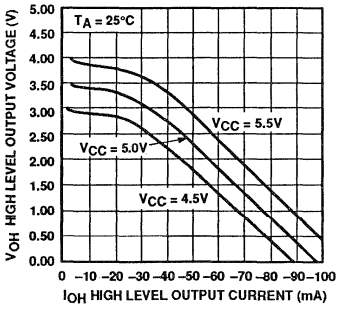
Output Voltage vs Enable G Input Voltage



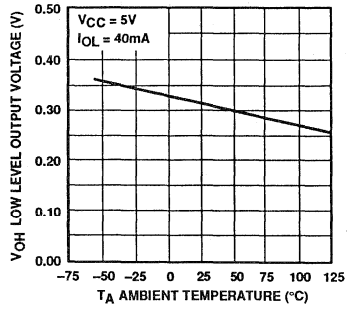
High Level Output Voltage vs Ambient Temperature



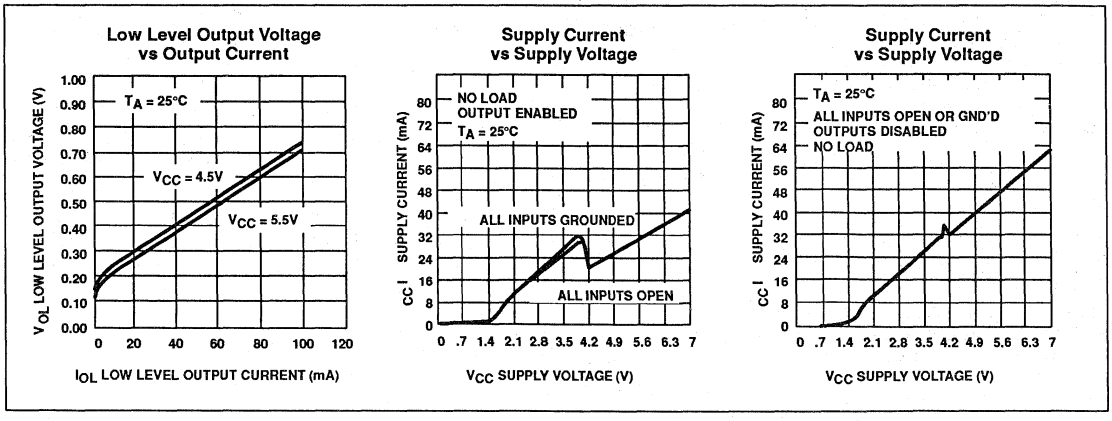
High Level Output Voltage vs Output Current



Low Level Output Voltage vs Ambient Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



Quad high-speed differential line receivers

AM26LS32/ AM26LS33

DESCRIPTION

The AM26LS32 and AM26LS33 are quad line receivers designed to meet all of the requirements of RS-422 and RS-423 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The AM26LS32 features an input sensitivity of ±200mV over the common mode input range of ±7V.

The AM26LS33 features an input sensitivity of ±500mV over the common mode input voltage range of ±15V.

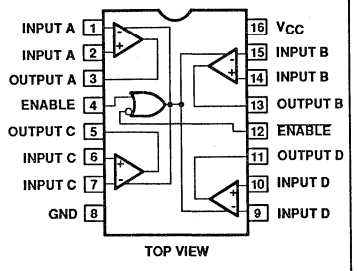
The AM26LS32 and AM26LS33 provide an enable and disable function common to all four receivers. Both parts feature 3-State outputs with 8mA sink capability and incorporate a fail-safe input-output relationship which forces the outputs high when the inputs are open.

FEATURES

- Input voltage range of 15V (differential or common mode) on AM26LS33; 7V (differential or common mode) on AM26LS32
- ±0.2V sensitivity over the input voltage range on AM26LS32
- ±0.5V sensitivity on AM26LS33
- 6kΩ minimum input impedance
- The AM26LS32 meets all the requirements of RS-422 and RS-423
- Operation from single +5V supply
- Fail safe input-output relationship. Output always high when inputs are open
- 3-State drive, with choice of complementary output enables, for receiving directly onto a data bus
- 3-State outputs disabled during power up and power down

PIN CONFIGURATION

F, D and N Packages



TOP VIEW

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0°C to +70°C	AM26LS32CN
16-Pin SO	0°C to +70°C	AM26LS32CD
16-Pin Plastic DIP	–40°C to +85°C	AM26LS32IN
16-Pin SO	–40°C to +85°C	AM26LS32ID
16-Pin Plastic DIP	–55°C to +125°C	AM26LS32MN
16-Pin Plastic DIP	0°C to +70°C	AM26LS33CN
16-Pin SO	0°C to +70°C	AM26LS33CD
16-Pin Plastic DIP	–40°C to +85°C	AM26LS33IN
16-Pin SO	–40°C to +85°C	AM26LS33ID
16-Pin Plastic DIP	–55°C to +125°C	AM26LS33MN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply	7	V
V_{IN}	Power supply	7	V
	Output sink current	50	mA
	Common mode range	±25	V
V_{TH}	Differential input voltage	±25	V
T_{STG}	Storage temperature range	–65 to +150	°C

DISSIPATION OPERATING TABLE

PACKAGE	POWER DISSIPATION	DERATING FACTOR	ABOVE T_A
F	1,524mW	12.19mW/°C	25°C
N	1,275mW	10.2mW/°C	25°C
D	1,262W	10.1mW/°C	25°C

DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10% for AM26LS32/33MX, V_{CC} = 5.0V ±5% for AM26LS32/33CX and AM26LS32/33IX over operating temperature range unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			LIMITS AM26LS32/33 Min	LIMITS AM26LS32/33 Typ[1]	LIMITS AM26LS32/33 Max	UNIT
V_{TH}	Differential input voltage	$V_{OUT} = V_{OL}$ or V_{OH} AM26LS32, $-7V \le V_{CM} \le +7V$			–0.2	0.06	0.2	V
		AM26LS33, $-15V \le V_{CM} \le +15V$			–0.5	0.06	0.5	V
R_{IN}	Input resistance	$-15V \le V_{CM} \le +15V$ (One input AC ground)			6.0	9.8		kΩ
I_{IN}	Input current (under test)	$V_{IN} = +15V$ Other input $-10V \le V_{IN} \le +15V$					2.3	mA
I_{IN}	Input current (under test)	$V_{IN} = -15V$ Other input $+10V \le V_{IN} \le -15V$					–2.8	mA
V_{OH}	Output HIGH voltage	V_{CC} = Min., I_{OH} = –440µA ΔV_{IN} = +1.0V $V_{\overline{ENABLE}}$ = 0.8V		Com'l	2.7	3.4		V
				Mil	2.5	3.4		V
V_{OL}	Output LOW voltage	$V_{\overline{CC}}$ = Min., $V_{\overline{ENABLE}}$ = 0.8V ΔV_{IN} = +1.0V	I_{OL} = 4.0mA			0.3	0.4	V
			I_{OL} = 8.0mA				0.45	V
V_{IL}	Enable LOW voltage						0.8	V
V_{IH}	Enable HIGH voltage				2.0			V
V_I	Enable clamp voltage	V_{CC} = Min., I_{IN} = –18mA					–1.5	V
I_O	Off state (high impedance) output current	V_{CC} = Max.	V_O = 2.4V				20	µA
			V_O = 0.4V				–20	µA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 5.0V ±10% for AM26LS32/33MX, V_{CC} = 5.0V ±5% for AM26LS32/33CX and AM26LS32/33IX over operating temperature range unless otherwise specified.

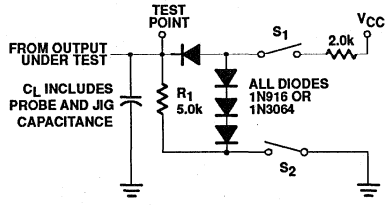
SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS AM26LS32/33 Min	Typ[1]	Max	UNIT
I_{IL}	Enable LOW current	V_{IN} = 0.4V			–0.2	–0.36	mA
I_{IH}	Enable HIGH current	V_{IN} = 2.7V			0.5	20	µA
I_I	Enable input HIGH current	V_{IN} = 5.5V			1	100	µA
I_{SC}	Output short circuit current	V_{CC} = Max., ΔV_{IN} = +1V, V_{OUT} = 0V		–15	–60	–85	mA
I_{CC}	Power supply current	V_{CC} = Max.; All V_{IN} = GND outputs disabled			52	70	mA
V_{HYST}	Input hysteresis	T_A = 25°C, V_{CC} = 5.0V, V_{CM} = 0V	AM26LS32		120		mV
			AM26LS33		120		mV
t_{PLH}	Input to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF (see test condition)			10	25	ns
t_{PHL}	Input to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF (see test condition)			10	25	ns
t_{LZ}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 5pF (see test condition)			15	30	ns
t_{HZ}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 5pF (see test condition)			12	22	ns
t_{ZL}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF (see test condition)			8	22	ns
t_{ZH}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF			9	22	ns

NOTE:
1. All typical values are T_A = 25°C, V_{CC} = 5.0V.

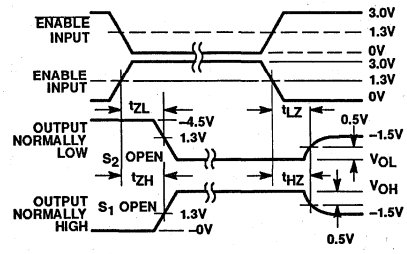
FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUT	ENABLES E	$\overline{E}$	OUTPUT
$V_{ID} \geq V_{TH}$	H	X	H
	X	L	H
$V_{TL} \leq V_{ID} \leq V_{TH}$	H	X	?
	X	L	?
$V_{ID} \leq V_{TL}$	X	L	L
	H	X	X
X	L	H	Z

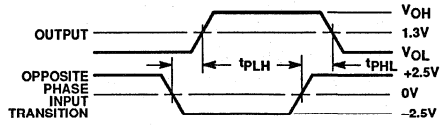
NOTES:
H = High level, L = Low level, X = Irrelevant
Z = High impedance (off), ? = Indeterminate
E = Enable, $\overline{E}$ = $\overline{\text{Enable}}$



Load Test Circuit for 3-State Outputs



Enable and Disable Tmes[2, 3, 4]



Propagation Delay[1, 4]

NOTES:

1. Diagram shown for $\overline{\text{Enable}}$ Low.
2. Enable is tested with $\overline{\text{Enable}}$ High; $\overline{\text{Enable}}$ is tested with Enable Low.
3. S_1 and S_2 of Load Circuit are closed except where shown.
4. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_O = 50Ω; t_r ≤ 15ns; t_f ≤ 6.0ns.

Power line modem — NE5050

DESCRIPTION

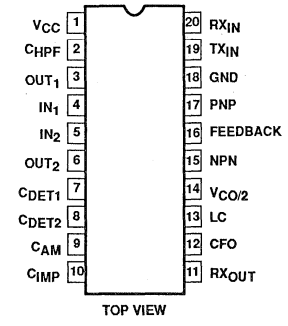
The NE5050 is a modem for power line, coaxial cable, and twisted-pair communications. The modem incorporates features to overcome line impulse noise and line impedance modulation. The modem's transmitter incorporates a Colpitts oscillator, positive logic, carrier-on/-off switch, and a line driver. The receiver has an amplifier, a limiter, an amplitude detector, an amplitude modulation cancelling stage, an impulse filter, and an SR flip-flop. One NE5050 can be used to transmit and receive with Amplitude Shift Key (ASK) carrier-on/-off modulation. With two NE5050s, Frequency Shift Key (FSK) modulation can be implemented. The transmitter input and the receiver output accept TTL or CMOS serial data.

FEATURES

- High receiver sensitivity — typ. 1.5mV$_{RMS}$
- Receiver input overload protected for signals up to 70V$_{P-P}$
- High data rates — 300kbit/s ASK NRZ over twisted-pair
- The modem reaches the Nyquist limit of 1 bit per carrier cycle
- Has listen-while-talking for carrier sense multiple access/collision detect (CSMA/CD) networking capability
- Increased noise immunity with balance interstage ports for bandpass filtering
- Flexible oscillator can be made with LC tank (Colpitts), with crystal (Pierce), or accept external clock
- Signals are processed in real-time making this modem suitable for repeater/carrier translation applications

PIN CONFIGURATION

D[1] and N Packages



TOP VIEW

NOTE:
1. SOL — Released in large SO package only.

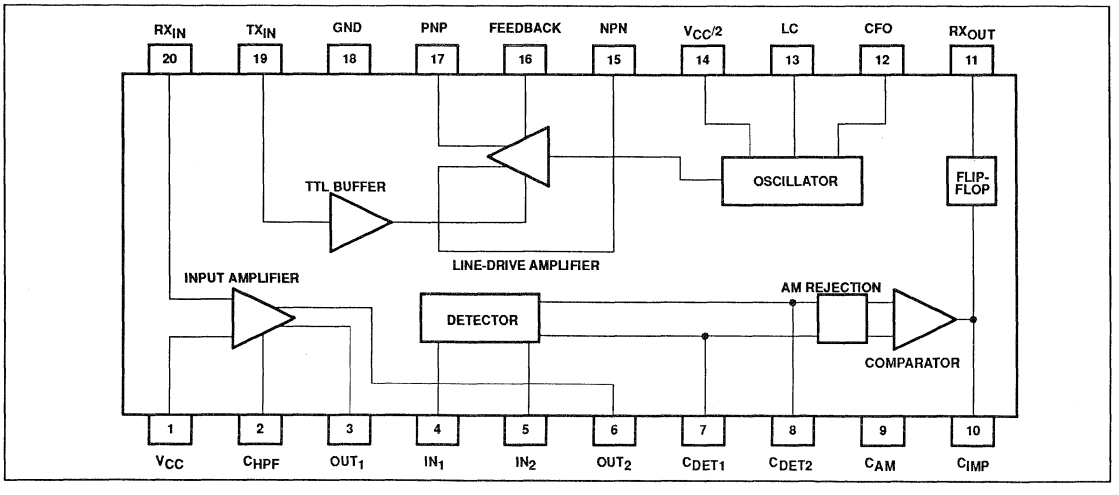
APPLICATIONS

- Twisted-pair communications
- Coaxial cable communications
- 120/277V$_{RMS}$, 50 or 60Hz, power line communications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	NE5050N
20-Pin Plastic SOL	0 to +70°C	NE5050D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	18	V
V_{LOGIC}	Logic supply voltage	18	V
T_A	Ambient temperature range	0 to +70	°C
T_J	Junction temperature range	–55 to +150	°C
T_{STG}	Storage temperature range	–65 to +150	°C
P_{DMAX}	Maximum power dissipation[1]	700	mW

NOTE:
1. The power dissipation is based on V_{CC} = 12V, T_J = +150°C, TX_{OFF}: I_{CC} = 20mA, TX_{ON}: I_{CC} = 50mA, θ_{JA} = 61°C/W 20-pin plastic package.

DC ELECTRICAL CHARACTERISTICS

T_A = +25°C, V_{CC} = 12V, F carrier = 120kHz, data = NRZ, 50% duty cycle unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		10	12	16	V
I_{CC}	Supply current	TX_{OFF}	5	8	11	mA
I_{CC}	Supply current	TX_{ON}[1]	18	24	30	mA
V_{LOGIC}	Logic voltage			5	16	V
P_D	Power dissipation	RX_{OFF}, TX_{OFF} RX_{ON}, TX_{ON}, 100Ω load		100 300	220 660	mW mW
V_{IHMIN}	TX TTL input	TX_{ON}, Pin 19	2.4			V
V_{ILMAX}	TX TTL input	TX_{OFF}, Pin 19			0.8	V
V_{OLMAX}	RX open-collector output	I_{OL} = 5mA, Pin 11			0.4	V
I_{OLMAX}	RX open-collector output	Pin 11			5	mA
	TX data rate[2]	f_{CXR} = 120kHz, 500kHz	DC	1k	300k	bit/s
	RX data rate[2]	f_{CXR} = 120kHz, 500kHz	0.1	1k	300k	bit/s
	Carrier cycles per bit, TX and RX[2]		1			cycle
Broadband I/O ports, carrier						
	RX input sensitivity	1:1 input transformer	3.5	1.5		mV_{RMS}
	RX input signal level	V_{CC} ±35V = –25V, +51V			70	V_{P-P}
	RX input impedance	Pin 20		9		kΩ
	RX line impedance modulation rejection	120HzAM 2V/20mV, 1kbit/s	40			dB
	RX carrier frequency[2]		0.1	120	500	kHz
	RX detector differential input impedance	Pin 4, Pin 5, each		27		kΩ
PSRR	RX power supply rejection ratio	60Hz and 120Hz		80		dB
	Broadband port impedance	RX_{OFF} and TX_{OFF}		7.3		kΩ
	TX output signal level	TX_{ON}, 100Ω load		8		V_{P-P}
	TX driver output impedance	TX_{OFF}		40		kΩ
	TX driver output impedance	TX_{ON}		1.2		Ω
	TX amplitude temperature drift	External oscillator		+140		ppm/°C
	TX amplitude temperature drift	LC oscillator		+0.23		%/°C
	TX output current capability	TX_{ON}, Pins 15, 17		40		mA peak
	TX output THD (total harmonic distortion)	TX_{ON}, LC oscillator		1	2	%
	TX line drive amplifier BW	At 6dB gain		500		kHz
	TX carrier frequency[2]		DC	120	500	kHz
	TX oscillator temperature drift	Temperature range		+60		ppm/°C
	TX oscillator initial frequency accuracy	Sam LC tank		±1		%
	TX carrier feedthrough (leakage)	TX_{OFF}		–90		dBmO

ABBREVIATIONS:
TX = transmitter
RX = receiver

NOTES:
1. TX looped back to RX, data = 1kbit/s TTL, NRZ, 50% duty cycle ASK.
2. The NE5050 modem reaches the theoretical maximum data density for a given (fixed) carrier frequency. This limit is set by the maximum data bandwidth required before intersymbol interference occurs. The minimum specified limits are not tested in production. They are guaranteed by design.

PIN FUNCTION DESCRIPTION

Pin 1: $+V_{CC}$
For de-coupling V_{CC} to ground a 0.1µF capacitor must be placed close to Pin 1 and Pin 18.

Pin 2: C_{HPF}
High-pass filter, rejects 60Hz and its harmonics, rejects low frequencies, directing them to ground. Capacitor to ground: C_{HPF} = 10nF for f_{CXR} = 120kHz and C_{HPF} = 4.7nF for f_{CXR} = 300kHz. The input amplifier provides a high-pass function: a +20dB/decade frequency response, with a DC attenuation of –50dB. A frequency of 100kHz is amplified by +24dB. The –3dB point of this high-pass filter is given by the equation:

$10^9/C_{HPF}$ (F) = f_{-3dB} (Hz)

Pin 3: OUT_1
RX amplifier differential (+) output. Low impedance output. See Pin 6. Pin 3 can be connected to Pin 4 directly. A differential, bandpass filter can be connected from Pins 3, 6 to Pins 4, 5. If LC values are used, they are the same as the oscillator LC values (see Pins 13 and 14). The BW_{-3dB} is controlled by the series resistors R_1 and R_2. An external active filter providing gain can improve the RX sensitivity and filter out CW interference.

Pin 4, Pin 5: IN_1, IN_2
AM detector (±) inputs. High-impedance inputs = 27kΩ each. The require DC bias voltage from Pins 3 and 6 or around 4.5V. Pin 3 can be connected to Pin 4 directly. Pin 6 can be connected to Pin 5 directly. A differential bandpass filter can be connected from Pins 3, 6 to Pins 4, 5. If LC values are used, they are the same as the oscillator LC values (see Pins 13 and 14). The BW_{-3dB} is controlled by series resistors. An external active filter providing gain can improve the RX sensitivity and filter out CW interference.

Pin 6: OUT_2
RX amplifier differential (–) output. Low impedance output. See Pin 3. Pin 6 can be connected to Pin 5 directly.

Pin 7, Pin 8: C_{DET}
Amplitude detector (±) output capacitor between Pins 7 and 8. t_{DET} is the time it takes for C_{DET} to charge from 0mV to 50mV, where 50mV is the detection threshold. The detector delay time, t_{DET}, affects the receiver's jitter. t_{DET} is a term in a sum of delays, the sum being the total receiver delay, t_D. See below in 'Receiver Delays' the relation between t_D and the maximum bit rate. The C_{DET} capacitor value is given by:

C_{DET} (F) = t_{DET} (sec)/10^5

Pin 9: C_{AM}
Line impedance modulation rejection capacitor. A 0.1µF capacitor to ground provides about 4s of delay for the transition from receive data to standby. The C_{AM} value is determined in function of the bit string or in the preamble. It is a measure of the "readiness" of the receiver to switch from the "standby" mode to the "receive data mode" with no loss of leading bits. A low C_{AM} value will make the modem react faster (shorter delays) in both transition directions: from "standby" to "receive data" (incoming or departing messages) and from "receive data" to "standby" (absence of data traffic). Its value should be

C_{AM} (F) = 10–4/bit rate [bits/s]

Pin 10: C_{IMP}
Impulse noise rejection cpacitor. At 1kbit/s a 10nF capacitor to ground provides 350µs of delay and impulse rejection. This capacitor determines the receiver impulse noise immunity (transmission channel with non-Gaussian noise). t_{IMP} is the time it takes to ramp up or down the C_{IMP} voltage (the beginning of the ramp is delayed by t_{DET}). The shortest bit should last longer than the widest impulse. t_{IMP} is a term in a sum of delays, the sum being the total receiver delay, t_D. See 'Receiver Delays' for the relation between t_D and the maximum bit rate. The C_{IMP} capacitor value is determined by the equation:

C_{IMP} (F) = t_{IMP} (s)/85kΩ

The following equation determines t_{IMP}:

Maximum rejected or expected impulse noise width (s) < t_{IMP} (s)

Pin 11: RX Data Output
Open-collector RX output. RX data output.

I_{OLMAX} = 5mA = $V_{LOGIC}/R_{PULL-UP}$

Pin 12: C_{F0}
Oscillator feedback input. C_{F0} = 27 to 51pF capacitor between Pins 12 and 13. C_{F1} = capacitor between Pins 12 and GND. If the on-chip oscillator is used, C_{F1} may be omitted. If external oscillations are injected at Pin 13, C_{F0} must be removed and C_{F1} must be connected to GND. Grounding Pin 12 disables the oscillator.

Pin 13: Oscillator I/O
Colpitts LC oscillator tank, Pierce crystal oscillator, or external oscillator input.

On-chip LC oscillator — oscillator output. External oscillator tank present. Parallel LC components attached between Pins 13 and 14. C_{F0} attached between Pin 12 and Pin 13. A resistor between Pins 13 and 14 can decrease the oscillation amplitude to the desired level. Amplitudes above 2V peak may have THD > 2%. C_{F1} is not used. The amplitude varies with temperature; thermistor compensation recommended at Pin 16.

On-chip crystal oscillator — oscillator output. Two external capacitors in series, C_{13} and C_{14}. C_{13} is connected to Pin 13 and C_{14} is connected to Pin 14. The external crystal is attached between Pin 13 and the connection of C_{13} and C_{14}. An optinal inductor L, attached between Pins 13 and 14, tuned at the oscillation frequency by C_{13} and C_{14} prevents oscillations at the crystal overtones. C_{F0} and C_{F1} are not used.

External oscillator — oscillator input. Parallel LC components attached between Pins 13 and 14 provide bias to Pin 13 and perform bandpass filtering. If a square wave is generated from a microprocessor by clock division, a series LC from the divider output to Pin 13 will perform additional bandpass filtering. C_{F1} = 0.1µF is connected to ground. C_{F0} is not used. If a sinusoidal wave is available, a 50Ω resistor may replace the parallel LC bandpass filter and a 0.1µF capacitor may replace the series LC bandpass filter. The amplitude is constant over temperature.

Pin 14: $+V_{CC}/2$
Oscillator bias at $+V_{CC}/2$. A 0.1µF de-coupling capacitor to GND is optional.

Parallel LC components attached between Pins 13 and 14.

Pin 15: TX Carrier Output (NPN Transistor Base)

Transmitter broadband output. Can drive 40mA peak (80mA peak non-repetitive).

NPN external Darlington translator drive — Drives 1Ω loads.

NPN external translator drive — 1Ω – 0.5W – R_{E1} to Pin 16 for 10Ω loads.

On-chip driver — 10Ω R_{E1} between Pins 15 and 16 for 50Ω loads.

Pin 16: TX Line Drive Feedback

$R_{FEEDBACK}$ adjusts the driver amplifier gain. Minimum gain ($R_{FEEDBACK}$ = 0) is 2 (6dB). A thermistor can compensate the LC oscillator amplitude variation. R_{E1} resistor (and NPN EB junction) to Pin 15. R_{E2} resistor (and PNP EB junction) to Pin 17. The C_{DRIVE} coupling capacitor is in series with the R_{DRIVE} resistor from Pin 16 to Pin 20. The R_{DRIVE} value is the assumed line impedance. The C_{DRIVE} impedance is $1/(2 \times f_{CXR} C_{DRIVE})$.

Pin 17: TX Carrier Output (PNP Transistor Base)

Transmitter broadband output. Can drive 40mA peak (80mA peak non-repetitive).

PNP external Darlington translator — Drives 1Ω loads.

PNP external translator drive — 1Ω – 5.0W – R_{E2} to Pin 16 for 10Ω loads.

On-chip driver — 10Ω R_{E2} between Pins 16 and 17 for 50Ω loads.

Pin 18: Ground

Pin 19: TX Data Input

Transmitter TTL data input. Logic 1 will turn the transmit driver on, and sinusoidal carrier will be sent to the line from a low impedance source. Logic 0 will turn the driver off, to high output impedance.

Pin 20: RX Carrier Input

Receiver carrier input. Withstands an over-voltage of $+V_{CC}$ ±35V. DC bias connected through the line coupling transformer secondary to $+V_{CC}$ (Pin 1). The C_{DRIVE} coupling capacitor is in series with the R_{DRIVE} resistor from Pin 16 to Pin 20.

DESCRIPTION OF OPERATION

The NE505 modem has been designed for transmitting and receiving control and data signals over the AC power lines, coaxial cables and twisted-pair cables. The modem overcomes line impulse noise and line impedance modulation. Two carrier modulation methods can be used: carrier on/off ASK, NRZ data and non-coherent FSK. The power line is not an ideal medium for communication. The line noise, interference and losses are caused by: impulse noise, CW interference, line impedance modulation, and distribution transformer attenuation. NE5050 was designed to support both ASK and non-coherent FSK communications in this environment.

Listen-While-Talk

The IC modem is always in the receive mode, even when transmitting (it receives its own carrier). This capability permits remote RX and TX functionality testing for each system node. In the receive mode, the modem receives carrier signals from other transmitters. In the transmit mode, the modem transmits carrier to other receivers and receives its own carrier.

On-Chip Collision Detection

The liten-while-talk capability enables this IC to perform CSMA/CD (carrier-sense, multiple-access/collision detect) networks. Collision is dtected when the local TX intends to transmit and the line is not clear.

In Dense Data Traffic

The RX data output (RX_{OUT}) does not have time to go into the stanby (lower power consumption, inverted logic) mode. In this case the RX_{OUT} is in positive logic (carrier-on = 1, carrier-off = 0). A collision is detected at the local node when the local TX is off and the local RX_{OUT} = 1. Collision: remote carrier present and detected. Abort local transmission. If, however, standby occurs (bursts of high-speed data) a proper value of C_{AN} will inusre capture of all leading bits except for the first "10" transition.

In Rare Data Traffic

The RX_{OUT} is in standby most of the time. In this case the RX_{OUT} logic mode is inverted due to a designed-in offset present in the AM rejection and impulse filter circuits. A logic sequence from the local TX insures proper RX offset adjustment (preamble, the first "10" bits). The collision detection proceeds as in the dense data traffic case. The transition time from the last received bit "1" to the standby mode is proportional to the value of the AM rejection capacitor at Pin 9. For C_{AM} = 10nF, the "receive data" to "standby" transition occurs after 4 seconds from the last "1". Therefore, long strings of "0"s can be transmitted and received. The standby function may be disabled with proper bias at Pin 9 (external components).

TX-to-RX and RX-to-TX Switching Times

With the listen-while-talk capability the TX-to-RX and the RX-to-TX switching times have the meaning of TX_{ON}-to-TX_{OFF} and TX_{OFF}-to-TX_{ON} switching times, respectively. The TX-to-RX and RX-to-TX minimum switching times can be calculated from the maximum data rate. Since one bit can last a minimum of 3µs (NRZ ASK data), this may be considered the minimum switching time.

Data Rate

The maximum data rate is 300kbit/s NRZ ASK. This data rate was achieved on a twisted-pair cable with a 150kHz, 50% duty cycle square wave fro data. The data rate depends on the BPF (between Pins 3 – 4 and 5 – 6), on the AM detector capacitor for delay, C_{DET} (between Pins 7 and 8), on C_{AM} (Pin 9) for capture of leading bits, and on the desired impulse noise immunity for delay, C_{IMP} (Pin 10).

AC Line Coupling Network

One or two (120V or 240V and 277V AC RMS) coupling capacitors rated 600V are connected in series with the primary of a 1:1 transformer and connected to the AC line. The transformer secondary may be tuned to the carrier frequency by a capacitor (TOKO transformer, low data rates) or no secondary tuning capacitor for higher data rates (AIE Magnetics transformer). Two back-to-back zener diodes must be placed between Pins 1 and 20 for the IC transient protection (1N4744 or 1N6275). The transformer secondary carries DC bias current between Pins 1 and 20 of the IC. This coupling network itself attenuates to below the RX input sensitivity the 50 or 60Hz and their harmonic frequencies. In a coaxial cable application the transformer can be replaced with a coupling capacitor.

Receiver (RX)

The typical RX sensitivity is $1.5mV_{RMS}$. For less sensitivity, adjust the turn ratio of the coupling transformer or insert loss in the bandpass filter. The RX-only function can be implemented by not using the oscillator and by grounding the TX input. The maximum data rate is 300kbit/s. The power supply rejection ratio (PSRR) is 80dB for 60Hz and 120Hz. The RX is composed of the following blocks:

The Input Amplifier/Limiter limits its output signals to $1.2V_{P-P}$. The maximum input carrier signal can be $70V_{P-P}$. The gain is 24dB. The input amplifier bandpass characteristic has the upper –3dB frequency

internally fixed at 300kHz. The lower –3dB frequency is adjustable with the C_{HPF} capacitor from Pin 2 to GND. For maximum RX sensitivity CHPF = 10nF at f_{CXR} = 120kHz. A C_{HPF} = 0.1µF value attenuates 60Hz by 50dB and 120Hz by 45dB.

The Bandpass Filter is differential RLC bandpass filter which can be connected from Pins 3, 6 to Pins 4, 5. The LC values are the same as the oscillator LC values (see Pins 13 and 14). The formulae relating the BW_{-3dB} to the RLC values are:

$$\frac{BW_{-3dB}}{\omega_{CXR}} = \frac{(\omega_{CXR} \cdot L)}{(2 \cdot R)} = \frac{1}{Q}$$

$$\frac{BW_{-3dB}}{\omega_{CXR}} = \frac{1}{(\omega_{CXR} \cdot 2 \cdot C \cdot R)} = \frac{1}{Q}$$

$$BW_{-3dB} = \frac{(\omega_{CXR} \cdot \omega_{CXR} \cdot L)}{(2 \cdot R)}$$

$$BW_{-3dB} = \frac{1}{(2 \cdot C \cdot R)} \quad \text{and}$$

$$\omega_{CXR} = 2 \cdot f_{CXR}$$

If no bandpass filter is required, connect Pin 3 to 4 and Pin 5 to 6 ($R_1 = R_2 = 0\Omega$).

The Amplitude Detector is a Gilbert phase detector with a single differential input. The compared signals are always in phase and the demodulatred output is a full rectified wave, function of the bias current, the carrier amplitude, and the collector load. The detected voltage is developed across a differential capacitive load between Pin 7 (+) and Pin 8 (–). DC offset is caused by the line impedance modulation.

The AM Rejection Circuit stabilizes the DC average value of the envelope by adding or subtracting a series voltage to the voltage of the detector capacitor. The AM rejection is 40dB at a modulation rate of 120Hz. The value of the AM rejection capacitor CAM (Pin 9 to GND) determines the transition times to and from receive data and standby.

The Slicing Comparator has current output and a fixed threshold of 50mV.

The Impulse Filter consists of a capacitor, C_{IMP}, at the output of the comparator, from Pin 10 to GND. This capacitor is charged or discharged with constant current from the comparator, causing the voltage variation to be a constant slope in time. Narrow current impulses will not last long enough to fully charge or discharge the capacitor.

$2V_{BE}$ Voltage Hysteresis provides a voltage interval in which the C_{IMP} voltage ramps and in which both inputs to the SR flip-flop are zero.

The Flip-Flop is an SR type, with an open-collector transistor output at Pin 11. The transistor can switch a maximum load of 5mA.

Receiver Delays and Maximum Data Rate

The total receiver delay is a sum of delays, where t_{DET} (sec) is the detector delay, t_{IMP} (sec) is the impulse filter delay, and 2µs is the approximate receiver delay with no C_{DET} and no C_{IMP}:

t_D (sec) = total receiver delay
= t_{DET} (sec) + t_{IMP} (sec) + 2µs

The maximum bit rate, in the no-return-to-zero, amplitude shift keying data format is determined by: Maximum bit rate MRZ ASK (bit/sec) < $1/t_D$ (sec^{-1})

NOTE:
The C_{DET} and C_{IMP} values so calculated are for guidance and the user shall deterine the optimal performance values in a range between 0.1 times to 10 times the calculated values (power line environment assumed). For twisted-pair or coaxial cables the calculated values are close to optimal. Based on power line applications made at 100bits/sec and at 50kbits/sec, the C_{IMP} / C_{DET} capacitor ratio ranges from 100:1 to 1:1.

Transmitter, TX

The transmitter includes an oscillator, a line driver, and a drive switch.

The TTL Switch is a low power TTL gate that switches on/off the bias current for the line driver. A logic "1" at Pin 19 (TXIN) enables the line driver and carrier is being sent on the line. A logic "0" disables the driver.

The Oscillator is a differential transistor pair. It can be configured as a Colpitts LC oscillator, as a Pierce crystal oscillator, or used with external input (microprocessor clock divided to the carrier frequency). When the TX drive is off, the carrier leak is less than –90dBmO. Pin 18 can be used as input for an external oscillator. Grounding Pin 12 disables the oscillation process.

The Line Driver is a class AB push-pull stage with optional external complementary transistor pair for increased current capability. The TX output impedance is 40Ω in the off-state (receive mode) and less than 2Ω in the on-state (transmit mode). Note that in the transmit mode one receives its own signal. To increase the amplitude of the transmitter, add a feedback resistor in the driver amplifier feedback path at Pin 16.

By itself the NE5050 is capable of driving consumer line impedance of 50Ω (40mA peak/80mA peak non-repetitive), the THD being less than 2%. With complementary transistors, 10Ω industrial loads can be driven. With complementary Darlington transistors, 1Ω industrial loads can be driven.

One design objective was to provide the user with a flexible IC modem for residential as well as for industrial AC lines, for twisted-pair, and for coaxial cables. The IC modem can be used for control functions and data applications. Practical observations of power line noise point to a data rate upper boundary of 1kbit/sec. The main sources of interference are the light dimmers. Software for error correction can be used for improved error rates. Two system configurations can be implemented: an ASK system and a non-coherent FSK system. The non-coherent FSK system can continue to transmit ASK data if the other channel is made unusable by CW interference. High-voltage transient protection and filtering are accomplished with user-selected external components.

Additional flexibility is provided by the chip architecture: one-IC real-time repeater, one-IC dual-frequency gateway, external oscillator input port, the listen-while-talk capability (CSMA/CD), immediate TX-to-RX switching, ASK and FSK, and ASK-multinode single-frequency network.

The modem can be used for control systems and data applications in homes and other consumer environments and in industry.

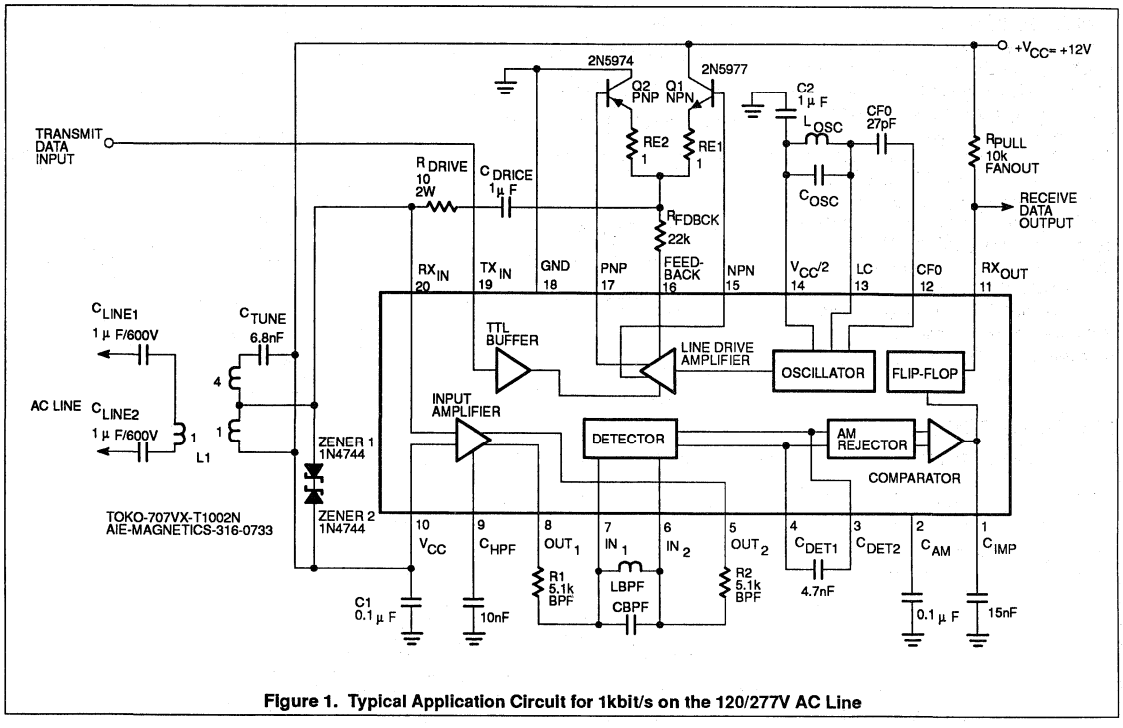


Figure 1. Typical Application Circuit for 1kbit/s on the 120/277V AC Line

High-speed FSK modem transmitter — NE5080

DESCRIPTION

The NE5080 is the transmitter chip, of a two-chip set, designed to be the heart of an FSK modem. (The NE5081 is the receiver chip.) The chips are compatible with the IEEE 802.4 standard for a "Single-Channel" Phase-Continuous-FSK Token Bus." The specifications shown in this data sheet are those guaranteed when the transmitter is tuned for the frequencies given in the 802 standard. However, both the NE5080 and the NE5081 may be used at other frequencies. The ratio of logic high to logic low frequencies is normally at 1.67 to 1.00 at any center frequency; however, it can be varied externally. (See AN1950.)

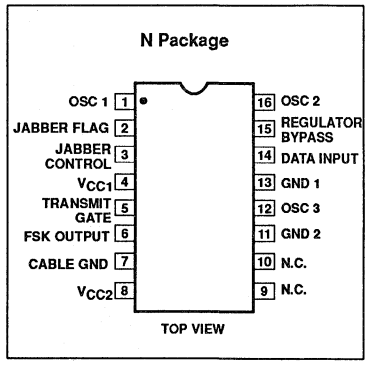
FEATURES

- Meets IEEE 802.4 standard
- Data rates to several Megabaud
- Half- or full-duplex operation
- Jabber function on-chip

APPLICATIONS

- Local Area Networks
- Point-to-point communications
- Factory automation
- Process control
- Office automation

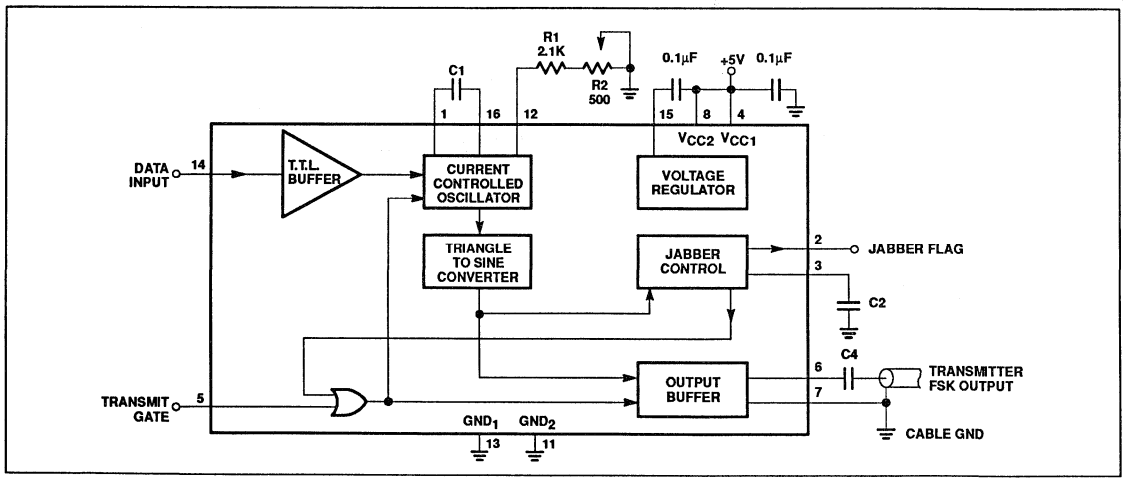
PIN CONFIGURATION



ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0°C to +70°C	NE5080N

BLOCK DIAGRAM



High-speed FSK modem transmitter | NE5080

GENERAL DESCRIPTION

The NE5080 is designed to transmit high frequency asynchronous data on coaxial cable, at rates from DC to 2M baud (see Note 1). The chip accepts serial data and transmits it as a periodic signal whose frequency depends on whether the data is high or low.

The device is meant to operate at a frequency of 6.25MHz for a logic high and 3.75MHz for a logic low (see Note 2). The frequency is set up by external trimming components; however, the ratio of the high and low frequencies is set internally and cannot be altered.

The FSK output can be turned off by use of the transmit gate pin. When turned off, the transmitter has a high output impedance and the oscillator is disabled.

The length of time a transmitter can transmit can be controlled by the use of the Jabber control pin (see description of Jabber Control Pin).

Jabber Control Pin

During the time the transmitter is transmitting, this pin sources a current. This current can be used to set the maximum time that the transmitter can be on. There are three options that can be used:

1. Use the current to charge a capacitor. When the voltage across the cap gets to approximately 1.4V, the transmitter will turn off. A logic low applied to Pin 3 will reset the Jabber function; an open collector output should be used for this purpose. A logic high applied to the pin will disable the transmitter.
2. Use to externally sense the current and have external circuitry to control the length of time the transmitter is on.
3. The pin can be tied to ground and is then not active. Transmission is then controlled solely by the signal at the transmit gate pin.

Jabber Flag Pin

This pin will go to a logic high when the Jabber Control pin is used to shut off the transmitter. It will latch and can be reset by applying a logic low to the Jabber Control pin.

NOTES:

1. The NE5080 is capable of transmitting up to 1M baud of differential Manchester code at a center frequency of 5MHz.
2. Although the chip is designed to meet the requirements of IEEE standard 802.4 (Token-Passing Single-Channel Phase-Continuous-FSK Bus), it can be used at other frequencies.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC1} V_{CC2}	Supply Voltage	+6	V
V_{IN}	Input voltage range (Data, Gate)	–0.3 to V_{CC}	V
P_D	Power dissipation	800	mW
T_A	Operating temperature range	0 to +70	°C
T_J	Maximum junction temperature	+150	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead temperature (soldering, 10sec)	300	°C

NE5080 PIN FUNCTION

PIN	FUNCTION
1	**OSC 1:** One end of the external capacitor used to set the carrier frequency.
2	**Jabber Flag:** This pin goes to a logic high if the transmitter attempts to transmit for a longer time than allowed by the Jabber control function.
3	**Jabber Control:** Used to control transmit time. See note on Jabber function.
4	**V_{CC1}:** Voltage supply.
5	**Transmit Gate:** A logic flow on this pin will enable the transmitter; a logic high will disable it.
6	**Transmitter FSK Output**
7	**Cable Ground:** The shield of the coax cable should be connected to this pin and to Pin 11.
8	**V_{CC2}:** Connect to Pin 4 close to device.
9	**No Connection**
10	**No Connection**
11	**Ground 2:** Connect to Analog ground close to device.
12	**OSC 3:** A variable resistor between this point and ground is used to set the carrier frequencies.
13	**Ground 1:** Connect to Analog close to device.
14	**Data Input**
15	**Regulator Bypass:** A bypass capacitor between this pin and V_{CC1} is required for the internal voltage regulator function.
16	**OSC 2:** One end of a capacitor that is between Pin 1 and Pin 16 and is used to set the carrier frequency.

DC ELECTRICAL CHARACTERISTICS $V_{CC1,2}$ = 4.75–5.25V, T_A = 0°C to +70°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
f_1	Output frequency (Logic high)	Data input ≥2.0V (See Note 1)	6.17	6.25	6.33	MHz
f_0	Output frequency (Logic low)	Data input ≤0.8V (See Note 1)	3.67	3.75	3.83	MHz
V_O	Output amplitude	Data input ≥2.0V or ≤0.8V Output Load = 37.5Ω	0.5		1.0	V_{RMS}
R_{OFF}	Output impedance (gated off)	Transmit gate ≥2.0V	100			kΩ
R_{ON}	Output impedance (gated on)	Transmit gate ≤0.8V			37.5	Ω
C_O	Output capacitance	Transmit gate ≥2.0V or ≤0.8V			10	pF
V_F	Feedthrough	Transmit gate ≥2.0V 2.0MHz sq. wave (TTL levels) input			1	mV_{RMS}
I_J	Jabber current	Transmit gate ≤0.8V Input ≥2.0V or ≤0.8V		1.25		μA
I_{CC}	Supply current	V_{CC1} connected to V_{CC2}		75	100	mA
Logic levels						
	Data Input					
V_{IH}	Logic high	Input high voltage	2.0			V
V_{IL}	Logic low	Input low voltage			0.8	V
I_{IH}	Input current	V_{IN} = 2.4V			40	μA
I_{IL}	Input current	V_{IN} = 0.4V			–1.6	mA
	Transmit gate					
V_{IH}	Logic high	Input high voltage	2.0			V
V_{IL}	Logic low	Input low voltage			0.8	V
I_{IH}	Input current	VG = 2.4V			40	μA
I_{IL}	Input current	VG = 0.4V			–1.6	mA
	Jabber flag					
V_{OH}	Logic high	I_{OH} = –400μA	2.4			V
V_{OL}	Logic low	I_{OL} = 4.0mA			0.4	V
	Jabber control					
V_{IH}	Logic high	Input high voltage	2.0			V
V_{IL}	Logic low	Input low voltage			0.8	V

NOTE:
1. Tuned per instructions in AN195.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
t_S	Setup time	Data in	Gate on	Figure 1	2	0.1		μs
t_A	Delay time	Output freq. change	Data transition	Figure 2			150	ns
t_B	Delay time	Output disabled	Gate off	Figure 3		0.4	2	μs
t_C	Delay time	Output disabled	Jabber control	Figure 4			100	ns
t_D	Delay time	Jabber flag	Jabber control	Figure 5			100	ns
	Jabber control reset Pulse width (Logic low)				100			ns

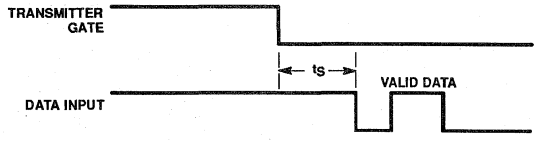


Figure 1. Setup Time, t_S

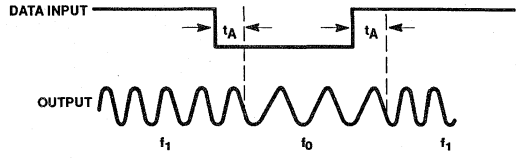


Figure 2. Delay Time, t_A

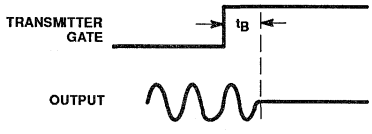


Figure 3. Delay Time, t_B

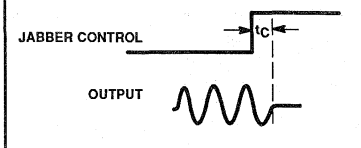


Figure 4. Delay Time, t_C

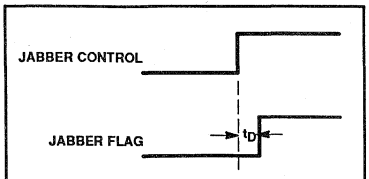


Figure 5. Delay Time, t_D

High-speed FSK modem receiver — NE5081

DESCRIPTION

The NE5081 is the receiver chip of a two-chip set designed to operate as an FSK modem (the NE5080 is the transmitter chip). The chips are compatible with the IEEE 802.4 standard for a "Single-Channel Phase-Continuous-FSK Token Bus." The specifications given in this data sheet are those guaranteed when the receiver is tuned to the frequencies given in the 802 standard. However, the receiver will work at other frequencies.

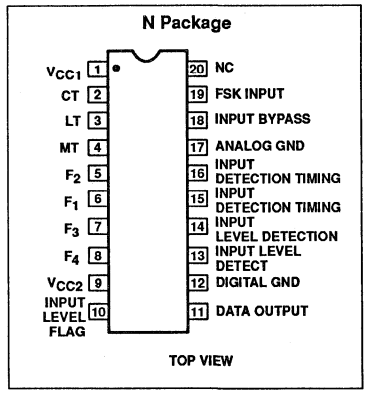
FEATURES

- Meets IEEE 802.4 standard
- Data rates to several Megabaud
- Half- or full-duplex operation
- Low bit rate error (10^{-12} typical)

APPLICATIONS

- Local Area Networks
- Point-to-point communications
- Factory automation
- Process control
- Office automation

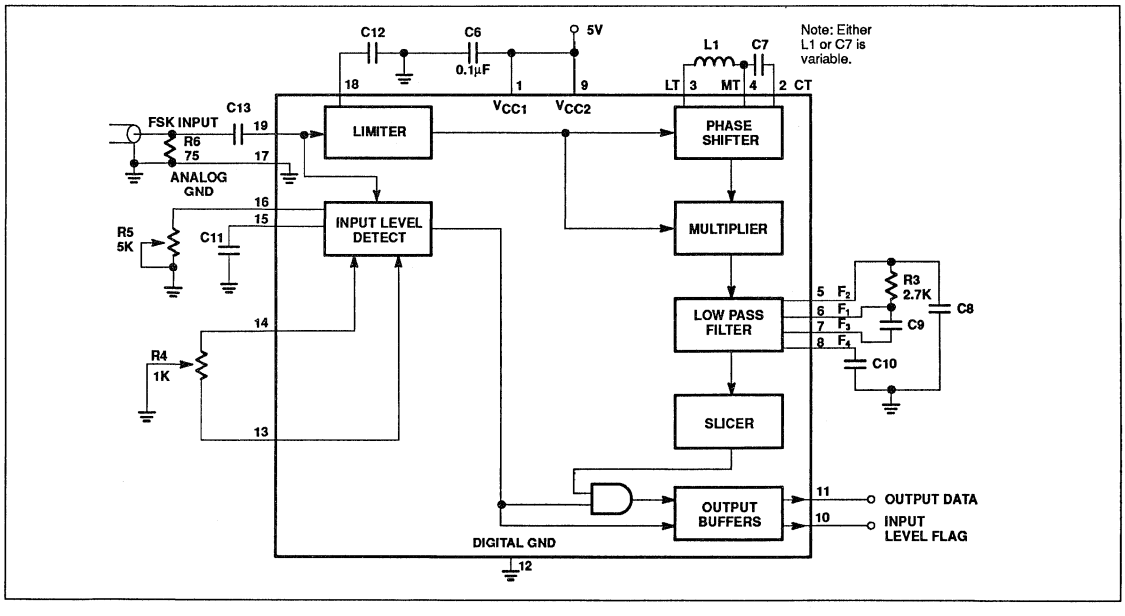
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0°C to +70°C	NE5081N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$

SYMBOL	PARAMETER	RATING	UNIT
V_{CC1} V_{CC2}	Supply voltage	+6	V
V_{IN}	Input voltage range	–0.3 to +V_{CC}	V
I_{DO}	Output (Data, Level detect) Max sink current	20	mA
P_D	Maximum power dissipation, $T_A = 25°C$, (still-air)[1] N package	1690	mW
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec. max)	300	°C
	Max differential voltage between analog and digital grounds	100	mV

NOTE:
1. Derate above 25°C as follows:
   N package at 13.5mW/°C.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1,2} = 4.75–5.25V$. External LC circuit tuned to 5MHz. Input level detect set at $16mV_{RMS}$, $T_A = 0°C$ +70°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
f_0	Logic Low Frequency	External LC tuned to 5MHz	3.67	3.75	3.83	MHz
f_1	Logic High Frequency	External LC tuned to 5MHz	6.17	6.25	6.33	MHz
IN_{DL}	Minimum Input Detect Level	Minimum input level that is detected as carrier (See Note 2 in General Description)	5		50	mV_{RMS}
	Logic Levels:					
V_{OL}	Data Output	$I_{OL} = 4.0mA$ $V_{IN} > 16mV_{RMS}$ Freq = f_0			0.4	V
V_{OH}	Data Output	$I_{OH} = –400\mu A$ $V_{IN} > 16mV_{RMS}$ Freq = f_1	2.4			V
V_{OH}	Data Output	$I_{OH} = –400\mu A$ $V_{IN} < 5mV_{RMS}$ Freq = f_0	2.4			V
V_{OL}	Input Detect Flag	$I_{OL} = 4.0mA$ $V_{IN} = 0V_{RMS}$			0.4	V
V_{OH}		$I_{OH} = –400\mu A$ $V_{IN} > 16mV$	2.4			V
I_{CC}	Supply Current	$V_{CC} = 5.25V$ (V_{CC1} connected to V_{CC2}) $V_{IN} = 1.0V_{RMS}$ Freq = f_1 or f_0			50	mA
BER	Bit Error Rate	Input Signal > $16mV_{RMS}$ maximum in-band noise = $1.6mV_{RMS}$		10^{-12}	10^{-9}	

AC ELECTRICAL CHARACTERISTICS (AN195, FIGURE 5 WITH A 100KHZ $1V_{P-P}$)

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
t_B	Delay Time	Input Level Detect Flag	Input On	Figure 1		0.05	1	µs
t_C	Delay Time	Input Level Detect Flag	Input Off	Figure 1	0.5	1.5	2.5	µs
t_D	Delay Time	Output Enabled	Input On	Figure 2			2	µs
t_E	Delay Time	Output Disabled	Input Off	Figure 2	0.5	1.5	2.5	µs
	Required Delay	Carrier Turn Off	Valid Data End		2			µs

GENERAL DESCRIPTION

The NE5081 will accept an FSK-encoded signal and provide the demodulated digital data at the output. It is optimized to work at frequencies specified in IEEE 802.4—Token-Passing Single-Channel Phase-Continuous-FSK Bus—(i.e., 3.75MHz and 6.25MHz). However, it will work at other frequencies.[1]

Its normal acceptable input signal level range is from 16mV$_{RMS}$ to 1V$_{RMS}$. This can be adjusted.[3]

The receiver will yield an undetected "Bit Error Rate" of 10^{-9} or lower when receiving signals with a 20dB signal-to-noise ratio. It has a maximum output Jitter of ± 40ns.[3]

NOTES:

1. The receiver can be tuned to accept different frequencies by adjustment of the LC circuit shown in Figure 7. However, the external components have been optimized for 3.75MHz and 6.25MHz. See "Determining Component Values" for use at other frequencies.
2. Input Level Detect
   This is a method of turning off the output of the receiver when the input signal falls below an acceptable level. This level is adjustable within the range given in the electrical specification section. The purpose of this function is to minimize the effect of noise on receiver performance and to indicate when there is an acceptable signal present at the input. All specifications given in this data sheet are with the input level detection set at 16mV$_{RMS}$.
3. Jitter (Definition)
   This is a measure of the ability of the receiver to accurately reproduce the timing of its FSK-coded digital input. The spec indicates the error band in the timing of a logic level change.

NE5081 PIN FUNCTION

PIN	FUNCTION
1	**V_{CC1}:** Should be connected to the 5V supply and Pin 9.
2	**CT:** One end of an external capacitor tthat is used to tune the receiver.
3	**LT:** One end of an indicator that is used to tune the receiver.
4	**MT:** The junction of the capacitor and inductor used for tuning the receiver.
5	**F2**
6	**F1** Pins 5, 6, 7, 8 are used for a low-pass filter to remove carrier
7	**F3** harmonics from the data output.
8	**F4**
9	**V_{CC2}:** Connect to Pin 1 (see Pin 1 function) close to the device.
10	**Input Level Flag:** This pin is used to indicate when there is a signal at the input that is greater than the level set by the input level detection circuitry. A logic high indicates an input greater than the set level.
11	**Data Output:** Supplies T^2L level data that corresponds to the FSK input received.
12	**Digital Ground:** Should be connected to digital ground.
13 and 14	**Input Level Detect:** These pins are used to set the level of input signal that the device will accept as valid.
15	**Input Detection Timing:** An external capacitor between this pin and ground is used to determine the time from carrier turn-off to output disable.
16	**Input Detection Timing:** Same as Pin 15, except that a resistor goes between this pin and ground. The values of the C and R depend on the carrier frequency. The values given in this data sheet are for a 5MHz carrier center frequency.
17	**Analog Ground:** Connect to analog ground close to the device.
18	**Input Bypass:** A capacitor between this pin and ground is used to bypass the input bias circuitry.
19	**Input:** The FSK signal from the cable goes to this pin.
20	**No Connection.**

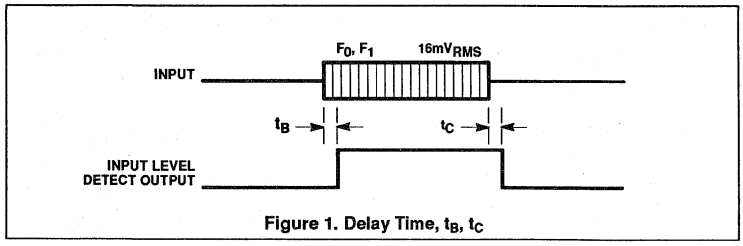


Figure 1. Delay Time, t_B, t_C

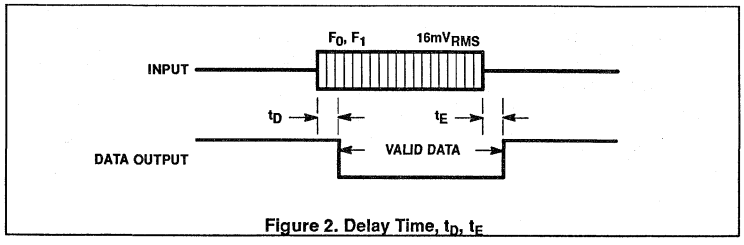


Figure 2. Delay Time, t_D, t_E

Coaxial transceiver interface for Ethernet/Thin Ethernet — NE8392A

DESCRIPTION

The NE8392A Coaxial Transceiver Interface (CTI) is a coaxial line driver/receiver for Ethernet (10base5) and Thin Ethernet (10base2) local area networks. The CTI is connected between the coaxial cable and the Data Terminal Equipment (DTE) and consists of a receiver, transmitter, collision detector, heartbeat generator and jabber timer (see Block Diagram). The transmitter output connects directly to a doubly terminated 50Ω cable, while the receiver output, collision detector output and transmitter input are connected to the DTE through isolation transformers. Isolation between the CTI and the DTE is an IEEE 802.3 requirement that can be met on signal lines by using a set of pulse transformers normally available in a standard 16-pin DIP. Power isolation for the CTI is achieved using DC-to-DC conversion through a power transformer (see Figure 1, Connection Diagram).

During transmission the jabber timer is initiated to disable the CTI transmitter in the event of a longer than legal length data packet. Collision detection circuitry monitors the signals on the coaxial cable to determine the presence of colliding packets and signals the DTE in the event of a collision. At the end of every transmission the heartbeat generator creates a pseudo collision for a short time to ensure that the collision circuitry is functioning correctly. The heartbeat function can be disabled for repeater applications.

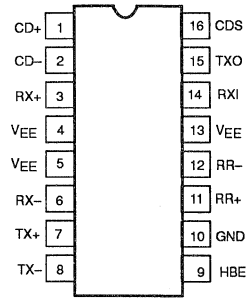
The CTI is normally part of a three chip set that implements a complete Ethernet/ Thin Ethernet network interface for a DTE (see Figure 2, Interface Diagram). The other chips are a Serial Network Interface (SNI) and a Network Interface Controller (NIC). The SNI provides Manchester Encoding and Decoding while the NIC handles the media access protocol and buffer management tasks.

FEATURES

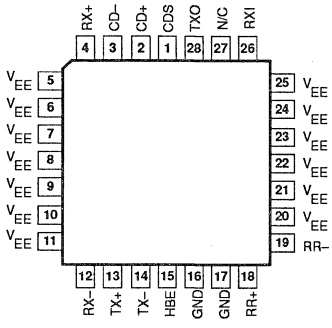
- Compatible with Ethernet II, IEEE 802.3 10base5 and 10base2, and ISO 8802/3 interface specifications
- Integrates all transceiver electronics except signal and power isolation
- Only one external resistor required for setting coaxial signaling current
- Jabber timer function integrated on chip
- Heartbeat generator can be externally disabled for operation as IEEE 802.3 compatible repeaters
- On-chip precision voltage reference for receive mode collision detection
- Squelch circuitry on all signal inputs rejects noise
- Full ESD protection
- Standard 16-pin DIP with special lead frame minimizes the operating die temperature
- Power-on reset prevents glitches on coaxial cable during power up.

PIN CONFIGURATION

N PACKAGE



A PACKAGE



ORDERING INFORMATION

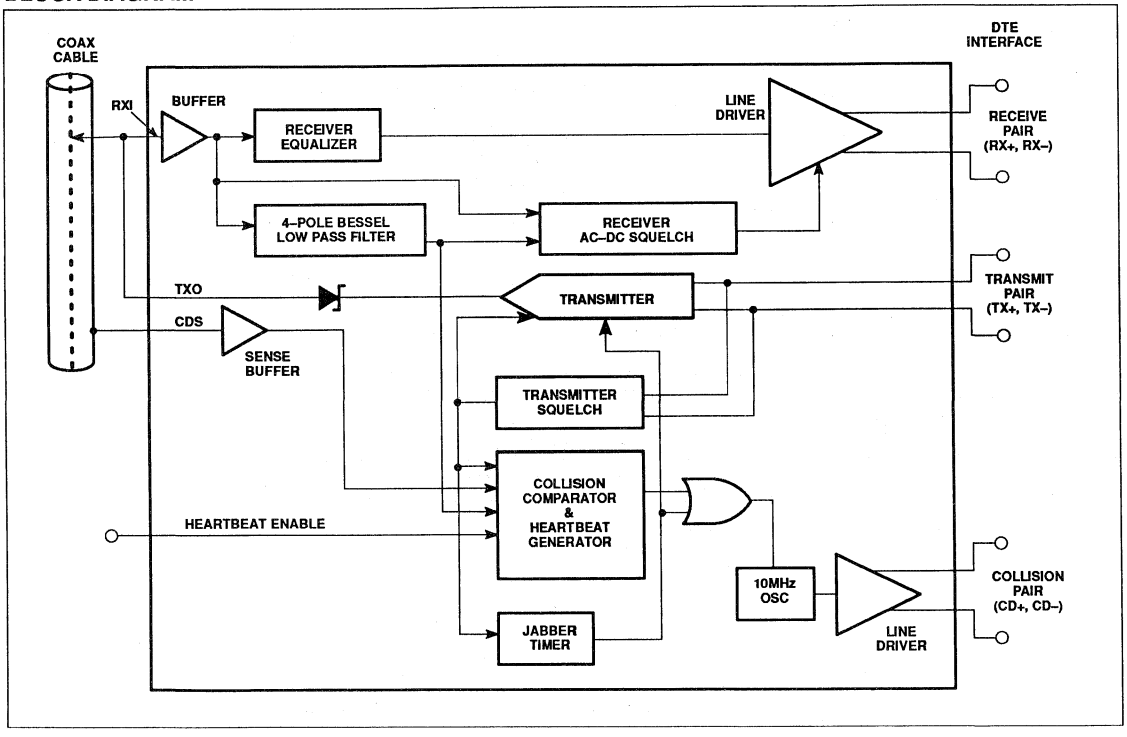
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE8392AN
28-Pin PLCC	0 to +70°C	NE8392AA

PIN DESCRIPTIONS

PIN NO. N PKG	PIN NO. PLCC	SYMBOL	DESCRIPTION
1 2	2 3	CD+ CD–	Collision Outputs. Balanced differential line driver outputs which send a 10MHz oscillation signal to the DTE in the event of a collision, jabber interrupt or heartbeat test.
3 6	4 12	RX+ RX–	Receiver Outputs. Balanced differential line driver outputs which send the received signal to the DTE.
7 8	13 14	TX+ TX–	Transmitter Inputs. Balanced differential line receiver inputs which accept the transmission signal from the DTE and apply it to the coaxial cable at TXO.
9	15	HBE	Heartbeat Enable. The heartbeat function is disabled when this pin is connected to V_{EE} and enabled when connected to GND or left floating.
11 12	18 19	RR+ RR–	External Resistor. A 1kΩ (1%) resistor connected between these pins establishes the signaling current at TXO. RR– is internally connected to V_{EE}.
14	26	RXI	Receiver Input. This pin is connected directly to the coaxial cable. Received signals are equalized, amplified, and sent to the DTE through the RX± pins.
15	28	TXO	Transmitter Output. This pin is connected directly (Thin Ethernet) or through an external isolating diode (Ethernet) to the coaxial cable.
16	1	CDS	Collision Detect Sense. Ground sense connection for the collision detection circuitry. This pin should be directly connected to the coaxial cable shield to prevent ground drops affecting the collision threshold voltage.
10	16 17	GND	Positive Supply Pin.
4 5 13	5 to 11 20 to 25	V_{EE}	Negative supply pins. These pins also serve as a low thermal resistance path for extracting heat from the die. They should, therefore, be connected to a large metal area on the PC board.

NOTE:
1. The IEEE 802.3 name for CD is CI; for RX is DI; for TX is DO.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{EE}	Supply voltage[1]	–12	V
V_{IN}	Voltage at any input[1]	0 to –12	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec.)	+300	°C
T_J	Recommended max junction temperature[2]	+130	°C
θ_{JA}	Thermal impedance (N and A packages)	60	°C/W

NOTE:

1. 100% measured in production.
2. The junction temperature is calculated from the following expression:

   $T_J = T_A + \theta_{JA}[V_{EE}(0.075 + n \times 0.05/100) + 8(V_{EE} - 2) / R]$

   where

   T_A = Ambient temperature in °C.
   θ_{JA} = Thermal resistance of package.
   V_{EE} = Normal operating supply voltage in volts.
   n = Percentage transmitter duty cycle.
   R = Pull down resistors on the RX and CD pins in Ω.

   The N package is specially designed to have a low θ_{JA} by directly connecting the four center Pins 4, 5, 12, and 13 to the die attachment area. These four pins then provide a conductive heat flow path from the die to the PCB where they should be soldered to a large area V_{EE} track. For the A package, Pins 5 to 11 and 19 to 25 should similarly be soldered to a large area V_{EE} and rack.

ELECTRICAL CHARACTERISTICS

V_{EE} = –9V ±5%; T_A = 0°C to +70°C unless otherwise specified[1,2]. No external isolation

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{POR}	Power–on reset voltage. Transmitter disabled for $\|V_{EE}\| < \|V_{POR}\|$			–6.5		V
I_{EE}	Supply current non–transmitting			–80	–130	mA
	Supply current transmitting			–125	–180	mA
I_{RXI}	Receive input bias current	V_{RXI} = 0V	–2		+25	µA
I_{CDS}	Cable sense input bias current	V_{CDS} = 0V		+2	+6	µA
V_{IH}	HBE input HIGH voltage		V_{EE} +1.4			V
V_{IL}	HBE input LOW voltage				V_{EE} +0.4	V
I_{IH}	HBE input HIGH current	V_{HBE} = 0V		250	500	µA
I_{IL}	HBE input LOW current	V_{HBE} = V_{EE}		–500	–1000	µA
I_{TDC}	Transmit output DC current level[3]		–37		–45	mA
I_{TAC}	Transmit output AC current level[3]		±28		$\pm I_{TDC}$	mA
I_{TX10}	Transmit current	V_{TXO} = –10V	–250		+250	µA
V_{TCOM}	Transmitter output voltage compliance[4]				–3.7	V
V_{CD}	Collision threshold[5]	Measured by applying DC voltage at RXI	–1450	–1530	–1580	mV
V_{OD}	Differential output voltage – non idle at $RX\pm$ and $CD\pm$[6]		±600		±1200	mV
V_{OB}	Differential output voltage imbalance – idle at $RX\pm$ and $CD\pm$[7]				±40	mV
V_{OC}	Output common mode voltage at $RX\pm$ and $CD\pm$		–1.5	–2	–2.5	V
V_{RS}	Receiver squelch threshold	V_{RXI} average DC	–130	–250	–370	mV
V_{TS}	Transmitter squelch threshold	$(V_{TX+} - V_{TX-})$ peak	–175	–225	–300	mV
R_{RXI}	Shunt resistance at RXI non–transmitting		100			kΩ
C_{RXI}	Input capacitance at RXI			2		pF
R_{TXO}	Shunt resistance at TXO transmitting			10		kΩ

NOTES:

1. Currents flowing into device pins are positive. All voltages are referenced to ground unless otherwise specified. For ease of interpretation, the parameter limit that appears in the MAX column is the largest value of the parameter, irrespective of sign. Similarly, the value in the MIN column is the smallest value of the parameter, irrespective of sign.
2. All typicals are for V_{EE} = –9V and T_A = 27°C.
3. I_{TDC} is measured as $(V_{MAX} + V_{MIN})/(2 \times 25)$ where V_{MAX} and V_{MIN} are the max and min voltages at TXO with a 25Ω load between TXO and GND. I_{TAC} is measured as $(V_{MAX} - V_{MIN})/(2 \times 25)$.
4. The TXO pin shall continue to sink at least I_{TDC} min when the idle (no signal) voltage on this pin is –3.7V.
5. Collision threshold for an AC signal is within 10% of V_{CD}.
6. Measured on secondary side of isolation transformer (see Connection Diagram, Figure 1). The transformer has a 1:1 turns ratio with an inductance between 30 and 100µH at 5MHz.
7. Measured as the voltage difference between the RX pins or the CD pins with the transformer removed.

TIMING CHARACTERISTICS

V_{EE} = –9V ±5%; T_A = 0 to 70°C, unless otherwise specified[1]. No external isolation diode on TXO.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{RON}	Receiver start up delay RXI to RX± (Figure 3) First received bit on RX±	V_{RXI} = –2V peak			5	bits
	First validly timed bit on RX±				t_{RON} +2	bits
t_{RD}	Receiver prop. delay RXI to RX±	V_{RXI} = –2V peak		35	50	ns
t_{RR}	Differential output rise time on RX± and CD±[2,3]			5		ns
t_{RF}	Differential output fall time on RX± and CD±[2,3]			5		ns
t_{OS}	Differential output settling time on RX± and CD± to V_{OB} = 40mV[2] (see Figure 5)			1		µs
t_{RJ}	Receiver and cable total jitter			±3		ns
t_{RHI}	Receiver high to idle time	Measured to +210mV	150		850	ns
t_{RM}	Rise and fall time matching on RX± and CD±	$t_{RF} - t_{RR}$		0.4		ns
t_{TST}	Transmitter start–up delay TX± to TXO (Figure 4)	$V_{TX±}$ = –1V peak				
	First transmitted bit on TXO			1	2	bits
	First validly timed bit				t_{TST} + 2	bits
t_{TD}	Transmitter prop delay TX± to TXO (see Figure 4)	$V_{TX±}$ = 1V peak		35	50	ns
t_{TR}	Transmitter rise time 10% to 90% (see Figure 4)			25		ns
t_{TF}	Transmitter fall time 10% to 90% (see Figure 4)			25		ns
t_{TM}	$t_{TF} - t_{TR}$ mismatch			±2		ns
t_{TS}	Transmitter added skew[4]			±2		ns
t_{TON}	Transmitter turn on pulse width (see Figure 4)	$V_{TX±}$ = 1V peak	10		40	ns
t_{TOFF}	Transmitter turn off pulse width (see Figure 4)	$V_{TX±}$ = 1V peak	150	250	340	ns
t_{CON}	Collision turn on delay (see Figure 6)	0V to –2V step at RXI			13	bits
t_{COFF}	Collision turn off delay (see Figure 6)	–2V to 0V step at RXI			16	bits
t_{CHI}	Collision high to idle time (see Figure 6)	Measured to +210mV	150		850	ns
f_{CD}	Collision frequency (see Figure 6)		8.0	10	12.5	MHz
t_{CP}	Collision signal pulse width (see Figure 6)		35		70	ns
t_{HON}	Heartbeat turn on delay (see Figure 7)		0.6		1.6	µs
t_{HW}	Heartbeat test duration (see Figure 7)		0.5		1.5	µs
t_{JA}	Jabber activation delay measured from TX± to CD± (see Figure 8)		20		60	ms
t_{JR}	Jabber reset delay measured from TX± to CD± (see Figure 8)		250		750	ms

NOTES:

1. All typicals are for V_{EE} = –9V and T_A = 27°C.
2. Measured on secondary side of isolation transformer (see Figure 1, Connection Diagram). The transformer has a 1:1 turn ratio with an inductance between 30 and 100µH at 5MHz.
3. The rise and fall times are measured as the time required for the differential voltage to change from –225mV to +225mV, or +225mV to –225mV, respectively.
4. Difference in propagation delay between rising and falling edges at TXO.

FUNCTIONAL DESCRIPTION

The NE8392A contains four main functional blocks (see Block Diagram). These are:

a. The receiver which takes data from the coaxial cable and sends it to the DTE.

b. The transmitter which receives data from the DTE and sends it onto the coaxial cable.

c. The collision detection and heartbeat generation circuitry which indicates to the DTE any collision on the coaxial cable and tests for collision circuitry functionality at the end of every transmission.

d. The jabber timer which disables the transmitter in the event of a longer than legal length data packet.

Receiver Functions

The receiver consists of an input buffer, a cable equalizer, a 4-pole Bessel low pass filter, a squelch circuit and a differential line driver.

The buffer provides high input resistance and low input capacitance to minimize loading and reflections on the coaxial cable.

The equalizer is a high pass filter that compensates for the low pass effect of the coaxial cable and results in a flatband response over all signal frequencies to minimize signal distortion.

The 4-pole Bessel low pass filter extracts the average DC voltage level on the coaxial cable for use by the receiver squelch and collision detection circuits.

The receiver squelch circuit prevents noise on the coaxial cable from falsely triggering the receiver in the absence of a true signal. At the beginning of a packet, the receiver turns on when the DC level from the low pass filter is lower than the DC squelch threshold. For normal signal levels this will take less than 500ns, or 5 bits. However, at the end of a packet, a fast receiver turn off is needed to reject both dribble bits on the coaxial cable and spurious responses due to settling of the on-chip bandpass filter. This is accomplished by an AC timing circuit that disables the receiver if the signal level on the coaxial cable remains high for typically 250ns and only enables the receiver again after approximately 1µs. Figures 3 and 5 illustrate receiver timing.

The differential line driver provides typically ±900mV signals to the DTE with less than 7ns rise and fall times. When in idle state (no received signal) its outputs provide <20mV differential voltage offset to minimize DC standing current in the isolation transformer.

The line driver outputs are emitter followers and, for Ethernet applications where they drive a 78Ω transmission line, require a 500Ω pull-down resistor to V_{EE}. For Thin Ethernet applications where the AUI cable is not used, the pull-down resistor can be increased to 1.5kΩ to save power consumption.

Transmitter Functions

The transmitter has differential inputs and an open collector current driver output. The differential input common mode voltage is established by the CTI and should not be altered by external circuitry. Controlled rise and fall times of 25ns (±5ns) minimize higher harmonic components in the transmitted spectrum, while matching of these rise and fall times to typically 2ns minimizes signal jitter. The drive current levels of the CTI are set by an on-chip bandgap voltage reference and an external 1% resistor. An on-chip isolation diode is provided to reduce the transmitter's coaxial cable load capacitance. For Thin Ethernet applications, no further external isolation diode is required, since the NE8392A meets the capacitive loading specifications. For Ethernet applications a further external diode should be added to reduce loading capacitance.

The transmitter squelch circuit ensures that the transmitter can only be enabled by negative-going differential signals of typically greater than 225mV in magnitude and 15ns in duration. The transmitter will be disabled at the end of a packet if there are no negative going signals of greater than 225mV for more than typically 250ns. Figure 4 illustrates transmitter timing.

Collision Functions

The collision detection scheme implemented in the NE8392A is receive mode detection, which detects a collision between any two stations on the network with certainty at all times, irrespective of whether or not the local DTE is producing one of the colliding signals. This is the only detection scheme allowed by the IEEE 802.3 standard for both repeater and non-repeater nodes.

The collision circuitry consists of the 4-pole Bessel low pass filter, a comparator, a precision voltage reference that sets up the collision threshold, a heartbeat generator, a 10MHz oscillator, and a differential line driver.

The collision comparator monitors the DC level at the output of the low pass filter and enables the line driver if it is more negative than the collision threshold. A collision condition is indicated to the DTE by a 10MHz oscillation signal at the CD outputs and typically occurs within 700ns of the onset of the collision. The collision signal begins with a negative-going pulse and ends with a continuous high-to-idle state longer than 170ns. Figure 6 illustrates collision timing.

At the end of every transmission, the heartbeat generator creates a pseudo collision to ensure that the collision circuitry is properly functioning. This pseudo collision consists of a 1µs burst of 10MHz oscillation at the line driver outputs approximately 1µs after the end of the transmission. The heartbeat function can be disabled externally by connecting the HBE (heartbeat enable) to V_{EE}. This allows the CTI to be used in repeater applications. Figure 7 illustrates heartbeat timing.

As with the receiver outputs, the collision outputs also require a pull down resistor to V_{EE} and maintain <20mV differential voltage offset in the idle state to minimize DC standing current in the isolation transformers.

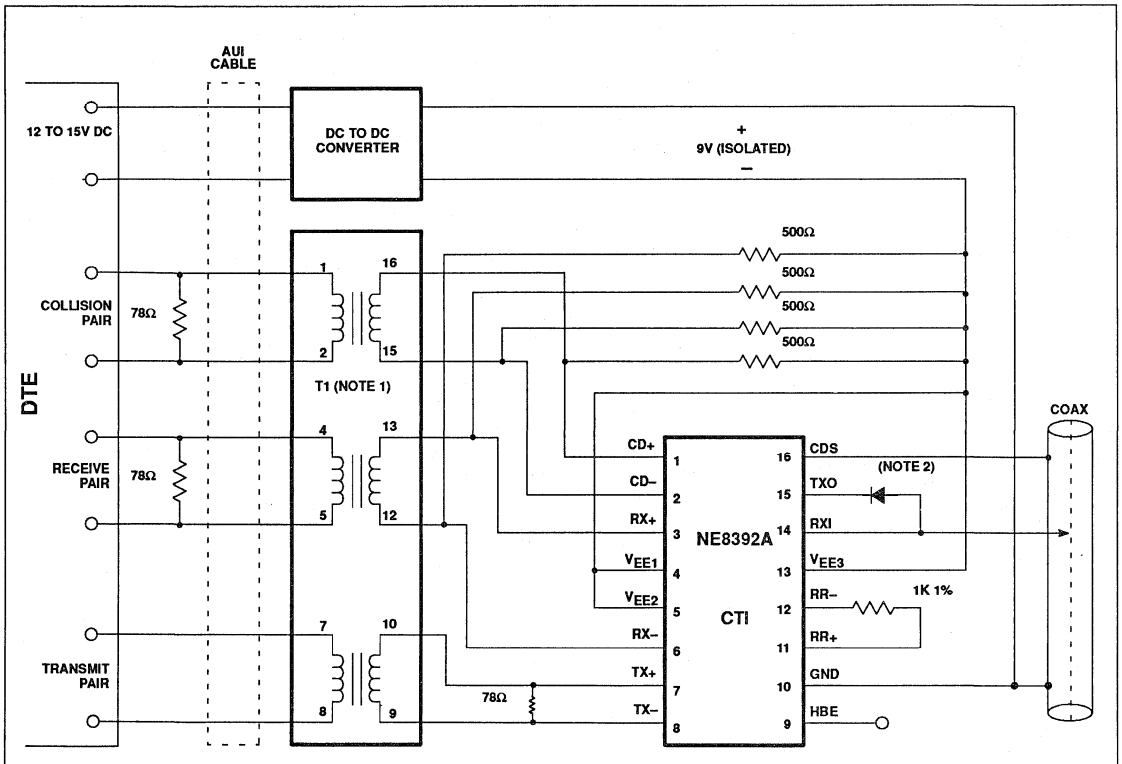
Jabber Functions

The jabber timer monitors the transmitter and inhibits transmission if it is active for longer than typically 30ms. The jabber circuit then enables the collision outputs for the remainder of the data packet and for typically 450ns (unjab time) after it has ended. At this point the transmitter becomes uninhibited. Figure 6 illustrates jabber timing.

Detection of Coaxial Cable Faults

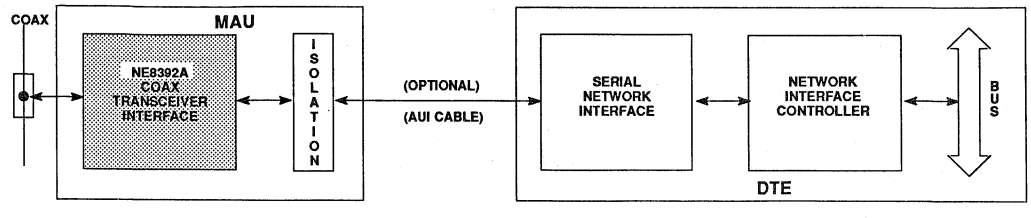
In the NE8392A there is no internal loopback path from the TX inputs to the RX outputs. This means that, when the local DTE is transmitting, the signal will only be present at the receiver outputs RX+ and RX– if it appears on the coaxial cable and is larger than the receiver squelch threshold V_{RS}. If a short circuit fault condition occurs at the cable connector to the CTI, then no signal will appear at the receiver outputs. An intelligent DTE can, therefore, detect this fault. If the fault is an open circuit, then a continuous collision signal will be sent to the DTE, provided the average DC voltage at the RXI pin is greater than the typical collision threshold of –1.53V.

If a short or open circuit occurs elsewhere on the coaxial cable, the resulting reflections can result in an impedance at the CTI of any value between a short circuit and 50Ω, depending on the distance of the CTI from the fault. The upper limit of 50Ω results from the fact that the coaxial cable is terminated in 50Ω at both ends. Faults on the cable itself are, therefore, not guaranteed to be detected by simply monitoring the RX and CD pins when in the transmit mode, and more sophisticated schemes may be necessary.



NOTES:
1. T1 is a 1:1 pulse transformer, with an inductance of 30 to 100μH.
2. IN916 or equivalent for Ethernet, not required for Thin Ethernet.

Figure 1. Connection Diagram



MAU = Medium Attachment Unit
AUI Cable = Attachment Unit Interface Cable (not used in Thin Ethernet applications)

Figure 2. Interface Diagram for Ethernet/Thin Ethernet Local Area Network

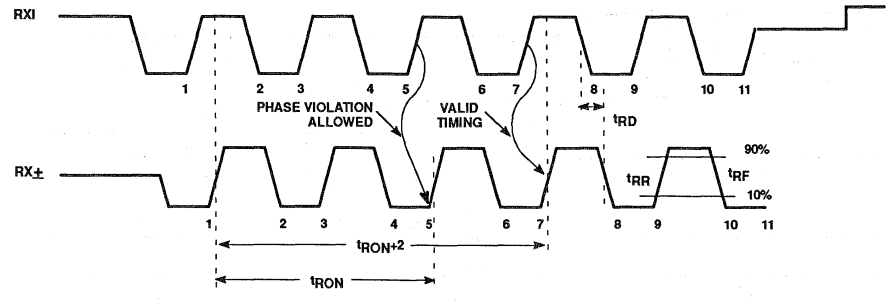


Figure 3. Receiver Timing

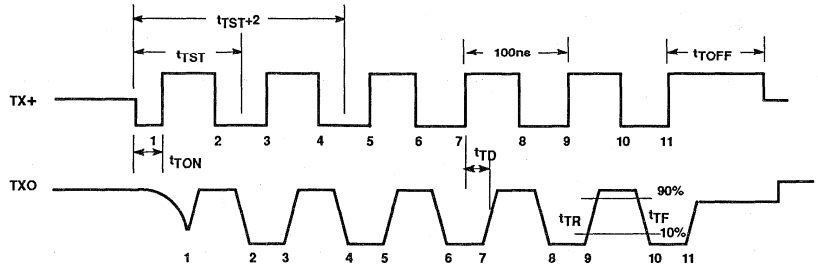


Figure 4. Transmitter Timing

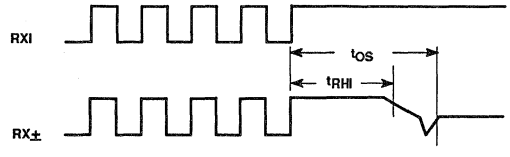


Figure 5. Receiver End–of–Packet Timing

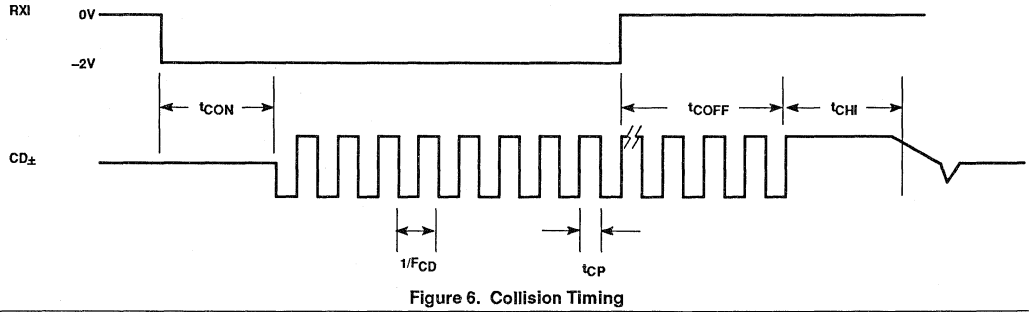


Figure 6. Collision Timing

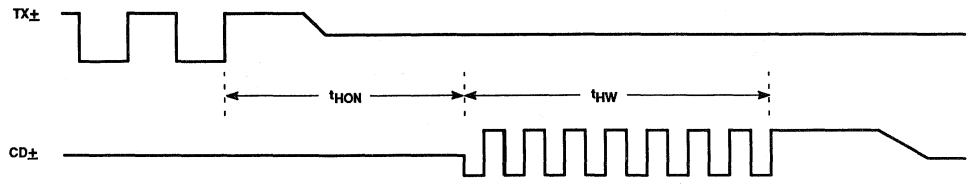


Figure 7. Heartbeat Timing

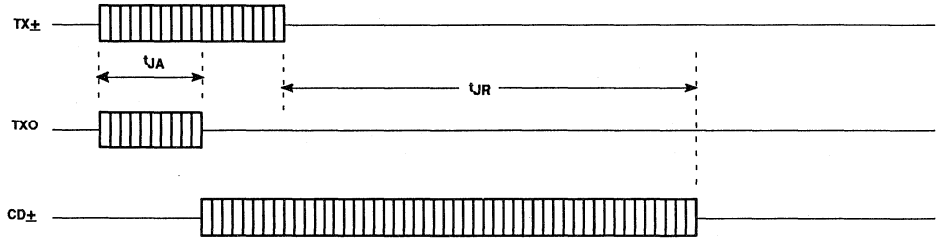


Figure 8. Jabber Timing

Twisted-pair transceiver interface — NE86C92

DESCRIPTION

The NE86C92 is a twisted-pair transceiver that implements the IEEE 802.3 10BASE-T Ethernet specification. The circuit provides the connection between the Manchester encoder/decoder and the twisted-pair cable and includes a receiver, transmitter, collision detector, heartbeat generator, jabber timer, link integrity monitor, and control circuits and drivers for five LED status indicators.

The NE86C92 includes receive polarity detection with automatic polarity correction, smart squelch on all signal inputs for improved noise immunity, and a highly reliable crystal oscillator to set pre-distortion timing and the collision signal frequency.

The NE86C92 also allows for automatic selection between AUI and twisted-pair (RJ-45) connections; thus eliminating the need for end-users to remove the interface board and move jumpers to switch between connections. An application note is available which describes implementation of this feature.

The twisted-pair outputs and inputs connect to the twisted-pair cable through transmit and receive filters while the receiver output, collision detector output and transmitter input are connected to the Manchester encoder/decoder through pulse transformers. This interface to the encoder/decoder is, therefore, directly compatible with current 10Base2/10Base5 connections and allows easy expansion of existing interface cards for twisted-pair wiring.

During transmission the jabber timer is initiated to disable the NE86C92 in the event of a longer than legal length data packet. Collision detection circuitry monitors both the transmit path and the receiver input to determine the presence of colliding packets and signals the Manchester encoder/decoder in the event of a collision. At the end of every transmission the heartbeat generator creates a pseudo collision for a short time to ensure that the collision circuitry is functioning correctly. The link integrity monitor emits pulses onto the twisted-pair cable and expects to receive pulses from the twisted-pair cable at regular intervals. If no pulses or packets are received, a link failure has occurred; this is indicated by the RLED status indicator. Both heartbeat and link integrity monitor functions can be disabled.

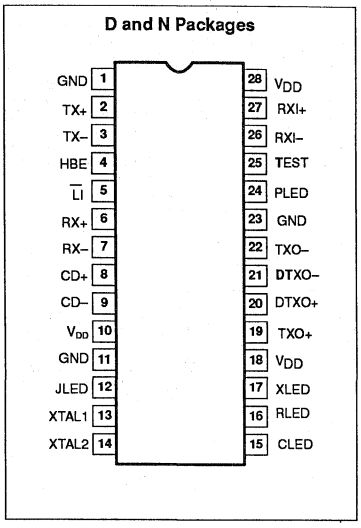
The NE86C92 is normally part of a three chip set for implementing a complete twisted-pair Ethernet network interface. The other chips are the Manchester encoder/decoder, such as the NE502A, and a Network Interface Controller, such as the NE86950.

FEATURES

- Compatible with IEEE 802.3 10BASE-T specifications
- Integrates all transceiver functions, with selectable heartbeat and link test generators
- Twisted-pair polarity detection and automatic correction
- Smart squelch on all data inputs
- Internal transmitter pre-distortion generator
- Supports automatic selection between AUI and RJ-45 connections
- Five LED status signals with on-chip drivers for transmit, receive and link integrity, collision, jabber status and twisted pair polarity reversal
- Advanced CMOS process uses single 5V supply
- Extremely low power operation: 24mA typical idle current

PIN CONFIGURATION

D and N Packages



APPLICATIONS

- 10BASE-T network interfaces for computers and workstations
- External 10BASE-T transceiver units

ORDERING INFORMATION

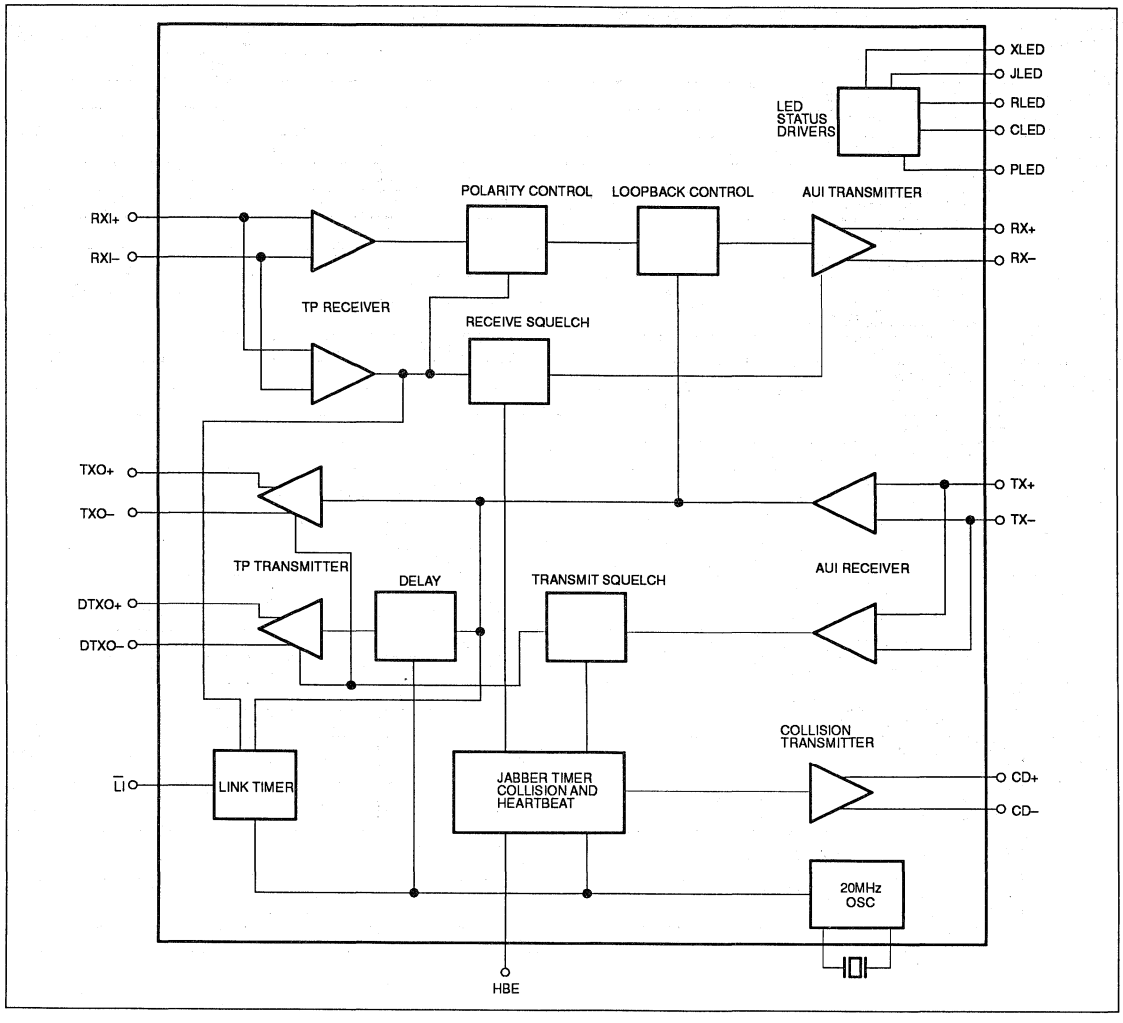
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (.600 in. wide)	0 to 70°C	NE86C92N
28-Pin Plastic SO (surface mount)	0 to 70°C	NE86C92D

PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	GND	Ground
2, 3	TX+, TX–	Transmitter inputs. Balanced differential line receiver. Inputs which accept the transmission signal from the Manchester encoder/decoder and apply it to the Twisted-Pair cable at TXO+, DTXO+, TXO– and DTXO-.
4	HBE	Heartbeat Enable. The heartbeat function is disabled when this pin is connected to GND and enabled when connected to V_{DD} or left floating.
5	$\overline{LI}$	Link Integrity. The link integrity function is disabled when this pin is connected to V_{DD} or left floating and enabled when connected to GND.
6, 7	RX+, RX-	Receive Outputs. Balanced differential line driver outputs which send the received signal to the Manchester encoder/decoder.
8, 9	CD+, CD-	Collision Outputs. Balanced differential line driver outputs which send a 10MHz oscillation signal to the Manchester encoder/decoder in the event of a collision, jabber interrupt or heart beat test.
10	V_{DD}	Positive power supply
11	GND	Ground.
12	JLED	Jabber Indicator. Indicates that the jabber timer has timed out and the twisted-pair drivers are disabled.
13	XTAL1	Crystal pin. One terminal of 20MHz crystal; or 20MHz external clock input.
14	XTAL2	Crystal Pin. One terminal of 20MHz crystal.
15	CLED	Collision Indicator. Indicates that a collision has been detected.
16	RLED	Receive Indicator. Indicates a packet is being received from the twisted-pair cable.
17	XLED	Transmit Indicator. Indicates a packet is being transmitted onto the twisted-pair cable.
18	V_{DD}	Positive power supply
19 20 21 22	TXO+, DTXO+, DTXO-, TXO-	Twisted-Pair drivers. These four outputs provide twisted-pair drive with pre-distortion. TXO+ and TXO- are balanced differential outputs that follow the signal at the TX+ and TX- inputs. DTXO+ and DTXO- are delayed and inverted with respect to TXO– and TXO+. Combining these outputs through an external resistor network provides the necessary pre-distortion to overcome the twisted-pair cable attenuation characteristics.
23	GND	Ground.
24	PLED	Polarity reversal indicator. Indicates polarity reversal of the twisted-pair receiver wires. A no-connect at this pin enables auto-correction although there is no LED indication. Connecting to GND disables auto-correction.
25	TEST	Test. No Connection, or connect to ground.
26, 27	RXI-, RXI+	Receiver inputs. These inputs receive the data from the twisted-pair cable and pass it on to RX+ and RX-.
28	V_{DD}	Positive power supply.

NOTE: The IEEE 802.3 designation for CD is CI, for RX is DI, for TX is DO, for RXI is RD and for TXO and DTXO combined is TD.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage with respect to GND	-0.5 to +6.5	V
V_{IN}	Voltage at any input to GND	-0.5 to V_{DD} +0.5	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec)	+300	°C
T_J	Recommended max junction temperature	+125	°C
θ_{JA}	Thermal impedance N package D package	55 70	°C/W °C/W

ELECTRICAL CHARACTERISTICS

V_{DD} = +5V ±10%, T_A = 0°C to 70°C; unless otherwise stated. Typical values measured at V_{DD} = +5V, T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Power supply threshold and currents						
V_{DDEN}	Enable V_{DD} threshold			3.4		V
V_{DDDIS}	Disable V_{DD} threshold			1.2		V
I_{DDI}	Supply current (no traffic)			20		mA
I_{DDT}	Supply current transmitting	TXO± RXI± active, 90% duty cycle		65	100	mA
Digital input voltage (HBE, $\overline{LI}$)						
V_{IL}	Input LOW voltage		GND - 0.3		0.8	V
V_{IH}	Input HIGH voltage		2.0		V_{DD} + 0.3	V
Digital input current (HBE, $\overline{LI}$, PLED)						
I_{IN}	Input current	GND - 0.3 < V_{IN} < V_{DD} + 0.3	-500		0	µA
LED driver output voltage						
V_{OL}	Output LOW voltage	I_{OUT} = 10mA			0.4	V
LED driver leakage current						
I_{OL}	Output leakage current, output inactive	GND < V_{OUT} < V_{DD} + 0.3			+10	µA
I_{OLPLED}	PLED output leakage current, inactive	GND < V_{OUT} < V_{DD} + 0.3			+250	µA
Transmitter, receiver and collision indicator						
V_{OC}	TX±, RXI± open circuit input voltage		1.5		3.5	V
I_{ITR}	TX+, TX-, RXI+, RXI- input current	GND - 0.3 < V_{IN} < V_{DD} + 0.3	-500		+500	µA
R_{TX}	TX± differential input resistance		16			kΩ
V_{TS}	Transmitter squelch threshold		-150	-200	-300	mV
V_{OH}	Output HIGH voltage TXO±, DTXO±	Load = 500Ω to GND	V_{DD} – 0.1			V
V_{OL}	Output LOW voltage TXO±, DTXO±	Load = 500Ω to V_{DD}			0.1	V
R_{RXI}	RXI± differential input resistance		20			kΩ
V_{RS}	Receive squelch threshold		±300	±400	±585	mV
V_{OD}	Differential output voltage non-idle at RX±, CD±	R_L = 78Ω	±600	±825	±1200	mV
V_{OB}	Differential output voltage imbalance at RX±, CD±, idle and non-idle	R_L = 78Ω	-40		+40	mV
V_{TPOD}	Peak differential output voltage	R_L = 100, R_1 = 48, R_2 = 464		2.8		V
V_{TOB}	Differential output voltage imbalance at TXO±, DTXO± idle and non-idle		-40		+40	mV
R_{TS}	TXO±, DTXO± output resistance	I = 25mA		7	10	Ω

TIMING CHARACTERISTICS

V_{DD} = +5V ±10%, T_A = 0°C to 70°C; unless otherwise stated. Typical values measured at V_{DD} = +5V, T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Receiver and collision signal						
t_{RST}	Receive start-up delay	$V_{RXI\pm}$ = 1V peak		250	500	ns
t_{RBL}	Bits lost at receiver start-up	$V_{RXI\pm}$ = 1V peak		2	4	bits
	First validly timed bit on RX±				t_{RBL} + 2	bits
t_{RD}	Receiver propagation delay RXI± to RX±	Include receive filter		40	100	ns
t_{ROFF}	Receiver turn-off pulse width		150		230	ns
t_{RHI}	Receiver high-to-idle time	Measured to ±210mV	200		400	ns
t_{CHI}	Collision high-to-idle time	Measured to ±210mV	400		500	ns
t_{RR}	Differential output rise time on RX±, CD±				5	ns
t_{RF}	Differential output fall time on RX±, CD±				5	ns
t_{RM}	Rise and fall time matching on RX±, CD±	t_{RF} - t_{RR}	-2		2	ns
t_{RJ}	Receiver added jitter RXI± to RX±	$V_{RXI\pm}$ = 1V peak	-1.5		+1.5	ns
t_{CMJ}	Receiver added common-mode jitter RXI± to RX±	$V_{RXI\pm}$ = 2.5V at receive filter input	-2.5		+2.5	ns
Transmitter						
t_{TST}	Transmit start-up delay	$V_{TX\pm}$ = 1V peak		280	400	ns
t_{TBL}	Bits lost at transmitter start-up	$V_{TX\pm}$ = 1V peak			2	bits
	First validly timed bit				t_{TBL+2}	bits
t_{TD}	Transmit propagation delay	$V_{TX\pm}$ = 1V peak (include transmitter filter)		50	100	ns
t_{TS}	Transmitter added jitter	Load = 100Ω and cable model	-3.5		+3.5	ns
t_{TOFF}	Transmitter turn off pulse width	$V_{TX\pm}$ = 1V	150		200	ns
t_{THI}	Transmitter high to idle time		250		450	ns
t_{PDPW}	Pre-distortion pulse width		45		55	ns
Link integrity						
t_{LTSD}	Transmit silence duration		8	16	24	ms
t_{LTPW}	Link test pulse width	With 100Ω load/measure at 585mV amplitude point	80		120	ns
t_{ICLTP}	Time period for ignored consecutive link pulses	$V_{RXI\pm}$ = 1V peak	2	5	7	ms
t_{CCLTP}	Time period for counted consecutive link pulses	$V_{RXI\pm}$ = 1V peak	25	48	150	ms
t_{LLD}	Link loss detect time		50	110	150	ms
Collision and jabber						
f_{CD}	Collision frequency		8.5	10.0	11.5	MHz
t_{CP}	Collision signal pulse width		40	50	60	ns
t_{CON}	Collision turn-on delay				9	bits
t_{COFF}	Collision turn-off delay				9	bits
t_{HON}	Heartbeat turn-on delay		0.6	1.1	1.6	µs
t_{HW}	Heartbeat test duration		0.5	1.0	1.5	µs
t_{JA}	Jabber activation delay		20	50	150	ms
t_{JR}	Jabber reset delay		250	450	750	ms

TIMING CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Loopback						
t_{LBON}	Loopback start-up delay				9	bits
t_{LBE}	Loopback enable time RXI± to RX±				9	bits
t_{LBD}	Loopback disable time RXI± to RX±				9	bits
t_{LBPD}	Loopback propagation delay TXI± to RX±				200	ns
LEDs						
t_{LED}	Turn-on or turn-off delay of LEDs				10	µs
$t_{XLEDOFF}$	XLED maximum off time		95		135	ms
t_{XLEDON}	XLED minimum on time		5		10	ms
$t_{RLEDOFF}$	RLED maximum off time	$\overline{LT}$ = high (V_{DD})	95		135	ms
t_{RLEDON}	RLED minimum on time		5		10	ms
t_{RLEDLL}	RLED turn-off time for link loss[1]			t_{LL}		ms
t_{RLEDLE}	RLED on time after link re-established	$\overline{LT}$ = low (GND)	0.5		1.5	sec
t_{CLEDON}	CLED minimum on time		10	11.5	14	ms
t_{JLEDON}	JLED on time[2]	ON while jabber is active		t_{JON}		ms
$t_{JLEDOFF}$	JLED off time[3]	OFF while jabber is inactive		t_{JOFF}		ms

NOTES:
1. t_{LL} = duration of link loss
2. t_{JON} = jabber active time.
3. t_{JOFF} = jabber inactive time

FUNCTIONAL DESCRIPTION

The NE86C92 contains eight main functional blocks (see Block Diagram). These are:

1. The receiver which takes data from the twisted-pair cable and sends it to the Manchester encoder/decoder.
2. The receive polarity detector and correction control which detects the polarity of the received signal and internally corrects the polarity of a reversed polarity connection.
3. The transmitter which receives data from the Manchester encoder/decoder and sends it onto the twisted-pair cable.
4. The collision detection and heartbeat generation circuitry which indicates to the Manchester encoder/decoder any collision resulting from a coincident transmit and receive activity and tests for collision circuitry functionality at the end of every transmission.
5. The jabber timer which disables the transmitter in the event of a longer than legal length data packet.
6. The link integrity monitor which periodically tests the integrity of the twisted-pair link and indicates if a link failure occurs.
7. A crystal controlled oscillator which provides all on-chip timing functions for control, pre-distortion and the 10MHz collision signal.
8. LED control circuitry and drivers for indicating the transmit, receive and link integrity, collision, jabber and Twisted-Pair polarity status of the NE86C92.

Receiver Functions

The receiver section consists of a differential twisted-pair receiver, a squelch circuit and a differential line driver for the AUI cable.

The twisted-pair receiver is connected to the output of a bandpass filter whose input is transformer coupled to the twisted- pair cable. The receiver has a high differential input impedance to allow accurate external resistors to be used for matching to the bandpass filter. The common mode voltage of the input buffer is set internally on the chip.

The receiver squelch circuit prevents noise on the twisted-pair cable from falsely triggering the receiver in the absence of true data. The twisted-pair receiver will be activated if the differential signal at the RXI pins exceeds typically ±400mV and has a low-high-low sequence with both the positive and negative pulse widths exceeding 50ns. Once activated the squelch threshold reduces to ±200mV to ensure reception. The fifth bit of the Manchester code is always received. The receiver is de-activated by a continuous high of between 150ns and 230ns. The receiver is then inhibited for a further 500ns at the end of a packet in order to reject dribble bits or the twisted-pair cable.

The data packet passed on to the Manchester encoder/decoder will typically have a high-to-idle time of 300ns.

The differential line driver provides typically ±825mV signals into a 78Ω transmission line connecting the transceiver to the Manchester encoder/decoder with rise and fall times less than 5ns. When in the idle state (no received or transmitted signal) both outputs are pulled to GND and provide < 40mV differential voltage offset to minimize DC standing current in the transformer.

Polarity Control Functions

The polarity control circuitry consists of a polarity detector and a polarity correction circuit. The polarity detector is activated following a link failure or power-on reset. It then waits for the detection of four consecutive link test pulses of the same

polarity, or the reception of a data frame to determine the correct polarity. Having determined the correct polarity, the correction circuit provides the correct data polarity to the receiver and the link integrity pulse detector.

The PLED pin provides a buffered output indication of the status of the polarity correction circuit. This output may be used to drive an LED directly (through an external current limiting resistor to V_{DD}) for visual indication of polarity.

The polarity detection and correction circuit may be externally DISABLED by connecting PLED (Pin 24) to ground.

Transmitter Functions

The transmitter consists of a differential receiver, a squelch circuit and a differential twisted-pair cable driver with pre-distortion. When data is being transmitted, and there is no collision or link integrity failure, the transmitted data is looped back to the receiver output ports RX+ and RX-.

The common mode voltage of the differential input buffer is set internally with a differential input resistance of typically 40 kΩ.

The transmitter squelch circuit prevents false triggering of the transmitter from noise on the AUI cable. The transmitter will be activated if the differential signal at the TX± pins exceeds typically ±200mV and has a high-low sequence with both the positive and negative pulse widths exceeding 50ns. The third bit of the Manchester data is always transmitted. The transmitter is de-activated by a continuous high of between 150ns and 200ns.

Pre-distortion of the transmitted waveform is included to reduce the bit dependent jitter at the end of a twisted-pair cable caused by it's inherent low pass characteristics. The pre-distortion is achieved by using two pairs of differential twisted-pair drivers. One pair of drivers produces a signal delayed by 50ns compared to the other. By combining the four driver outputs through an external resistor network, the signal on the twisted-pair is pre-emphasized for the first 50ns following a voltage transition. The pre-emphasis can be changed by selection of different external resistance values.

Collision Functions

The collision circuitry consists of logic for detecting simultaneous transmission and reception, a heartbeat generator, a 10MHz signal source and a differential line driver.

The collision detection scheme implemented in the NE86C92 is transmit mode detection which detects a collision if both the transmitter and receiver are active at the same time. A collision condition is indicated to the Manchester encoder/decoder by a 10MHz signal at the CD outputs of the differential line driver and occurs within 900ns of the onset of a collision. The collision signal begins with a negative going pulse and ends with a continuous high-to-idle state of typically 450ns.

When a collision occurs the internal loopback is disabled and the signal received at the RXI inputs is passed to the RX outputs. At the end of a collision the loopback is enabled again.

At the end of every transmission the heartbeat generator creates a pseudo collision to ensure that the collision circuitry is properly functioning. The pseudo collision consists of a 1µs burst of 10MHz signal at the CD outputs approximately 1us after the end of the transmission. The heartbeat function can be disabled externally by connecting the HBE (heartbeat enable) to GND. This allows the NE86C92 to be used in hub or repeater applications.

As with the receiver outputs the collision outputs CD+ and CD- are pulled low in the idle state and maintain < 40mV offset to minimize DC standing current in the transformer.

Jabber Functions

The jabber timer monitors the transmitter and inhibits transmission if it is active for longer than typically 50ms. The jabber circuit then enables the collision outputs for the remainder of the data frame and for typically 450ms (unjab time) after it has ended. At this point the transmitter becomes uninhibited.

Link Integrity Functions

This circuit monitors the integrity of the twisted-pair cable connected to the RXI inputs. In the event of a fault, the transmit, loopback and receive functions of the NE86C92 are disabled and the fail status is indicated by turning off the LED connected to RLED.

The twisted-pair cable integrity is monitored by detecting periodic link-integrity pulses at the RXI inputs. These pulses are 100ns in duration, with pre-distortion, followed by a return to idle. The receiver does not recognize these as data and is not enabled by them.

When no data frames are being received the NE86C92 provides a link-integrity reception window during which a link pulse is expected to arrive. The window opens nominally 5ms after receipt of the previous link pulse or the end of a data frame and remains open for 110ms. If a link pulse is received before the window opens then it is ignored. If a link pulse arrives while it is open then the internal window timers are reset. If no link pulse is received after 110ms, then the transmit, receive and loopback functions are disabled and a link failure is indicated by turning OFF the LED connected to RLED.

The NE86C92 can only re-enable the transmit, loopback and receive functions if it receives four consecutive link pulses within the link pulse window, or if a data frame is received. In either case the NE86C92 waits until both the transmit and receive paths are idle before re-enabling the transmit, loopback and receive paths.

When the link integrity circuit is enabled ($\overline{LI}$ connected to GND) a link integrity pulse is transmitted onto the twisted-pair cable typically once every 16ms irrespective of whether the transmitter is jabbed or there is a link integrity failure.

If the link integrity circuit is disabled ($\overline{LI}$ connected to V_{DD}) no link pulses are transmitted, the received link pulses are ignored and the RLED indicator remains ON in the absence of receive traffic.

Crystal Controlled Oscillator

Clock signals for the 50ns pre-distortion delay for transmitted data, the 10MHz collision signal and all on-chip timing functions are produced by a 20MHz crystal controlled oscillator.

An external MOS-level or TTL clock can also be applied directly to the XTAL1 input. In the case XTAL2 provides a buffered output of the signal applied to XTAL1; and may be left disconnected, used to drive other devices, or connected ground.

Any commercially available parallel resonant crystal may be used, but it is recommended that the total capacitance on each of the XTAL pins should be kept below 20pF.

LED Status Functions

The NE86C92 provides output drivers for five LED status indicators.

The LED connected to XLED indicates transmit status; (see Figure 8)

- The LED is ON when no transmission is in progress.
- The LED turns OFF when a data frame is transmitted and remains OFF for typically 115ms.
- The LED then turns back ON for a minimum of typically 6.4ms until turned OFF by the next transmission.

The LED connected to RLED indicates receive status and behaves differently depending on whether the link integrity circuit is disabled or enabled.

When the link integrity circuit is disabled; (see Figure 10)

- The LED is ON when no reception is in progress.
- The LED turns OFF when a data frame is received and remains OFF for typically 115ms.
- The LED then turns back ON for a minimum of typically 6.4ms until turned OFF by the next reception.

When the link integrity circuit is enabled the LED behavior is the same as above except that; (see Figure 11)

- The LED is ON when both no reception is in progress and link integrity pulses are being successfully received.
- The LED turns OFF in the event of a link failure
- The LED turns back ON for nominally 1sec when the the link is re-established.

The LED connected to CLED indicates collision status; (see Figure 9)

- The LED is OFF for no collision.
- The LED turns ON for nominally 12ms in the event of a collision.
- The LED remains ON if a further collisions occur during this time and remains ON for the nominal on-time following the last transition.
- There is no minimum OFF time. The LED will turn ON immediately another collision is detected.

The LED connected to JLED indicates jabber status; (see Figure 7)

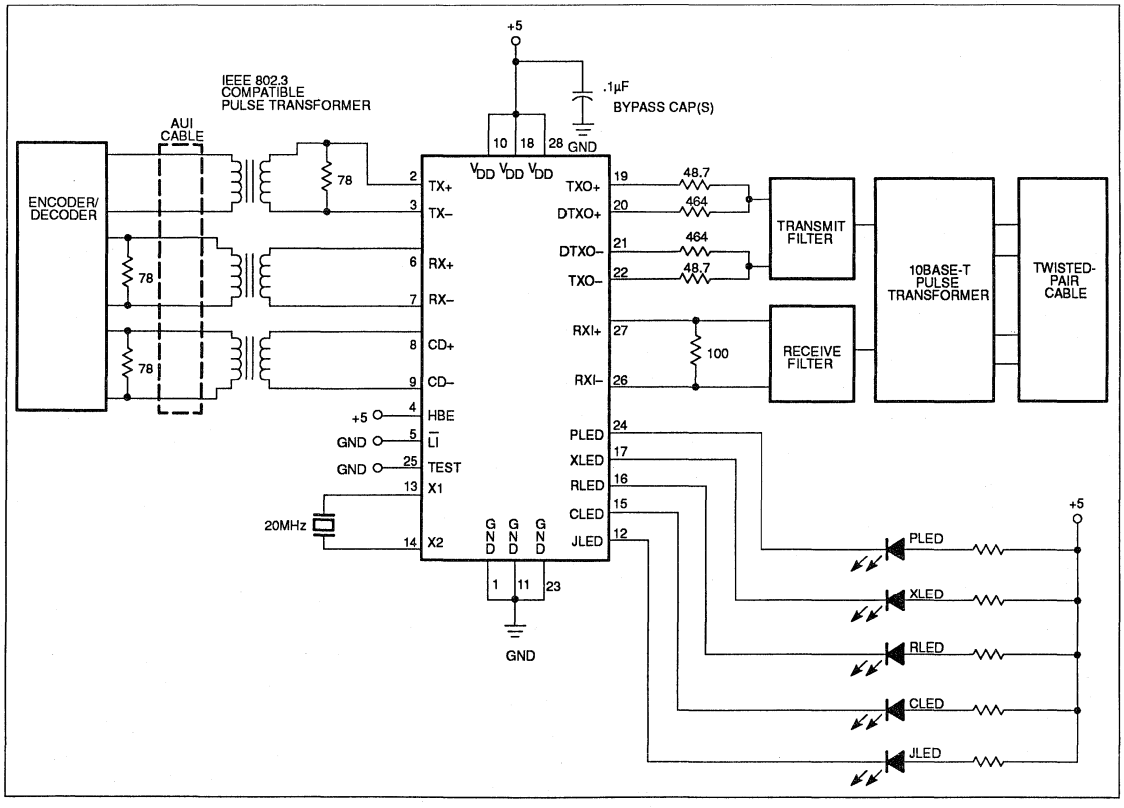
- The LED is OFF for a no-jab condition.
- The LED turns ON when the twisted-pair drivers are jabbed.
- The LED turns back OFF when the twisted-pair drivers are unjabbed.

The LED connected to PLED (when used) indicates polarity reversal status;

- The LED is ON when there is no polarity reversal of the twisted-pair receive wires.
- The LED is OFF when the polarity is reversed.
- The LED flashes during link-fail before polarity has been determined.

The LED drivers require an external resistor in series with the LED (see connection diagram) to limit the LED current.

TYPICAL APPLICATION DIAGRAM



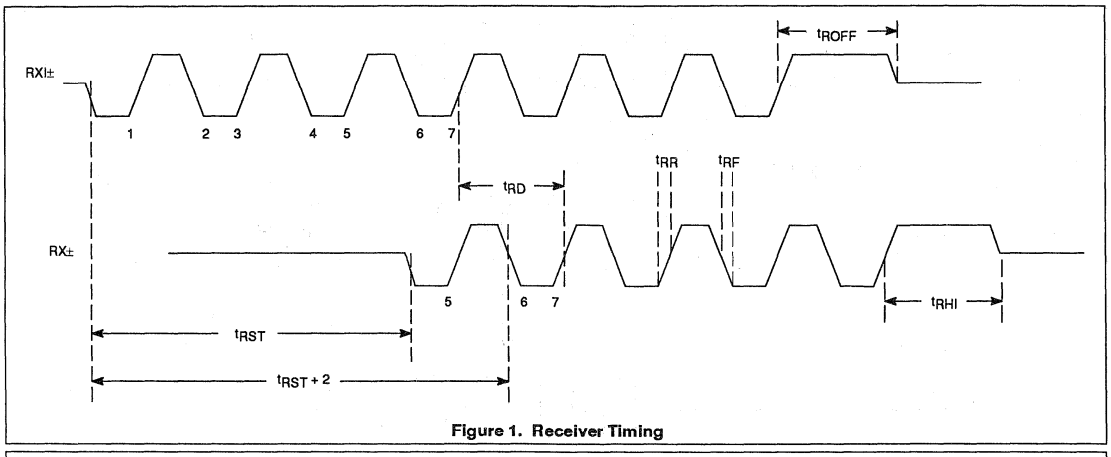


Figure 1. Receiver Timing

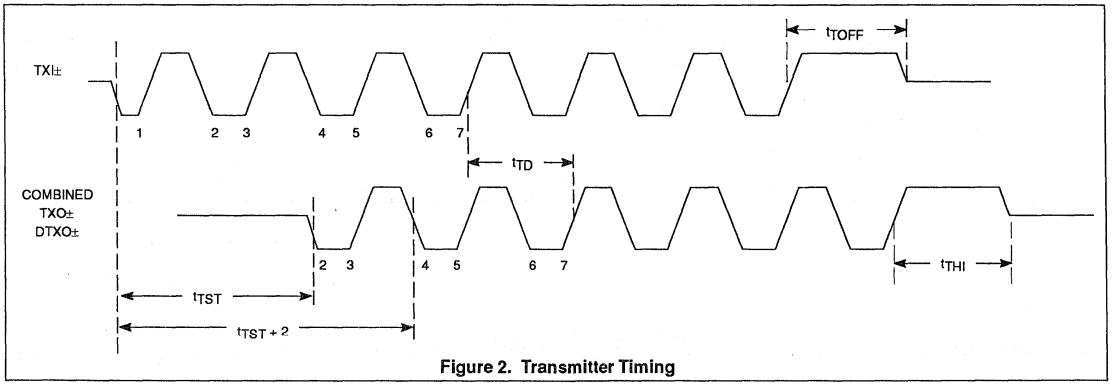


Figure 2. Transmitter Timing

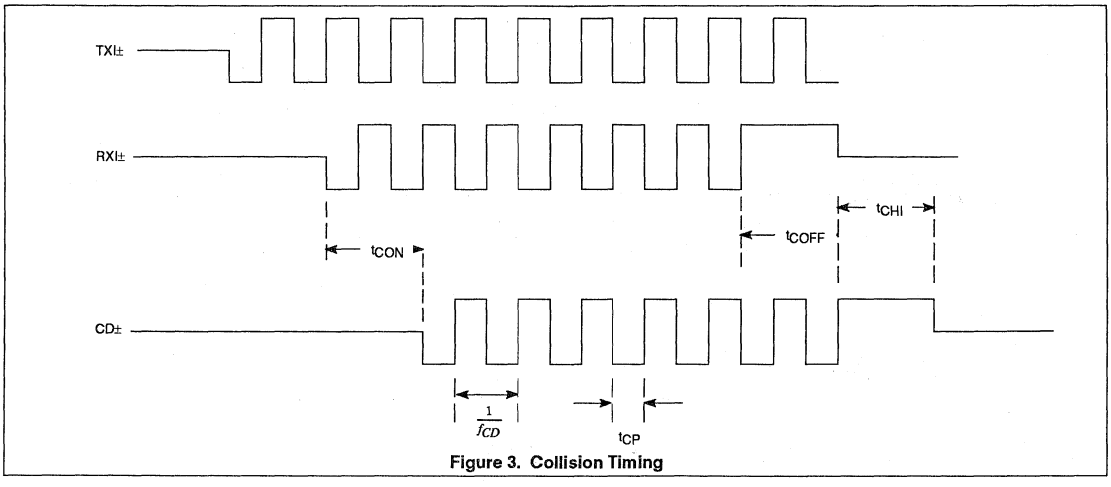


Figure 3. Collision Timing

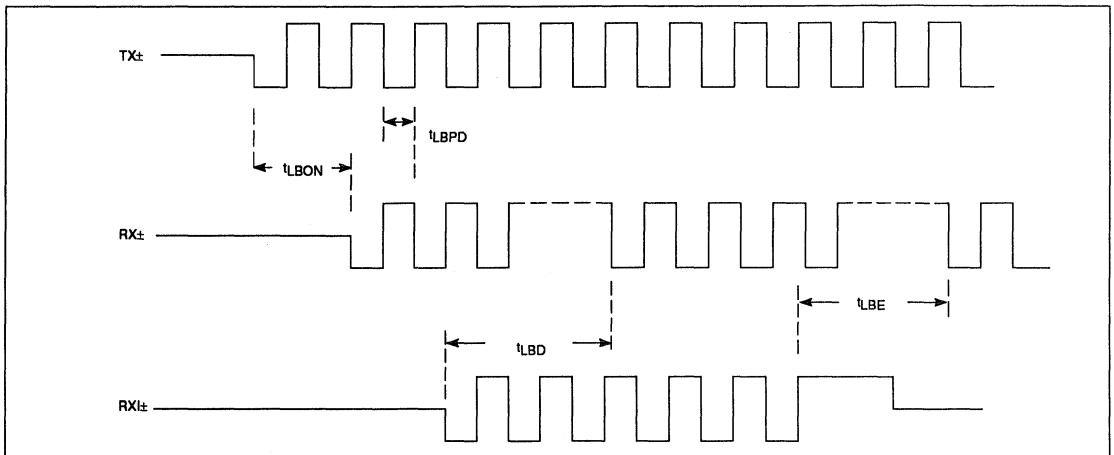


Figure 4. Loopback Timing

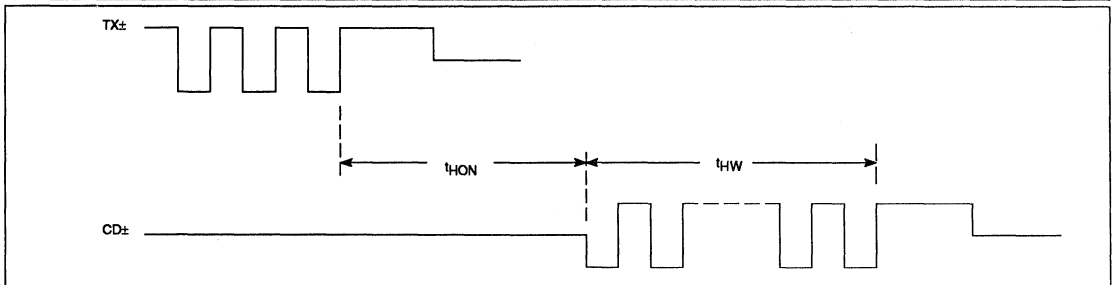


Figure 5. Heartbeat Timing

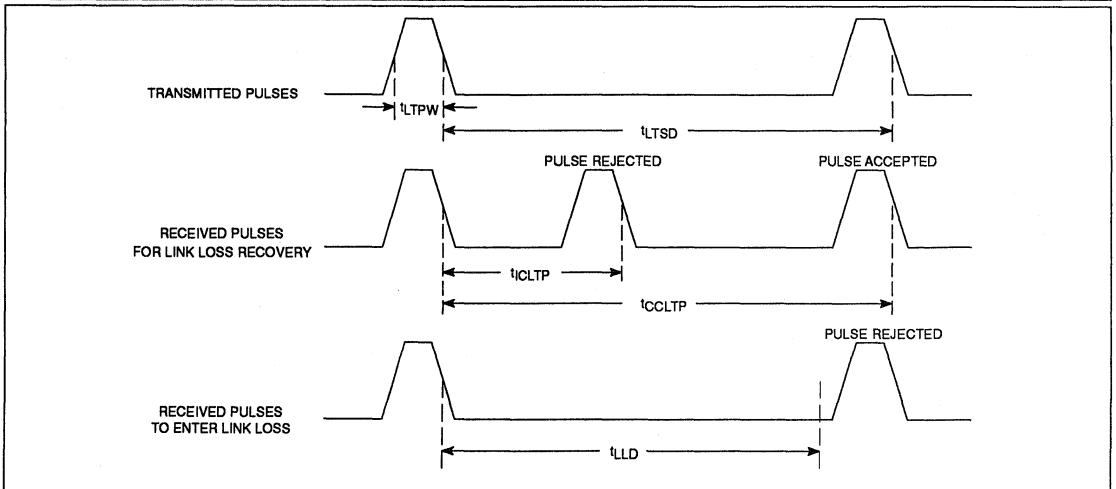


Figure 6. Link Test Timing

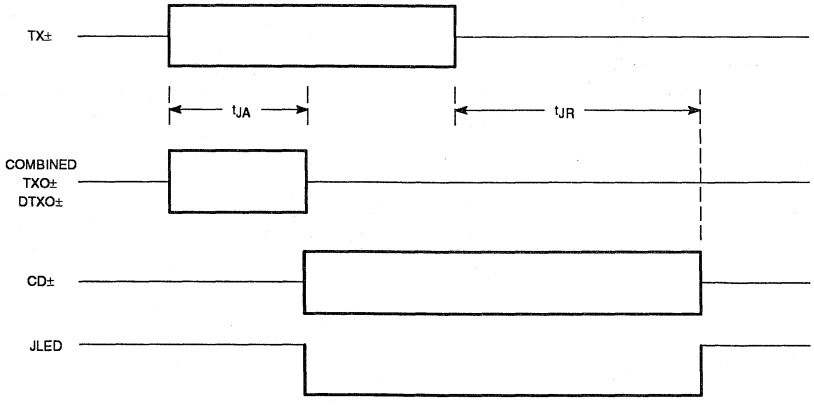


Figure 7. Jabber Timing

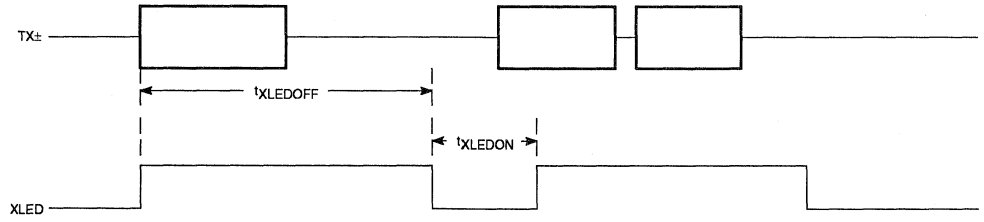


Figure 8. XLED Timing

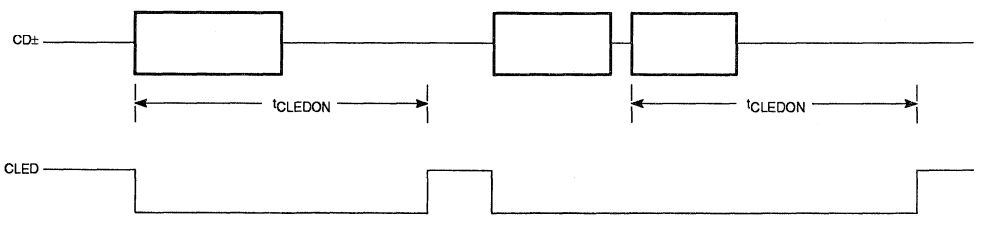


Figure 9. CLED Timing

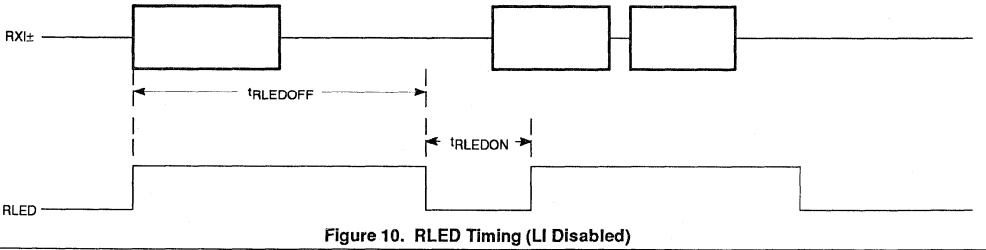


Figure 10. RLED Timing (LI Disabled)

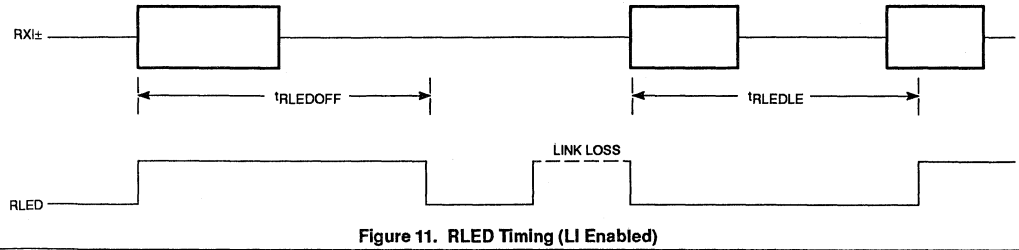


Figure 11. RLED Timing (LI Enabled)

Section 4
Fibre Optic Products
Data Sheets

INDEX

Transimpedance amplifier (280MHz) NE5210

DESCRIPTION

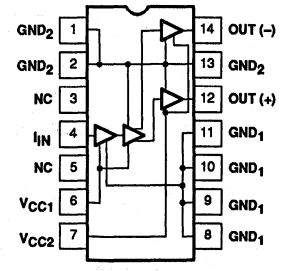
The NE5210 is a 7kΩ transimpedance wide band, low noise amplifier with differential outputs, particularly suitable for signal recovery in fiber-optic receivers. The part is ideally suited for many other RF applications as a general purpose gain block.

FEATURES

- Low noise: 3.5pA/√Hz
- Single 5V supply
- Large bandwidth: 280MHz
- Differential outputs
- Low input/output impedances
- High power supply rejection ratio
- High overload threshold current
- Wide dynamic range
- 7kΩ differential transresistance

PIN CONFIGURATION

D Package



TOP VIEW

APPLICATIONS

- Fiber-optic receivers, analog and digital
- Current-to-voltage converters
- Wideband gain block
- Medical and scientific instrumentation
- Sensor preamplifiers
- Single-ended to differential conversion
- Low noise RF amplifiers
- RF signal processing

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +70°C	NE5210D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply	6	V
T_A	Operating ambient temperature range	0 to +70	°C
T_J	Operating junction temperature range	-55 to +150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
P_{DMAX}	Power dissipation T_A=25°C (still air)[1]	1.0	W
I_{INMAX}	Maximum input current[2]	5	mA

NOTES:

1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance: θ_{JA}=125°C/W.
2. The use of a pull-up resistor to V_{CC} for the PIN diode, is recommended.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	4.5 to 5.5	V
T_A	Ambient temperature range	0 to +70	°C
T_J	Junction temperature range	0 to +90	°C

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over operating temperature range at V_{CC}=5V, unless otherwise specified. Typical data applies at V_{CC}=5V and T_A=25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IN}	Input bias voltage		0.6	0.8	0.95	V
$V_{O\pm}$	Output bias voltage		2.8	3.3	3.7	V
V_{OS}	Output offset voltage			0	80	mV
I_{CC}	Supply current		21	26	32	mA
I_{OMAX}	Output sink/source current[1]		3	4		mA
I_{IN}	Input current (2% linearity)	Test Circuit 8, Procedure 2	±120	±160		µA
I_{INMAX}	Maximum input current overload threshold	Test Circuit 8, Procedure 4	±160	±240		µA

NOTES:
1. Test condition: output quiescent voltage variation is less than 100mV for 3mA load current.

AC ELECTRICAL CHARACTERISTICS

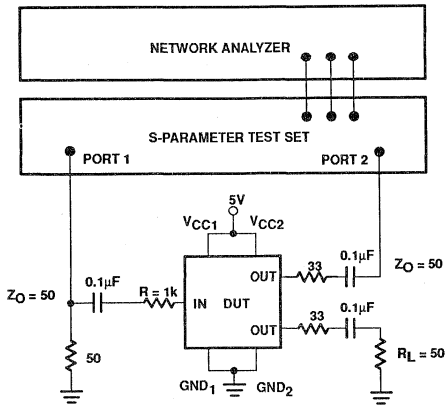
Typical data and Min/Max limits apply at V_{CC}=5V and T_A=25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
R_T	Transresistance (differential output)	DC tested, R_L=∞ Test Circuit 8, Procedure 1	4.9	7	10	kΩ
R_O	Output resistance (differential output)	DC tested	16	30	42	Ω
R_T	Transresistance (single-ended output)	DC tested, R_L=∞	2.45	3.5	5	kΩ
R_O	Output resistance (single-ended output)	DC tested	8	15	21	Ω
f_{3dB}	Bandwidth (-3dB)	Test Circuit 1, T_A=25°C	200	280		MHz
R_{IN}	Input resistance			60		Ω
C_{IN}	Input capacitance			7.5		pF
ΔR/ΔV	Transresistance power supply sensitivity	V_{CC}=5±0.5V		9.6	20	%/V
ΔR/ΔT	Transresistance ambient temperature sensitivity	$\Delta T_A = T_{A\,MAX} - T_{A\,MIN}$		0.05	0.1	%/°C
I_N	RMS noise current spectral density (referred to input)	f=10MHz, T_A=25°C Test Circuit 2		3.5	6	pA/√Hz
I_T	Integrated RMS noise current over the bandwidth (referred to input) C_S=0[1]	T_A=25°C Test Circuit 2				
		Δf=100MHz		37		nA
		Δf=200MHz		56		nA
		Δf=300MHz		71		nA
	C_S=1pF	Δf=100MHz		40		nA
		Δf=200MHz		66		nA
		Δf=300MHz		89		nA
PSRR	Power supply rejection ratio[2] (V_{CC1}=V_{CC2})	DC tested, ΔV_{CC}=0.1V Equivalent AC test circuit 3	20	36		dB
PSRR	Power supply rejection ratio[2] (V_{CC1})	DC tested, ΔV_{CC}=0.1V Equivalent AC test circuit 4	20	36		dB
PSRR	Power supply rejection ratio[2] (V_{CC2})	DC tested, ΔV_{CC}=0.1V Equivalent AC test circuit 5		65		dB
PSRR	Power supply rejection ratio[2] (ECL configuration)	f=0.1MHz, Test Circuit 6		23		dB
V_{OMAX}	Maximum output voltage swing differential	R_L=∞ Test Circuit 8, Procedure 3	2.4	3.2		V_{P-P}
V_{INMAX}	Maximum input amplitude for output duty cycle of 50±5%[3]	Test Circuit 7	650			mV_{P-P}
t_R	Rise time for 50 mV_{P-P} output signal[4]	Test Circuit 7		0.8	1.2	ns

NOTES:

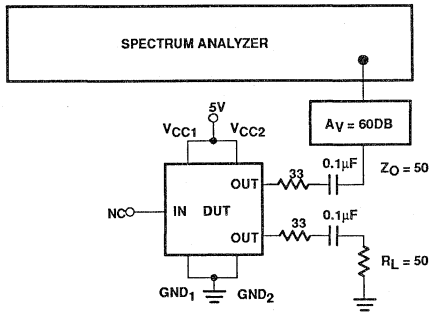
1. Package parasitic capacitance amounts to about 0.2pF
2. PSRR is output referenced and is circuit board layout dependent at higher frequencies. For best performance use RF filter in V_{CC} line.
3. Guaranteed by linearity and overload tests.
4. t_R defined as 20-80% rise time. It is guaranteed by a -3dB bandwidth test.

TEST CIRCUITS



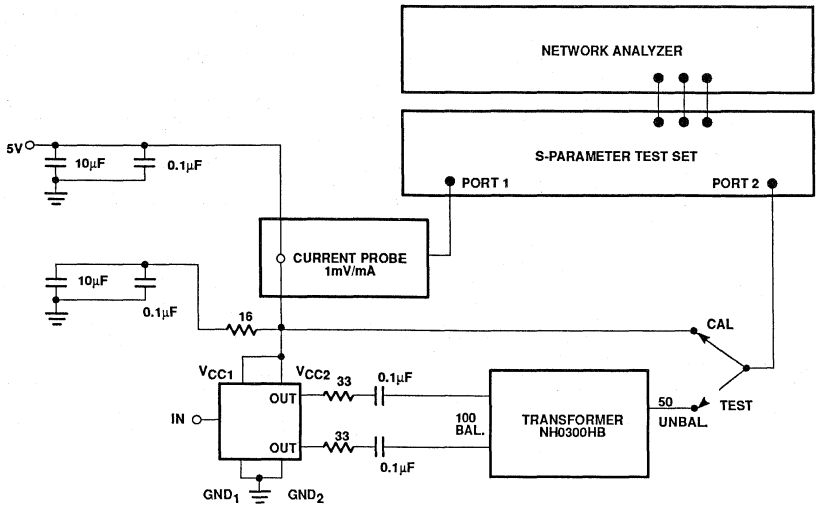
SINGLE-ENDED	DIFFERENTIAL
$R_T \approx \frac{V_{OUT}}{V_{IN}} R = 2 \cdot S21 \cdot R$	$R_T = \frac{V_{OUT}}{V_{IN}} R = 4 \cdot S21 \cdot R$
$R_O \approx Z_O \left\lvert \frac{1 + S22}{1 - S22} \right\rvert - 33$	$R_O = 2Z_O \left\lvert \frac{1 + S22}{1 - S22} \right\rvert - 66$

Test Circuit 1

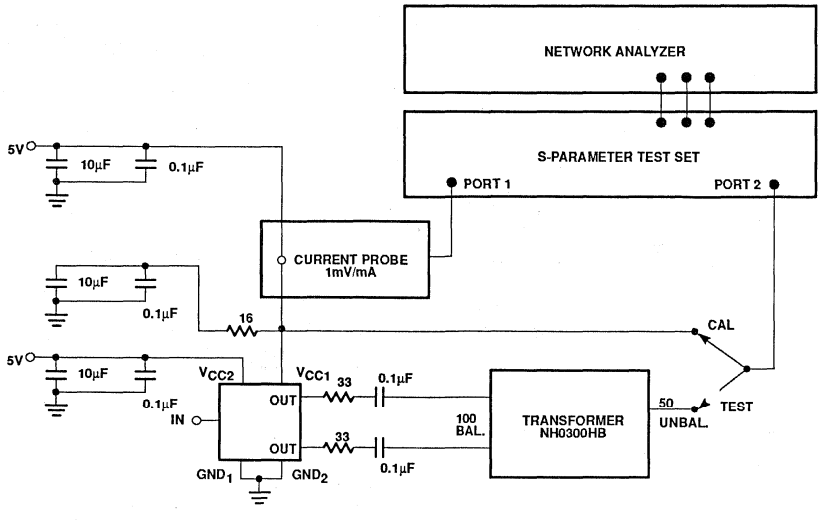


Test Circuit 2

TEST CIRCUITS (Continued)

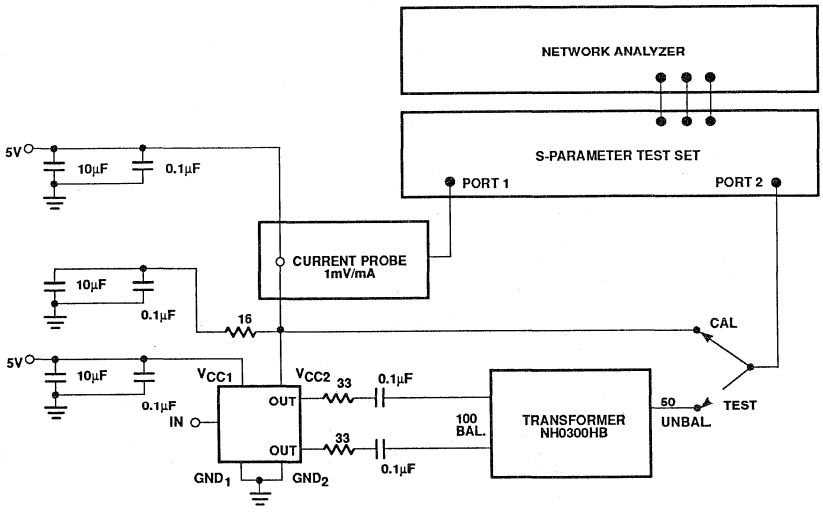


Test Circuit 3

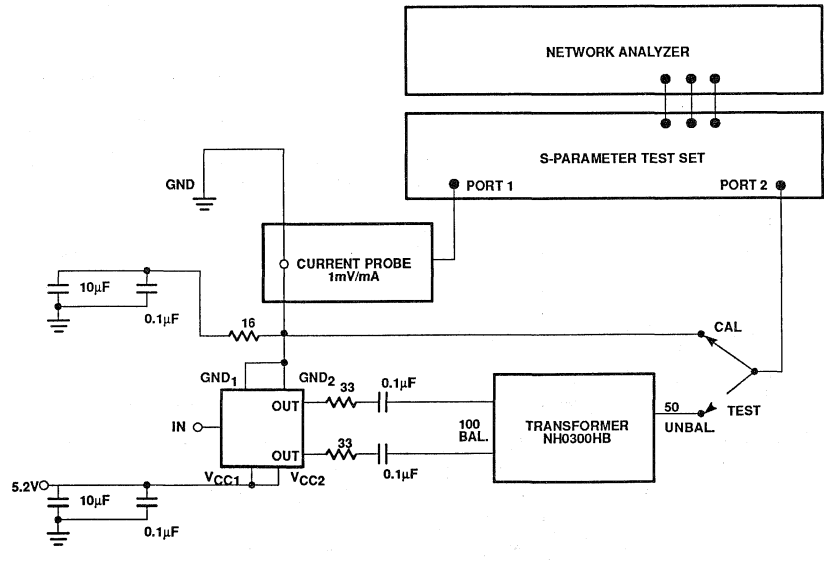


Test Circuit 4

TEST CIRCUITS (Continued)

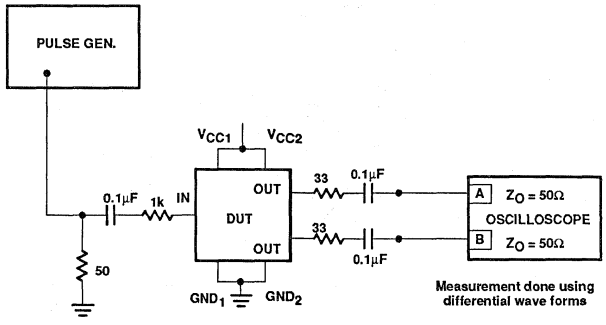


Test Circuit 5



Test Circuit 6

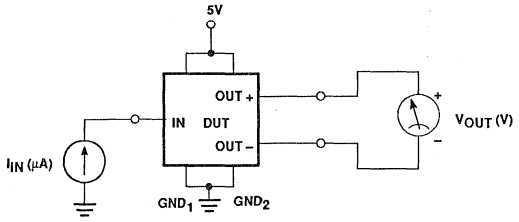
TEST CIRCUITS (Continued)

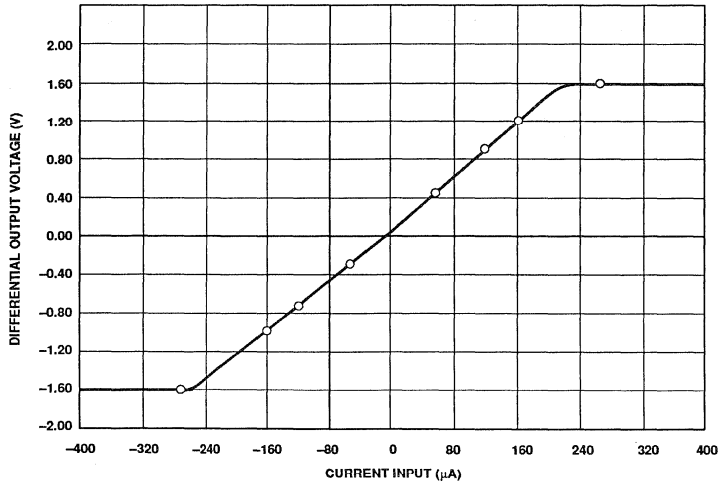


Test Circuit 7

TEST CIRCUITS (Continued)

Typical Differential Output Voltage vs Current Input





NE5210 TEST CONDITIONS

Procedure 1

R_T measured at 60μA
$R_T = (V_{O1} - V_{O2})/(+60\mu A - (-60\mu A))$
Where: V_{O1} Measured at $I_{IN} = +60\mu A$
V_{O2} Measured at $I_{IN} = -60\mu A$

Procedure 2

Linearity = 1 – ABS(($V_{OA} - V_{OB}$) / ($V_{O3} - V_{O4}$))
Where: V_{O3} Measured at $I_{IN} = +120\mu A$
V_{O4} Measured at $I_{IN} = -120\mu A$
$V_{OA} = R_T \cdot (+120\mu A) + V_{OB}$
$V_{OB} = R_T \cdot (-120\mu A) + V_{OB}$

Procedure 3

$V_{OMAX} = V_{O7} - V_{O8}$
Where: V_{O7} Measured at $I_{IN} = +260\mu A$
V_{O8} Measured at $I_{IN} = -260\mu A$

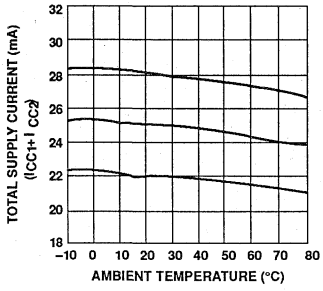
Procedure 4

I_{IN} Test Pass Conditions:
$V_{O7} - V_{O5} > 20mV$ and $V_{O6} - V_{O5} > 20mV$
Where: V_{O5} Measured at $I_{IN} = +160\mu A$
V_{O6} Measured at $I_{IN} = -160\mu A$
V_{O7} Measured at $I_{IN} = +260\mu A$
V_{O8} Measured at $I_{IN} = -260\mu A$

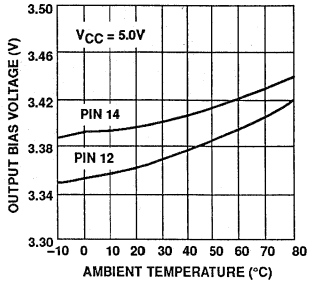
Test Circuit 8

TYPICAL PERFORMANCE CHARACTERISTICS

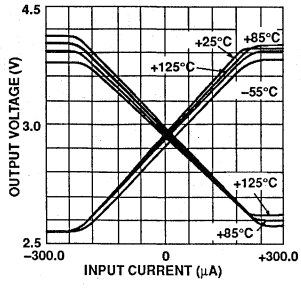
NE5210 Supply Current vs Temperature



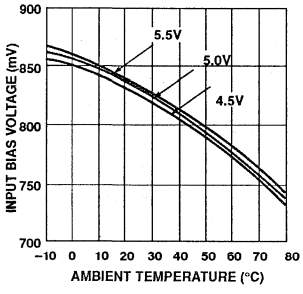
NE5210 Output Bias Voltage vs Temperature



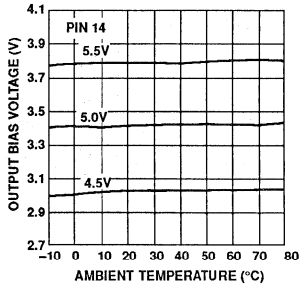
Output Voltage vs Input Current



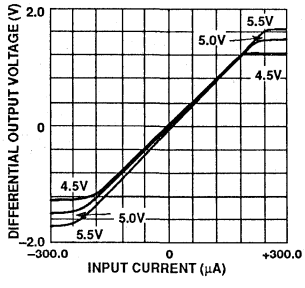
NE5210 Input Bias Voltage vs Temperature



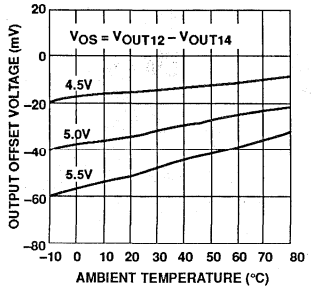
NE5210 Output Bias Voltage vs Temperature



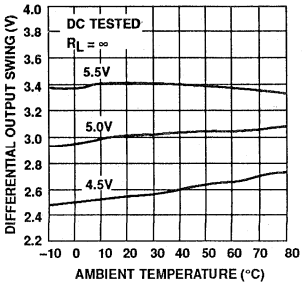
Differential Output Voltage vs Input Current



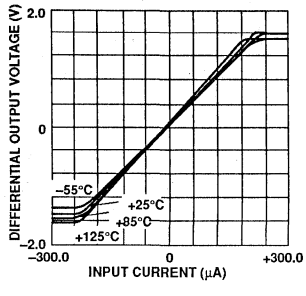
NE5210 Output Offset Voltage vs Temperature



NE5210 Differential Output Swing vs Temperature

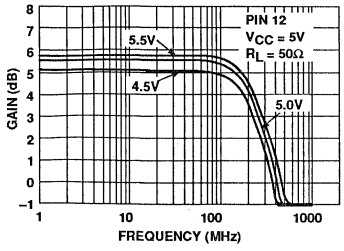


Differential Output Voltage vs Input Current

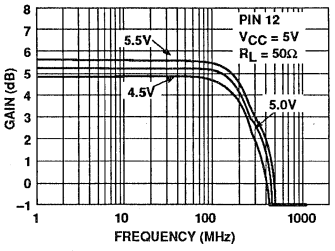


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

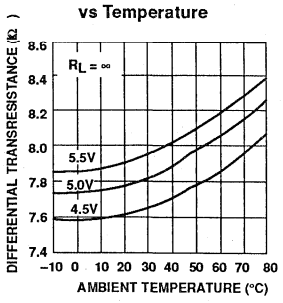
Gain vs Frequency



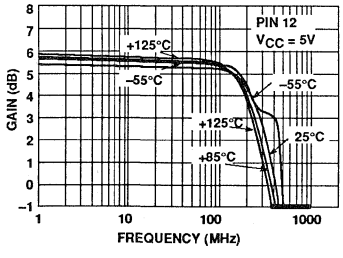
Gain vs Frequency



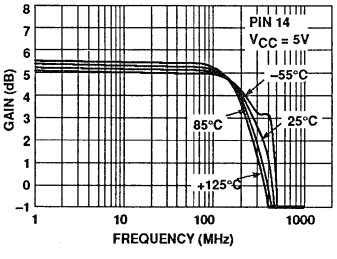
NE5210 Differential Transresistance vs Temperature



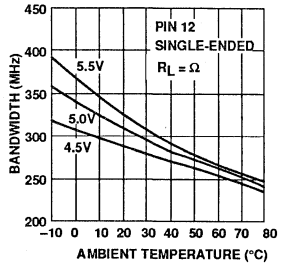
Gain vs Frequency



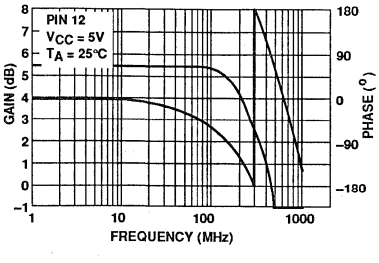
Gain vs Frequency



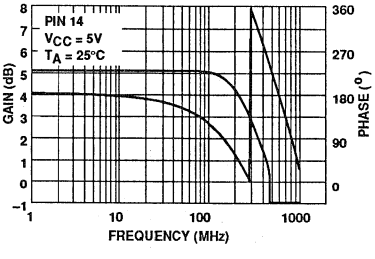
NE5210 Bandwidth vs Temperature



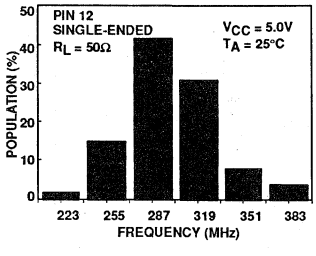
Gain and Phase Shift vs Frequency



Gain and Phase Shift vs Frequency

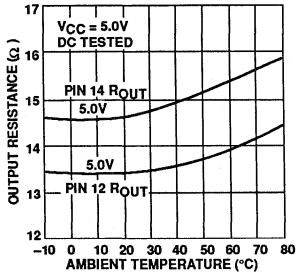


NE5210 Typical Bandwidth Distribution (70 Parts from 4 Wafer Lots)

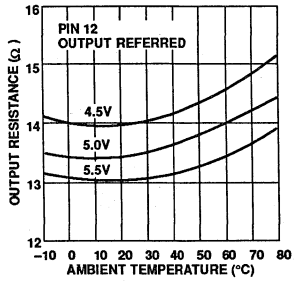


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

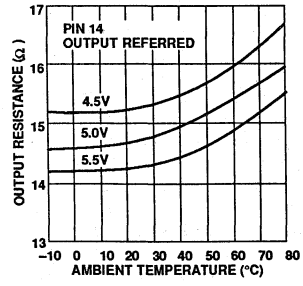
NE5210 Output Resistance vs Temperature



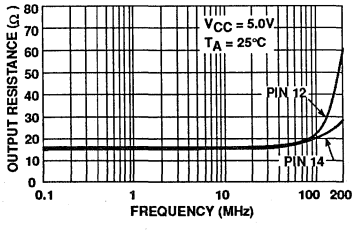
NE5210 Output Resistance vs Temperature



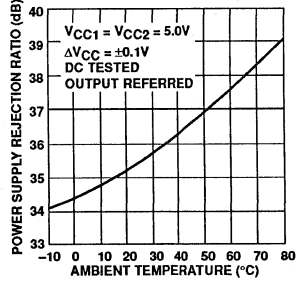
NE5210 Output Resistance vs Temperature



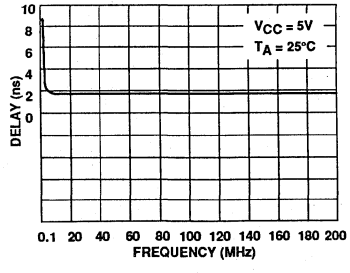
Output Resistance vs Frequency



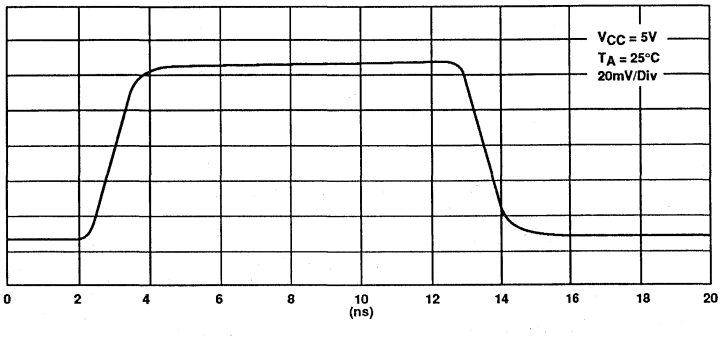
NE5210 Power Supply Rejection Ratio vs Temperature



Group Delay



Output Step Response



THEORY OF OPERATION

Transimpedance amplifiers have been widely used as the preamplifier in fiber-optic receivers. The NE5210 is a wide bandwidth (typically 280MHz) transimpedance amplifier designed primarily for input currents requiring a large dynamic range, such as those produced by a laser diode. The maximum input current before output stage clipping occurs at typically 240μA. The NE5210 is a bipolar transimpedance amplifier which is current driven at the input and generates a differential voltage signal at the outputs. The forward transfer function is therefore a ratio of the differential output voltage to a given input current with the dimensions of ohms. The main feature of this amplifier is a wideband, low-noise input stage which is desensitized to photodiode capacitance variations. When connected to a photodiode of a few picoFarads, the frequency response will not be degraded significantly. Except for the input stage, the entire signal path is differential to provide improved power-supply rejection and ease of interface to ECL type circuitry. A block diagram of the circuit is shown in Figure 1. The input stage (A1) employs shunt-series feedback to stabilize the current gain of the amplifier. The transresistance of the amplifier from the current source to the emitter of Q_3 is approximately the value of the feedback resistor, R_F=3.6kΩ. The gain from the second stage (A2) and emitter followers (A3 and A4) is about two. Therefore, the differential transresistance of the entire amplifier, R_T is

$$R_T = \frac{V_{OUT(diff)}}{I_{IN}} = 2R_F = 2(3.6K) = 7.2k\Omega$$

The single-ended transresistance of the amplifier is typically 3.6kΩ.

The simplified schematic in Figure 2 shows how an input current is converted to a differential output voltage. The amplifier has a single input for current which is referenced to Ground 1. An input current from a laser diode, for example, will be converted into a voltage by the feedback resistor R_F. The transistor Q1 provides most of the open loop gain of the circuit, A_{VOL}≈70. The emitter follower Q_2 minimizes loading on Q_1. The transistor Q_4, resistor R_7, and V_{B1} provide level shifting and interface with the Q_{15} – Q_{16} differential pair of the second stage which is biased with an internal reference, V_{B2}. The differential outputs are derived from emitter followers Q_{11} – Q_{12} which are biased by constant current sources. The collectors of Q_{11} – Q_{12} are bonded to an external pin, V_{CC2}, in order to reduce the feedback to the input stage. The output impedance is about 17Ω single-ended. For ease of performance evaluation, a 33Ω resistor is used in series with each output to match to a 50Ω test system.

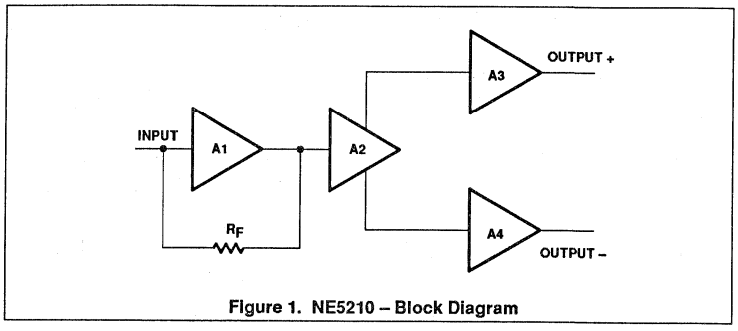


Figure 1. NE5210 – Block Diagram

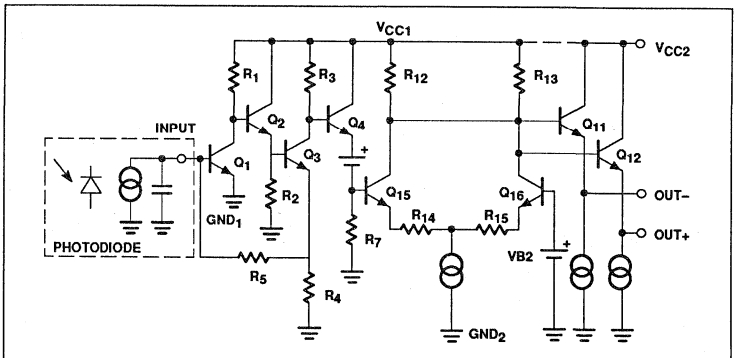


Figure 2. Transimpedance Amplifier

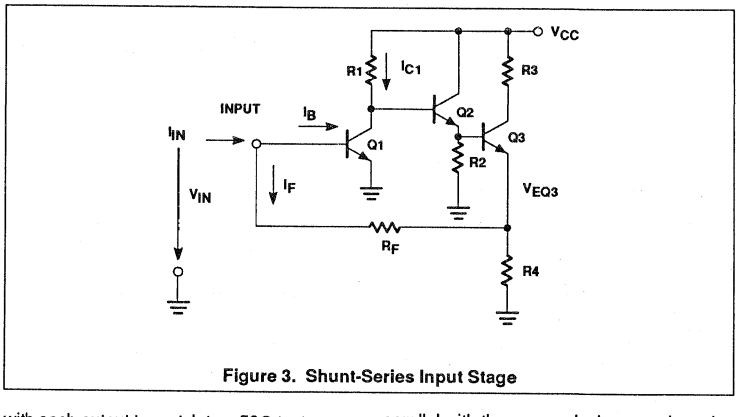


Figure 3. Shunt-Series Input Stage

BANDWIDTH CALCULATIONS

The input stage, shown in Figure 3, employs shunt-series feedback to stabilize the current gain of the amplifier. A simplified analysis can determine the performance of the amplifier. The equivalent input capacitance, C_{IN}, in parallel with the source, I_S, is approximately 7.5pF, assuming that C_S=0 where C_S is the external source capacitance.

Since the input is driven by a current source the input must have a low input resistance. The input resistance, R_{IN}, is the ratio of the incremental input voltage, V_{IN}, to the corresponding input current, I_{IN} and can be calculated as:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{R_F}{1 + A_{VOL}} = \frac{3.6K}{71} = 51\Omega$$

More exact calculations would yield a higher value of 60Ω.

Thus C_{IN} and R_{IN} will form the dominant pole of the entire amplifier;

$$f_{-3dB} = \frac{1}{2\pi\ R_{IN}\ C_{IN}}$$

Assuming typical values for R_F = 3.6kΩ, R_{IN} = 60Ω, C_{IN} = 7.5pF

$$f_{-3dB} = \frac{1}{2\pi\ 7.5pF\ 60} = 354MHz$$

The operating point of Q1, Figure 2, has been optimized for the lowest current noise without introducing a second dominant pole in the pass-band. All poles associated with subsequent stages have been kept at sufficiently high enough frequencies to yield an overall single pole response. Although wider bandwidths have been achieved by using a cascode input stage configuration, the present solution has the advantage of a very uniform, highly desensitized frequency response because the Miller effect dominates over the external photodiode and stray capacitances. For example, assuming a source capacitance of 1pF, input stage voltage gain of 70, R_{IN} = 60Ω then the total input capacitance, C_{IN} = (1+7.5) pF which will lead to only a 12% bandwidth reduction.

NOISE

Most of the currently installed fiber-optic systems use non-coherent transmission and detect incident optical power. Therefore, receiver noise performance becomes very important. The input stage achieves a low input referred noise current (spectral density) of 3.5pA/√Hz. The transresistance configuration assures that the external high value bias resistors often required for photodiode biasing will not contribute to the total noise system noise. The equivalent input $_{RMS}$ noise current is strongly determined by the quiescent current of Q_1, the feedback resistor R_F, and the bandwidth; however, it is not dependent upon the internal Miller-capacitance. The measured wideband noise was 66nA$_{RMS}$ in a 200MHz bandwidth.

DYNAMIC RANGE CALCULATIONS

The electrical dynamic range can be defined as the ratio of maximum input current to the peak noise current:

Electrical dynamic range, D_E, in a 200MHz bandwidth assuming I_{INMAX} = 240μA and a wideband noise of I_{EQ}=66nA$_{RMS}$ for an external source capacitance of C_S = 1pF.

$$D_E = 20log\ \frac{(Max.\ input\ current)\ (PK)}{(Peak\ noise\ current)\ (RMS)\cdot\sqrt{2}}$$

$$= 20\log\frac{(240\cdot10^{-6})}{(\sqrt{2}\ \ 66\ \ 10^{-9})} = 68dB$$

In order to calculate the optical dynamic range the incident optical power must be considered.

For a given wavelength λ; (meters)

Energy of one Photon = $\frac{hc}{\lambda}$ watt sec (Joule)

Where h=Planck's Constant = 6.6×10^{-34} Joule sec.

c = speed of light = 3×10^8 m/sec

c / λ = optical frequency (Hz)

No. of incident photons/sec= where P=optical incident power

No. of incident photons/sec = $\frac{\frac{P}{hs}}{\lambda}$

where P = optical incident power

No. of generated electrons/sec = $\eta \cdot \frac{\frac{P}{hs}}{\lambda}$

where η = quantum efficiency

$$= \frac{no.\ of\ generated\ electron\ hole\ paris}{no.\ of\ incident\ photons}$$

$$\therefore I = \eta \cdot \frac{\frac{P}{hs}}{\lambda} \cdot e\ Amps\ (Coulombs/sec.)$$

where e = electron charge = 1.6×10^{-19} Coulombs

Responsivity R = $\frac{\frac{\eta \cdot e}{hs}}{\lambda}$ Amp/watt

$$I = P \cdot R$$

Assuming a data rate of 400 Mbaud (Bandwidth, B=200MHz), the noise parameter Z may be calculated as:[1]

$$Z = \frac{I_{EQ}}{qB} = \frac{66\cdot10^{-9}}{(1.6\cdot10^{-19})(200\cdot10^{6})} = 2063$$

where Z is the ratio of $_{RMS}$ noise output to the peak response to a single hole-electron pair. Assuming 100% photodetector quantum efficiency, half mark/half space digital transmission, 850nm lightwave and using Gaussian approximation, the minimum required optical power to achieve 10^{-9} BER is:

$$P_{avMIN} = 12\frac{hc}{\lambda}B\ Z = 12\ 2.3\cdot10^{-19}\ \ 200\cdot10^{6}\ 2063$$

$$= 1139nW = -29.4dBm$$

where h is Planck's Constant, c is the speed of light, λ is the wavelength. The minimum input current to the NE5210, at this input power is:

$$I_{avMIN} = qP_{avMIN}\frac{\lambda}{hc}$$

$$= \frac{1139\cdot10^{-9}\cdot1.6\cdot10^{-19}}{2.3\cdot10^{-19}}$$

$$= 792nA$$

Choosing the maximum peak overload current of I_{avMAX}=240μA, the maximum mean optical power is:

$$P_{avMAX} = \frac{hcI_{avMAX}}{\lambda q} = \frac{2.3\cdot10^{-19}}{1.6\cdot10^{-19}}240\cdot10^{-6}$$

Thus the optical dynamic range, D_O is:

$D_O = P_{avMAX} - P_{avMIN}$ = -4.6 -(-29.4) = 24.8dB.

This represents the maximum limit attainable with the NE5210 operating at 200MHz bandwidth, with a half mark/half space digital transmission at 850nm wavelength.

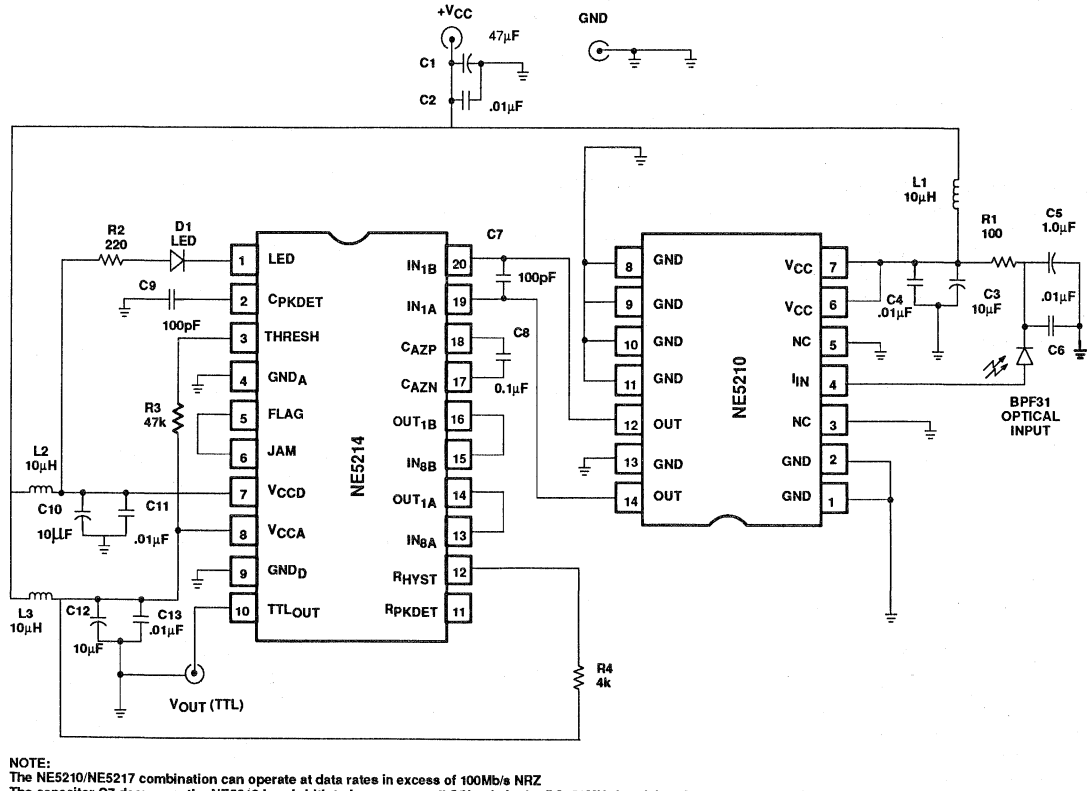
APPLICATION INFORMATION

Package parasitics, particularly ground lead inductances and parasitic capacitances, can significantly degrade the frequency response. Since the NE5210 has differential outputs which can feed back signals to the input by parasitic package or board layout capacitances, both peaking and attenuating type frequency response shaping is possible. Constructing the board layout so that Ground 1 and Ground 2 have very low impedance paths has produced the best results. This was accomplished by adding a ground-plane stripe underneath the device connecting Ground 1, Pins 8–11, and Ground 2, Pins 1 and 2 on opposite ends of the SO14 package. This ground-plane stripe also provides isolation between the output return currents flowing to either V_{CC2} or Ground 2 and the input photodiode currents to flowing to Ground 1. Without this ground-plane stripe and with large lead inductances on the board, the part may be unstable and oscillate near 800MHz. The easiest way to realize that the part is not functioning normally is to measure the DC voltages at the outputs. If they are not close to their quiescent values of 3.3V (for a 5V supply), then the circuit may be oscillating. Input pin layout necessitates that

the photodiode be physically very close to the input and Ground 1. Connecting Pins 3 and 5 to Ground 1 will tend to shield the input but it will also tend to increase the capacitance on the input and slightly reduce the bandwidth.

As with any high-frequency device, some precautions must be observed in order to enjoy reliable performance. The first of these is the use of a well-regulated power supply. The supply must be capable of providing varying amounts of current without significantly changing the voltage level. Proper supply bypassing requires that a good quality 0.1μF high-frequency capacitor be inserted between V_{CC1} and V_{CC2}, preferably a chip capacitor, as close to the package pins as possible. Also, the parallel combination of 0.1μF capacitors with 10μF tantalum capacitors from each supply, V_{CC1} and V_{CC2}, to the ground plane should provide adequate decoupling. Some applications may require an RF choke in series with the power supply line. Separate analog and digital ground leads must be maintained and printed circuit board ground plane should be employed whenever possible.

Figure 4 depicts a 50Mb/s TTL fiber-optic receiver using the BPF31, 850nm LED, the NE5210 and the NE5214 post amplifier.



NOTE:
The NE5210/NE5217 combination can operate at data rates in excess of 100Mb/s NRZ
The capacitor C7 decreases the NE5210 bandwidth to improve overall S/N ratio in the DC–50MHz band, but does create extra high frequency noise on the NE5210 V_{CC} pin(s).

Figure 4. A 50Mb/s Fiber Optic Receiver

Transimpedance amplifier (180MHz) NE/SA5211

DESCRIPTION

The NE/SA5211 is a 28kΩ transimpedance, wide-band, low noise amplifier with differential outputs, particularly suitable for signal recovery in fiber optic receivers. The part is ideally suited for many other RF applications as a general purpose gain block.

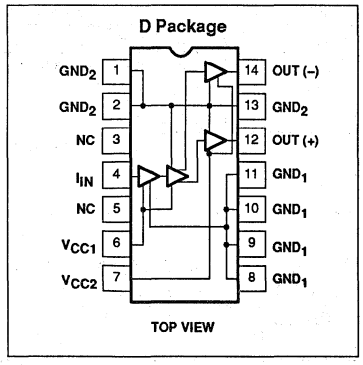
FEATURES

- Extremely low noise: $1.8pA / \sqrt{Hz}$
- Single 5V supply
- Large bandwidth: 180MHz
- Differential outputs
- Low input/output impedances
- High power supply rejection ratio
- 28kΩ differential transresistance

APPLICATIONS

- Fiber optic receivers, analog and digital
- Current-to-voltage converters
- Wide-band gain block
- Medical and scientific Instrumentation
- Sensor preamplifiers
- Single-ended to differential conversion
- Low noise RF amplifiers
- RF signal processing

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +70°C	NE5211D
14-Pin Plastic SO	-40 to +85°C	SA5211D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNIT
		NE5211	SA5211	
V_{CC}	Power supply	6	6	V
T_A	Operating ambient temperature range	0 to +70	-40 to +85	°C
T_J	Operating junction temperature range	-55 to +150	-55 to +150	°C
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C
$P_{D\,MAX}$	Power dissipation, T_A=25°C (still-air)[1]	1.0	1.0	W
$I_{IN\,MAX}$	Maximum input current[2]	5	5	mA
θ_{JA}	Thermal resistance	125	125	°C/W

NOTES:

1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance: θ_{JA}=125°C/W
2. The use of a pull-up resistor to V_{CC}, for the PIN diode is recommended.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	4.5 to 5.5	V
T_A	Ambient temperature range		
	NE Grade	0 to +70	°C
	SA Grade	-40 to +85	°C
T_J	Junction temperature range		
	NE Grade	0 to +90	°C
	SA Grade	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over operating temperature range at V_{CC}=5V, unless otherwise specified. Typical data apply at V_{CC}=5V and T_A=25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5211			SA5211			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IN}	Input bias voltage		0.6	0.8	0.95	0.55	0.8	1.00	V
$V_{O\pm}$	Output bias voltage		2.8	3.4	3.7	2.7	3.4	3.7	V
V_{OS}	Output offset voltage			0	120		0	130	mV
I_{CC}	Supply current		21	24	30	20	26	31	mA
I_{OMAX}	Output sink/source current[1]		3	4		3	4		mA
I_{IN}	Input current (2% linearity)	Test Circuit 8, Procedure 2	±30	±40		±20	±40		µA
$I_{IN\ MAX}$	Maximum input current overload threshold	Test Circuit 8, Procedure 4	±40	±60		±30	±60		µA

NOTES:
1. Test condition: output quiescent voltage variation is less than 100mV for 3mA load current.

AC ELECTRICAL CHARACTERISTICS

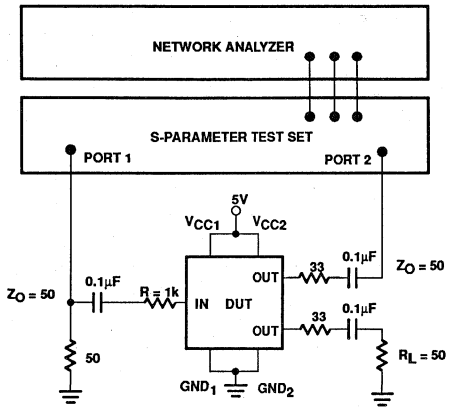
Typical data and Min and Max limits apply at V_{CC}=5V and T_A=25°C

SYMBOL	PARAMETER	TEST CONDITIONS	NE5211			SA5211			UNIT
			Min	Typ	Max	Min	Typ	Max	
R_T	Transresistance (differential output)	DC tested $R_L = \infty$ Test Circuit 8, Procedure 1	22	28	35	21	28	36	kΩ
R_O	Output resistance (differential output)	DC tested		30			30		Ω
R_T	Transresistance (single-ended output)	DC tested $R_L = \infty$	11	14	17.5	10.5	14	18.0	kΩ
R_O	Output resistance (single-ended output)	DC tested		15			15		Ω
f_{3dB}	Bandwidth (-3dB)	T_A = 25°C Test circuit 1		180			180		MHz
R_{IN}	Input resistance			200			200		Ω
C_{IN}	Input capacitance			4			4		pF
$\Delta R/\Delta V$	Transresistance power supply sensitivity	V_{CC} = 5±0.5V		3.7			3.7		%/V
$\Delta R/\Delta T$	Transresistance ambient temperature sensitivity	$\Delta T_A = T_{A\,MAX} - T_{A\,MIN}$		0.025			0.025		%/°C
I_N	RMS noise current spectral density (referred to input)	Test Circuit 2 f = 10MHz T_A = 25°C		1.8			1.8		pA/√Hz
I_T	Integrated RMS noise current over the bandwidth (referred to input)	T_A = 25°C Test Circuit 2							
	C_S=0[1]	Δf = 50MHz		13			13		nA
		Δf = 100MHz		20			20		nA
		Δf = 200MHz		35			35		nA
	C_S=1pF	Δf = 50MHz		13			13		nA
		Δf = 100MHz		21			21		nA
		Δf = 200MHz		41			41		nA
PSRR	Power supply rejection ratio[2] ($V_{CC1} = V_{CC2}$)	DC tested, ΔV_{CC} = 0.1V Equivalent AC Test Circuit 3	26	32		23	32		dB
PSRR	Power supply rejection ratio[2] (V_{CC1})	DC tested, ΔV_{CC} = 0.1V Equivalent AC Test Circuit 4	26	32		23	32		dB
PSRR	Power supply rejection ratio[2] (V_{CC2})	DC tested, ΔV_{CC} = 0.1V Equivalent AC Test Circuit 5	45	65		45	65		dB
PSRR	Power supply rejection ratio (ECL configuration)[2]	f = 0.1MHz Test Circuit 6		23			23		dB
V_{OMAX}	Maximum differential output voltage swing	$R_L = \infty$ Test Circuit 8, Procedure 3	2.4	3.2		1.7	3.2		V_{P-P}
$V_{IN\,MAX}$	Maximum input amplitude for output duty cycle of 50±5%[3]	Test Circuit 7	160			160			mV_{P-P}
t_R	Rise time for 50mV output signal[4]	Test Circuit 7		0.8	1.2		0.8	1.8	ns

NOTES:

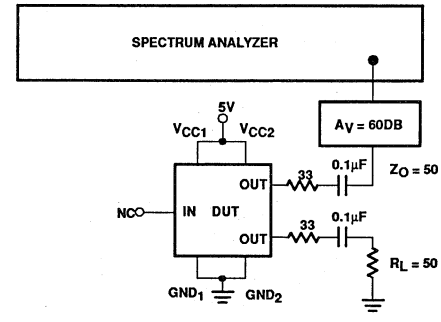
1. Package parasitic capacitance amounts to about 0.2pF
2. PSRR is output referenced and is circuit board layout dependent at higher frequencies. For best performance use RF filter in V_{CC} lines.
3. Guaranteed by linearity and overload tests.
4. t_R defined as 20-80% rise time. It is guaranteed by -3dB bandwidth test.

TEST CIRCUITS



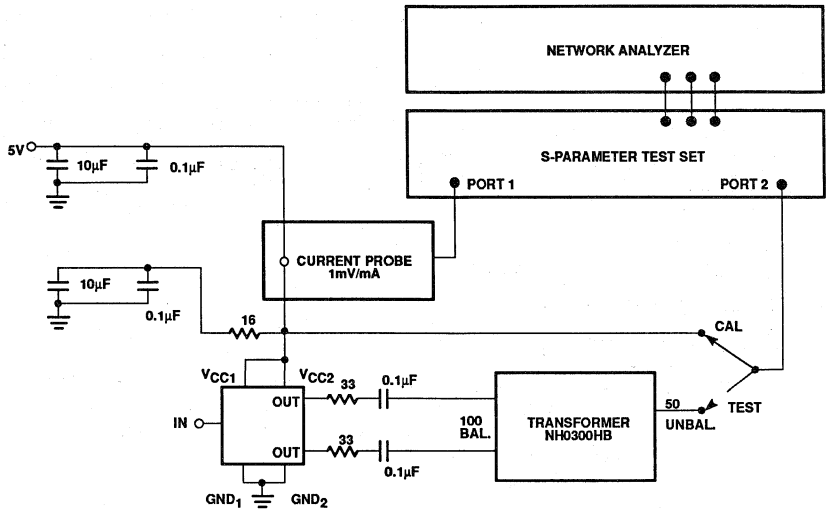
SINGLE-ENDED	DIFFERENTIAL
$R_T \approx \frac{V_{OUT}}{V_{IN}} R = 2 \cdot S21 \cdot R$	$R_T = \frac{V_{OUT}}{V_{IN}} R = 4 \cdot S21 \cdot R$
$R_O \approx Z_O \left\lvert \frac{1 + S22}{1 - S22} \right\rvert - 33$	$R_O = 2Z_O \left\lvert \frac{1 + S22}{1 - S22} \right\rvert - 66$

Test Circuit 1

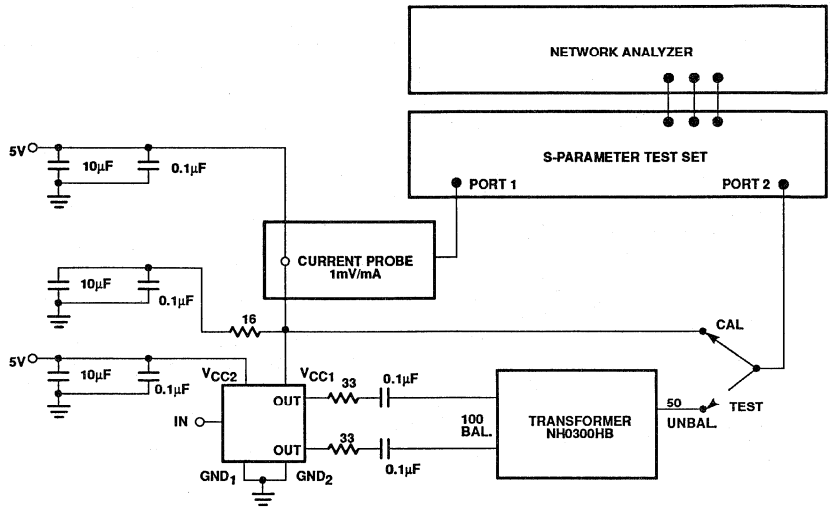


Test Circuit 2

TEST CIRCUITS (Continued)

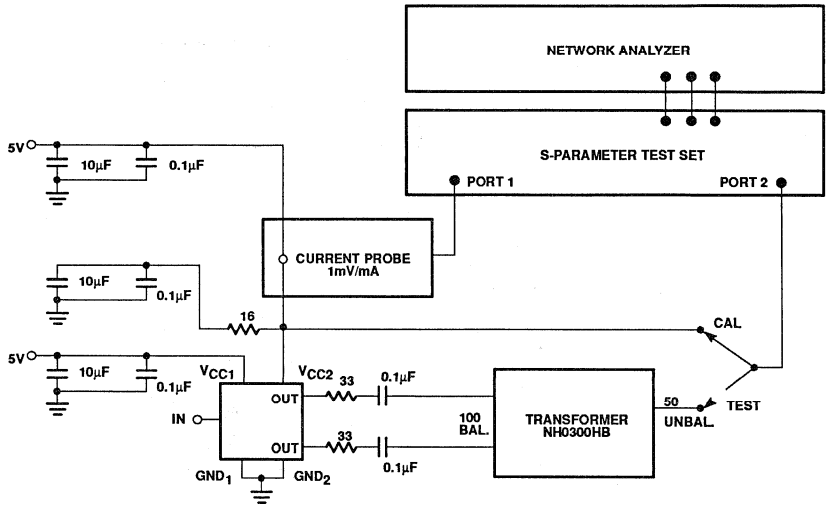


Test Circuit 3

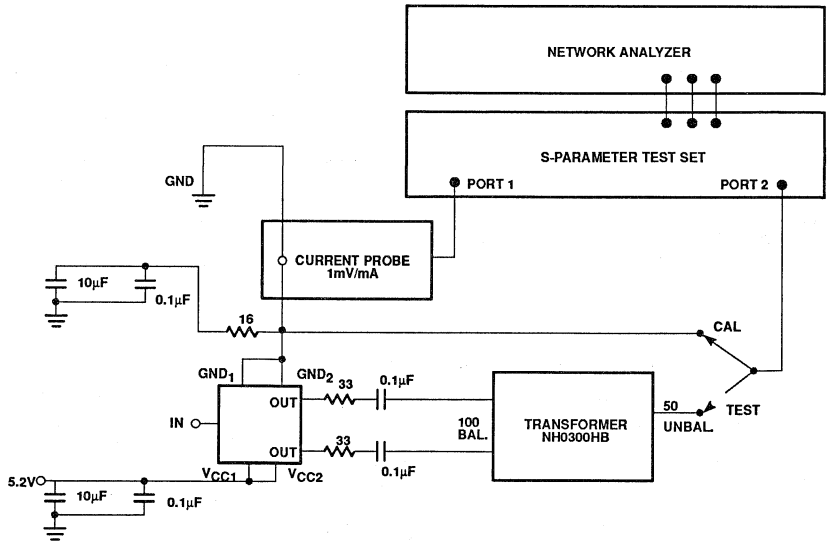


Test Circuit 4

TEST CIRCUITS (Continued)

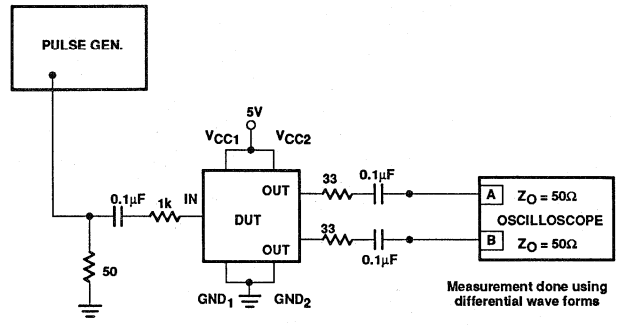


Test Circuit 5



Test Circuit 6

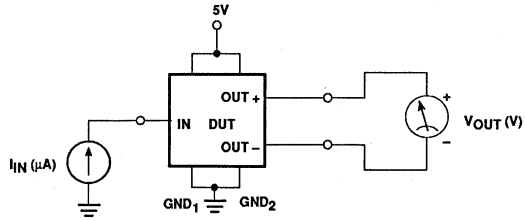
TEST CIRCUITS (Continued)

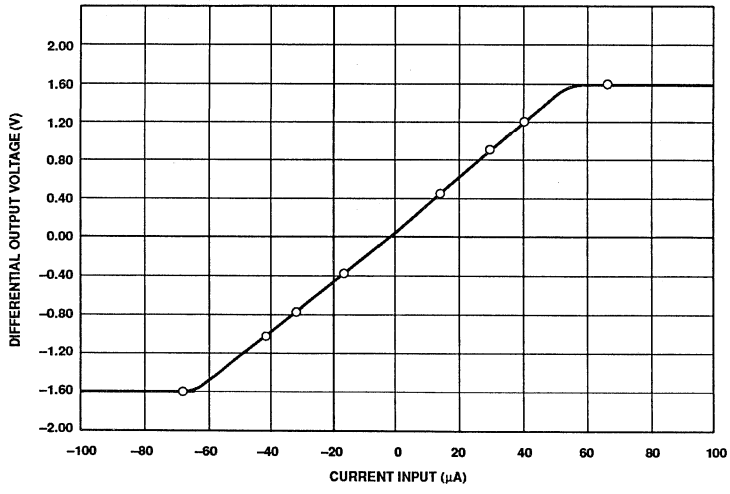


Test Circuit 7

TEST CIRCUITS (Continued)

Typical Differential Output Voltage vs Current Input





NE5211 TEST CONDITIONS

Procedure 1

R_T measured at 15μA

$R_T = (V_{O1} - V_{O2})/(+15\mu A - (-15\mu A))$

Where: V_{O1} Measured at $I_{IN} = +15\mu A$

V_{O2} Measured at $I_{IN} = -15\mu A$

Procedure 2

Linearity = 1 – ABS(($V_{OA} - V_{OB}$) / ($V_{O3} - V_{O4}$))

Where: V_{O3} Measured at $I_{IN} = +30\mu A$

V_{O4} Measured at $I_{IN} = -30\mu A$

$V_{OA} = R_T \cdot (+30\mu A) + V_{OB}$

$V_{OB} = R_T \cdot (-30\mu A) + V_{OB}$

Procedure 3

$V_{OMAX} = V_{O7} - V_{O8}$

Where: V_{O7} Measured at $I_{IN} = +65\mu A$

V_{O8} Measured at $I_{IN} = -65\mu A$

Procedure 4

I_{IN} Test Pass Conditions:

$V_{O7} - V_{O5} > 20mV$ and $V_{O6} - V_{O5} > 50mV$

Where: V_{O5} Measured at $I_{IN} = +40\mu A$

V_{O6} Measured at $I_{IN} = -400\mu A$

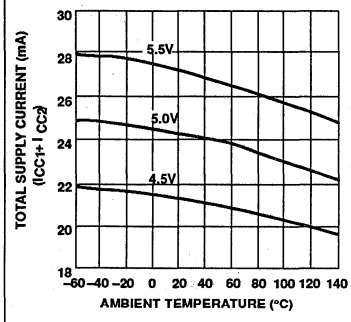
V_{O7} Measured at $I_{IN} = +65\mu A$

V_{O8} Measured at $I_{IN} = -65\mu A$

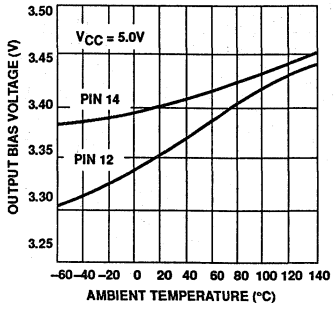
Test Circuit 8

TYPICAL PERFORMANCE CHARACTERISTICS

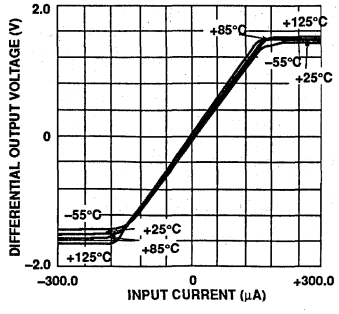
NE5211 Supply Current vs Temperature



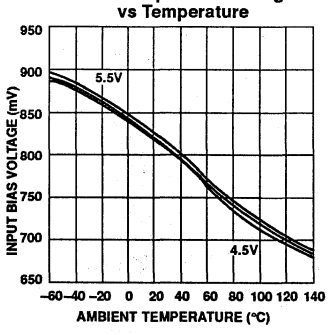
NE5211 Output Bias Voltage vs Temperature



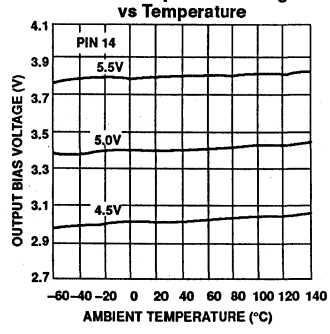
NE5211 Output Voltage vs Input Current



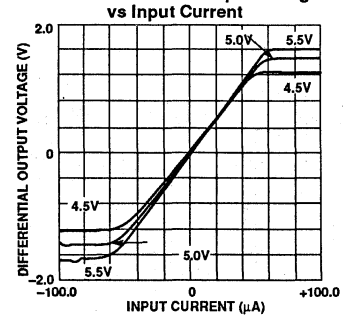
NE5211 Input Bias Voltage vs Temperature



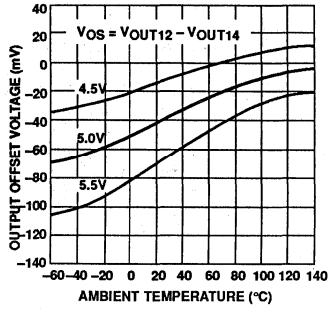
NE5211 Output Bias Voltage vs Temperature



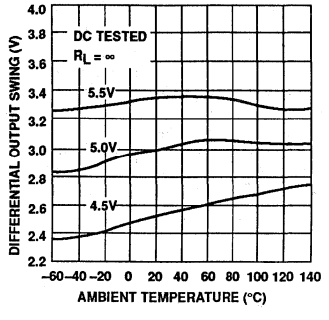
NE5211 Differential Output Voltage vs Input Current



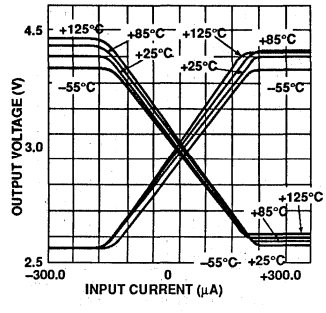
NE5211 Output Offset Voltage vs Temperature



NE5211 Differential Output Swing vs Temperature

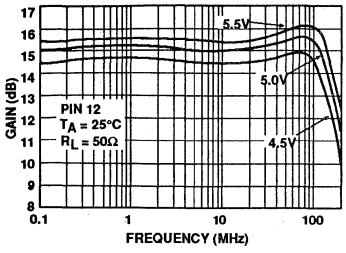


NE5211 Differential Output Voltage vs Input Current

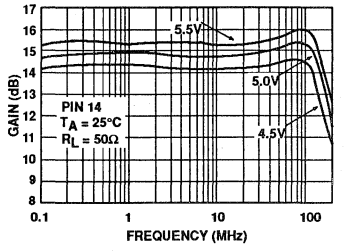


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

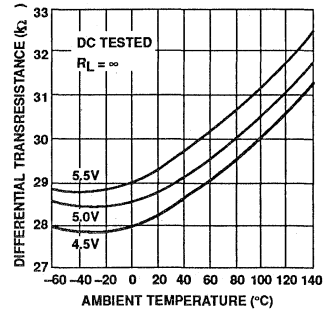
NE5211 Gain vs Frequency



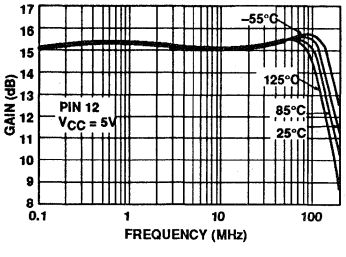
NE5211 Gain vs Frequency



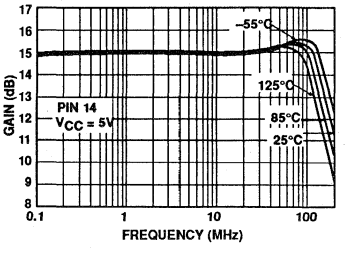
NE5211 Differential Transresistance vs Temperature



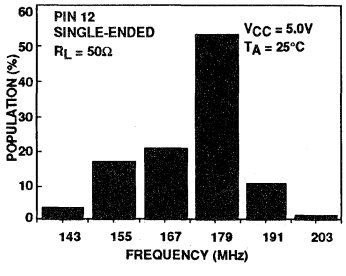
NE5211 Gain vs Frequency



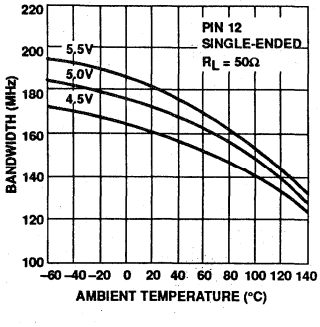
NE5211 Gain vs Frequency



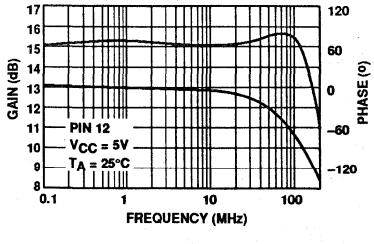
NE5211 Typical Bandwidth Distribution (70 Parts from 3 Wafer Lots)



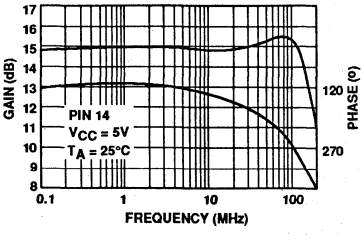
NE5211 Bandwidth vs Temperature



NE5211 Gain and Phase Shift vs Frequency

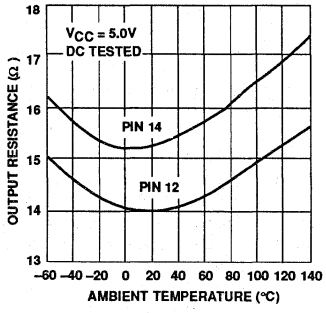


NE5211 Gain and Phase Shift vs Frequency

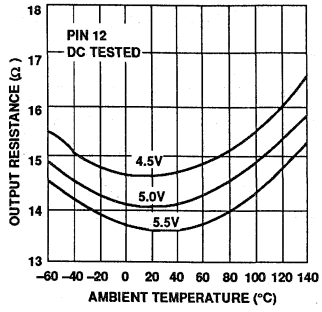


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

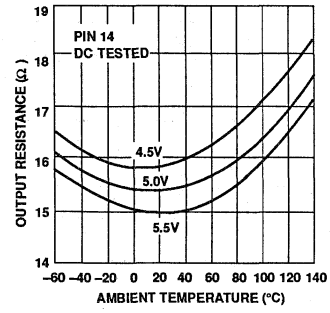
NE5211 Output Resistance vs Temperature



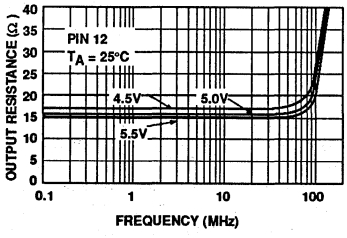
NE5211 Output Resistance vs Temperature



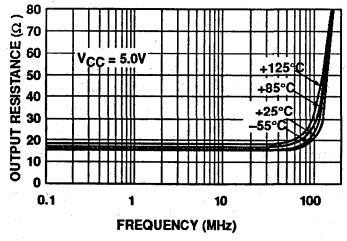
NE5211 Output Resistance vs Temperature



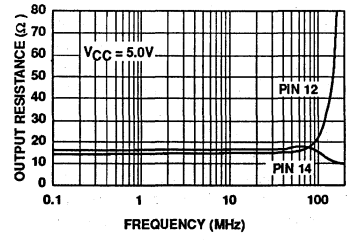
NE5211 Output Resistance vs Frequency



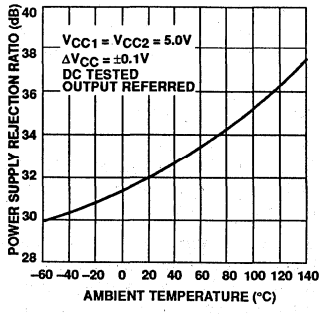
NE5211 Output Resistance vs Frequency



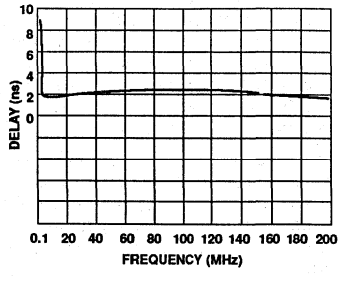
NE5211 Output Resistance vs Frequency



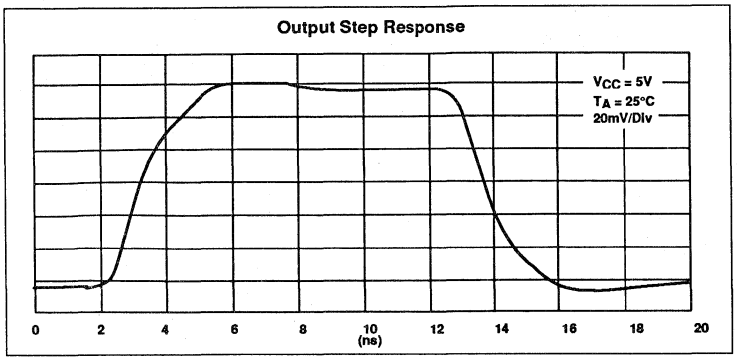
NE5211 Power Supply Rejection Ratio vs Temperature



NE5211 Group Delay vs Frequency



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



THEORY OF OPERATION

Transimpedance amplifiers have been widely used as the preamplifier in fiber-optic receivers. The NE5211 is a wide bandwidth (typically 180MHz) transimpedance amplifier designed primarily for input currents requiring a large dynamic range, such as those produced by a laser diode. The maximum input current before output stage clipping occurs at typically 50μA. The NE5211 is a bipolar transimpedance amplifier which is current driven at the input and generates a differential voltage signal at the outputs. The forward transfer function is therefore a ratio of the differential output voltage to a given input current with the dimensions of ohms. The main feature of this amplifier is a wideband, low-noise input stage which is desensitized to photodiode capacitance variations. When connected to a photodiode of a few picoFarads, the frequency response will not be degraded significantly. Except for the input stage, the entire signal path is differential to provide improved power-supply rejection and ease of interface to ECL type circuitry. A block diagram of the circuit is shown in Figure 1. The input stage (A1) employs shunt-series feedback to stabilize the current gain of the amplifier. The transresistance of the amplifier from the current source to the emitter of Q_3 is approximately the value of the feedback resistor, R_F=14.4kΩ. The gain from the second stage (A2) and emitter followers (A3 and A4) is about two. Therefore, the differential transresistance of the entire amplifier, R_T is

$$R_T = \frac{V_{OUT(diff)}}{I_{IN}} = 2R_F = 2(14.4K) = 28.8k\Omega$$

The single-ended transresistance of the amplifier is typically 14.4kΩ.

The simplified schematic in Figure 17 shows how an input current is converted to a differential output voltage. The amplifier has a single input for current which is referenced to Ground 1. An input current from a laser diode, for example, will be converted into a voltage by the feedback resistor R_F. The transistor Q1 provides most of the open loop gain of the circuit, A_{VOL}≈70. The emitter follower Q_2 minimizes loading on Q_1. The transistor Q_4, resistor R_7, and V_{B1} provide level shifting and interface with the $Q_{15} - Q_{16}$ differential pair of the second stage which is biased with an internal reference, V_{B2}. The differential outputs are derived from emitter followers $Q_{11} - Q_{12}$ which are biased by constant current sources. The collectors of $Q_{11} - Q_{12}$ are bonded to an external pin, V_{CC2}, in order to reduce the feedback to the input stage. The output impedance is about 17Ω single-ended. For ease of performance evaluation, a 33Ω resistor is used in series with each output to match to a 50Ω test system.

BANDWIDTH CALCULATIONS

The input stage, shown in Figure 3, employs shunt-series feedback to stabilize the current gain of the amplifier. A simplified analysis can determine the performance of the amplifier. The equivalent input capacitance, C_{IN}, in parallel with the source, I_S, is approximately 7.5pF, assuming that C_S=0 where C_S is the external source capacitance.

Since the input is driven by a current source the input must have a low input resistance. The input resistance, R_{IN}, is the ratio of the incremental input voltage, V_{IN}, to the corresponding input current, I_{IN} and can be calculated as:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{R_F}{1 + A_{VOL}} = \frac{14.4K}{71} = 203\Omega$$

More exact calculations would yield a higher value of 60Ω.

Thus C_{IN} and R_{IN} will form the dominant pole of the entire amplifier;

$$f_{-3dB} = \frac{1}{2\pi\ R_{IN}\ C_{IN}}$$

Assuming typical values for R_F = 14.4kΩ, R_{IN} = 200Ω, C_{IN} = 4pF

$$f_{-3dB} = \frac{1}{2\pi\ 4pF\ 200\Omega} = 200MHz$$

The operating point of Q1, Figure 2, has been optimized for the lowest current noise without introducing a second dominant pole in the pass-band. All poles associated with subsequent stages have been kept at sufficiently high enough frequencies to yield an overall single pole response. Although wider bandwidths have been achieved by using a cascode input stage configuration, the present solution has the advantage of a very uniform, highly desensitized frequency response because the Miller effect dominates over the external photodiode and stray capacitances. For example, assuming a source capacitance of 1pF, input stage voltage gain of 70, R_{IN} = 60Ω then the total input capacitance, C_{IN} = (1+7.5) pF which will lead to only a 12% bandwidth reduction.

NOISE

Most of the currently installed fiber-optic systems use non-coherent transmission and detect incident optical power. Therefore, receiver noise performance becomes very important. The input stage achieves a low input referred noise current (spectral density) of 3.5pA/√Hz. The transresistance configuration assures that the external high value bias resistors often required for photodiode biasing will not contribute to the total noise system noise. The equivalent input $_{RMS}$ noise current is strongly determined by the quiescent current of Q_1, the feedback resistor R_F, and the bandwidth; however, it is not dependent upon the internal Miller-capacitance. The measured wideband noise was 66nA in a 200MHz bandwidth.

DYNAMIC RANGE CALCULATIONS

The electrical dynamic range can be defined as the ratio of maximum input current to the peak noise current:

Electrical dynamic range, D_E, in a 200MHz bandwidth assuming I_{INMAX} = 60μA and a wideband noise of I_{EQ}=41nA$_{RMS}$ for an external source capacitance of C_S = 1pF.

$$D_E = \frac{(Max.\ input\ current)}{(Peak\ noise\ current)}$$

$$D_E(dB) = 20\log\frac{(60\cdot10^{-6})}{(\sqrt{2}\ 41\ 10^{-9})}$$

$$D_E(dB) = 20\log\frac{(60\mu A)}{(58nA)} = 60dB$$

In order to calculate the optical dynamic range the incident optical power must be considered.

For a given wavelength λ;

Energy of one Photon = $\frac{hc}{\lambda}$ watt sec (Joule)

Where h=Planck's Constant = 6.6×10^{-34} Joule sec.

c = speed of light = 3×10^{8} m/sec

c / λ = optical frequency

No. of incident photons/sec= $\frac{P}{\frac{hs}{\lambda}}$ where

P=optical incident power

No. of generated electrons/sec = $\eta\cdot\frac{P}{\frac{hs}{\lambda}}$

where η = quantum efficiency

$$= \frac{no.\ of\ generated\ electron\ hole\ paris}{no.\ of\ incident\ photons}$$

$$\therefore I = \eta\cdot\frac{P}{\frac{hs}{\lambda}}\cdot e\ Amps\ (Coulombs/sec.)$$

where e = electron charge = 1.6×10^{-19} Coulombs

Responsivity R = $\frac{\eta\cdot e}{\frac{hs}{\lambda}}$ Amp/watt

$I = P\cdot R$

Assuming a data rate of 400 Mbaud (Bandwidth, B=200MHz), the noise parameter Z may be calculated as:[1]

$$Z = \frac{I_{EQ}}{qB} = \frac{41\cdot10^{-9}}{(1.6\cdot10^{-19})(200\cdot10^{6})} = 1281$$

where Z is the ratio of $_{RMS}$ noise output to the peak response to a single hole-electron pair. Assuming 100% photodetector quantum efficiency, half mark/half space digital transmission, 850nm lightwave and using Gaussian approximation, the minimum required optical power to achieve 10^{-9} BER is:

$$P_{avMIN} = 12\frac{hc}{\lambda}B\ Z = 12\cdot2.3\cdot10^{-19}$$

$$200\cdot10^{6}\ (1281) = 719nW = -31.5dBm$$

$$= 1139nW = -29.4dBm$$

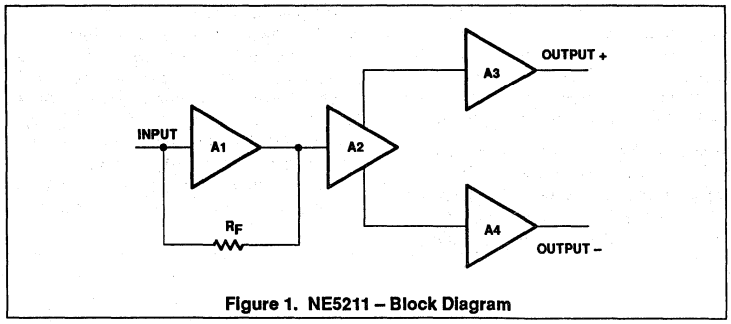


Figure 1. NE5211 – Block Diagram

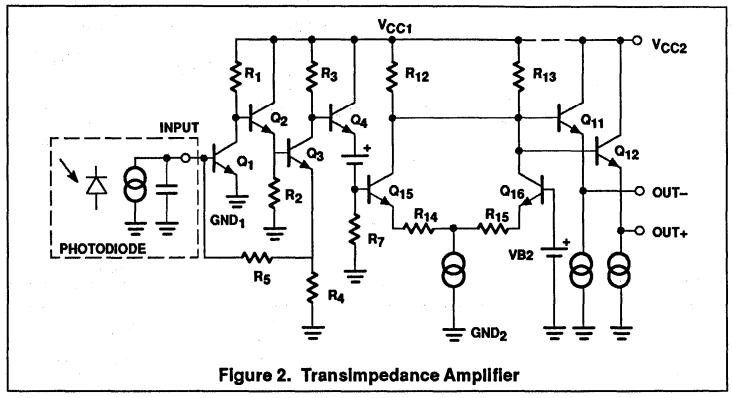


Figure 2. Transimpedance Amplifier

where h is Planck's Constant, c is the speed of light, λ is the wavelength. The minimum input current to the NE5211, at this input power is:

$$I_{avMIN} = qP_{avMIN}\frac{\lambda}{hc}\quad\frac{1}{Joule}\cdot\frac{Joule}{\sec}\cdot q = I$$

$$= \frac{707\cdot10^{-9}\cdot1.6\cdot10^{-19}}{2.3\cdot10^{-19}}$$

$$= 500nA$$

Choosing the maximum peak overload current of I_{avMAX}=60μA, the maximum mean optical power is:

$$P_{avMAX} = \frac{hcI_{avMAX}}{\lambda q} = \frac{2.3\cdot10^{-19}}{1.6\cdot10^{-19}}\ 60\cdot10\mu A$$

$$= 86\mu W\ or\ -10.6dBm\ (optical)$$

Thus the optical dynamic range, D_O is:

$D_O = P_{avMAX} - P_{avMIN} = -4.6 - (-29.4) = 24.8dB.$

$$D_O = P_{avMAX} - P_{avMIN} = -31.5 - (-10.6)$$

$$= 20.8dB$$

This represents the maximum limit attainable with the NE5211 operating at 200MHz bandwidth, with a half mark/half space digital transmission at 850nm wavelength.

APPLICATION INFORMATION

Package parasitics, particularly ground lead inductances and parasitic capacitances, can significantly degrade the frequency response. Since the NE5211 has differential outputs which can feed back signals to the input by parasitic package or board layout capacitances, both peaking and attenuating type frequency response shaping is possible. Constructing the board layout so that Ground 1 and Ground 2 have very low impedance paths has produced the best results. This was accomplished by adding a ground-plane stripe underneath the device connecting Ground 1, Pins 8–11, and Ground 2, Pins 1 and 2 on opposite ends of the SO14 package. This ground-plane stripe also provides isolation between the output return currents flowing to either V_{CC2} or Ground 2 and the input photodiode currents to flowing to Ground 1. Without this ground-plane stripe and with large lead inductances on the board, the part may be unstable and oscillate near 800MHz. The easiest way to realize that the part is not functioning normally is to measure the DC voltages at the outputs. If they are not close to their quiescent values of 3.3V (for a 5V supply), then the circuit may be

1. S.D. Personick, *Optical Fiber Transmission Systems*, Plenum Press, NY, 1981, Chapter 3.

oscillating. Input pin layout necessitates that the photodiode be physically very close to the input and Ground 1. Connecting Pins 3 and 5 to Ground 1 will tend to shield the input but it will also tend to increase the capacitance on the input and slightly reduce the bandwidth.

As with any high-frequency device, some precautions must be observed in order to enjoy reliable performance. The first of these is the use of a well-regulated power supply. The supply must be capable of providing varying amounts of current without significantly changing the voltage level. Proper supply bypassing requires that a good quality 0.1μF high-frequency capacitor be inserted between V_{CC1} and V_{CC2}, preferably a chip capacitor, as close to the package pins as possible. Also, the parallel combination of 0.1μF capacitors with 10μF tantalum capacitors from each supply, V_{CC1} and V_{CC2}, to the ground plane should provide adequate decoupling. Some applications may require an RF choke in series with the power supply line. Separate analog and digital ground leads must be maintained and printed circuit board ground plane should be employed whenever possible.

Figure 4 depicts a 50Mb/s TTL fiber-optic receiver using the BPF31, 850nm LED, the NE5211 and the NE5214 post amplifier.

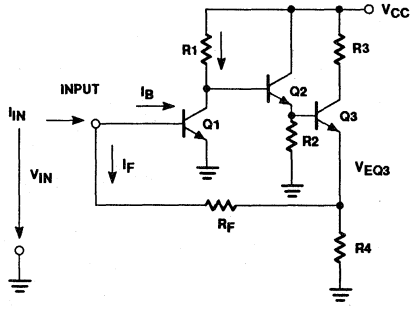


Figure 3. Shunt-Series Input Stage

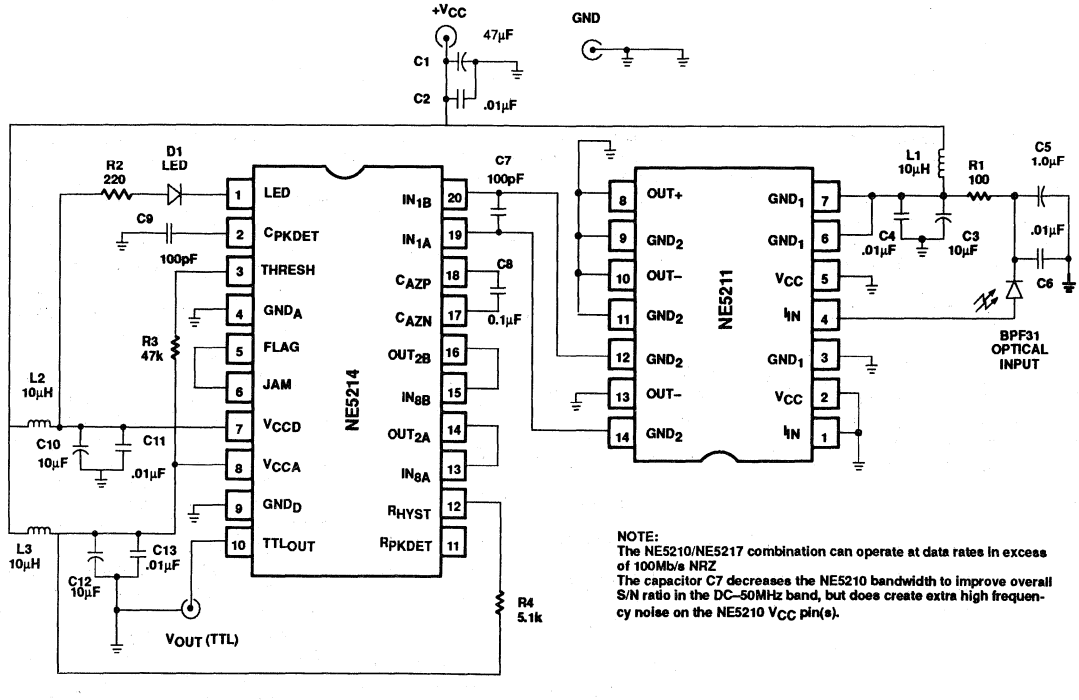


Figure 4. A 50Mb/s Fiber Optic Receiver

Transimpedance amplifier (140MHz) NE/SA/SE5212A

DESCRIPTION

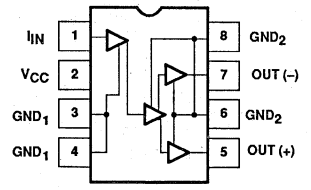
The NE/SA/SE5212A is a 14kΩ transimpedance, wideband, low noise differential output amplifier, particularly suitable for signal recovery in fiber optic receivers and in any other applications where very low signal levels obtained from high-impedance sources need to be amplified.

APPLICATIONS

- Fiber-optic receivers, analog and digital
- Current-to-voltage converters
- Wideband gain block
- Medical and scientific instrumentation
- Sensor preamplifiers
- Single-ended to differential conversion
- Low noise RF amplifiers
- RF signal processing

PIN CONFIGURATION

N, FE, D Packages



FEATURES

- Extremely low noise: 2.5pA/√Hz
- Single 5V supply
- Large bandwidth: 140MHz
- Differential outputs
- Low input/output impedances
- 14kΩ differential transresistance
- ESD hardened

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5212AN
8-Pin Plastic SO	0 to +70°C	NE5212AD
8-Pin Ceramic DIP	0 to +70°C	NE5212AFE
8-Pin Plastic SO	-40°C to +85°C	SA5212AD
8-Pin Plastic DIP	-40°C to +85°C	SA5212AN
8-Pin Ceramic DIP	-40°C to +85°C	SA5212AFE
8-Pin Plastic DIP	-55°C to +125°C	SE5212AN
8-Pin Ceramic DIP	-55°C to +125°C	SE5212AFE

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING			UNIT
		NE5212A	SA5212A	SE5212A	
V_{CC}	Power Supply	6	6	6	V
$P_{D\,MAX}$	Power dissipation, T_A=25°C (still air)[1]				
	8-Pin Plastic DIP	1100	1100	1100	mW
	8-Pin Plastic SO	750	750	750	mW
	8-Pin Cerdip	750	750	750	mw
$I_{IN\,MAX}$	Maximum input current[2]	5	5	5	mA
T_A	Operating ambient temperature range	0 to 70	-40 to 85	-55 to 125	°C
T_J	Operating junction	-55 to 150	-55 to 150	-55 to 150	°C
T_{STG}	Storage temperature range	-65 to 150	-65 to 150	-65 to 150	°C

NOTES:

1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance:
   8-Pin Plastic DIP: 110°C/W
   8-Pin Plastic SO: 160°C/W
   8-Pin Cerdip: 165°C/W
2. The use of a pull-up resistor to V_{CC}, for the PIN diode, is recommended

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	4.5 to 5.5	V
T_A	Ambient temperature ranges		
	NE Grade	0 to +70	°C
	SA Grade	-40 to +85	°C
	SE Grade	-55 to +125	°C
T_J	Junction temperature ranges		
	NE Grade	0 to +90	°C
	SA Grade	-40 to +105	°C
	SE Grade	-55 to +145	°C

DC ELECTRICAL CHARACTERISTICS

Minimum and Maximum limits apply over operating temperature range at V_{CC}=5V, unless otherwise specified. Typical data applies at V_{CC}=5V and T_A=25°C[1].

SYMBOL	PARAMETER	TEST CONDITIONS	NE5212A			SA/SE5212A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IN}	Input bias voltage		0.6	0.8	0.95	0.55	0.8	1.05	V
$V_{O\pm}$	Output bias voltage		2.8	3.3	3.7	2.5	3.3	3.8	V
V_{OS}	Output offset voltage				80			120	mV
I_{CC}	Supply current		21	26	32	20	26	33	mA
I_{OMAX}	Output sink/source current		3	4		3	4		mA
I_{IN}	Maximum input current (2% linearity)	Test Circuit 6, Procedure 2	±60	±80		±40	±80		µA
$I_{N\ MAX}$	Maximum input current overload threshold	Test Circuit 6, Procedure 4	±80	±120		±60	±120		µA

NOTES:

1. As in all high freuency circuits, a supply bypass capacitor should be located as close to the part as possible.

AC ELECTRICAL CHARACTERISTICS

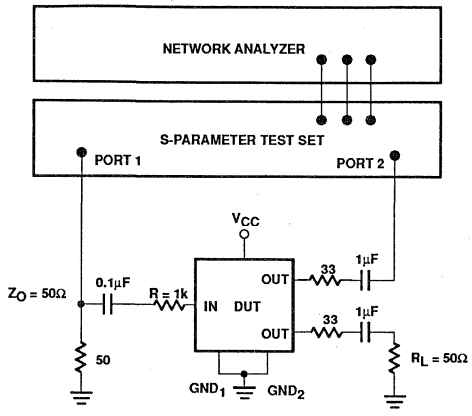
Minimum and Maximum limits apply over operating temperature range at V_{CC}=5V, unless otherwise specified. Typical data applies at V_{CC}=5V and T_A=25°C[5].

SYMBOL	PARAMETER	TEST CONDITIONS	NE5212A			SA/SE5212A			UNIT
			Min	Typ	Max	Min	Typ	Max	
R_T	Transresistance (differential output)	DC tested, $R_L = \infty$ Test Circuit 6, Procedure 1	9.8	14	18.2	9.0	14	19	kΩ
R_O	Output resistance (differential output)	DC tested	14	30	42	14	30	46	Ω
R_T	Transresistance (single-ended output)	DC tested, $R_L = \infty$	4.9	7	9.1	4.5	7	9.5	kΩ
R_O	Output resistance (single-ended output)	DC tested	7	15	21	7	15	23	Ω
f_{3dB}	Bandwidth (-3dB)	Test Circuit 1 D package, T_A = 25°C	100	140		100	140		MHz
		N, FE packages, T_A = 25°C	100	120		100	120		MHz
R_{IN}	Input resistance		75	110	143	70	110	150	Ω
C_{IN}	Input capacitance			10	15		10	18	pF
$\Delta R/\Delta V$	Transresistance power supply sensitivity	V_{CC} = 5 ±0.5V		9.6			9.6		%/V
$\Delta R/\Delta T$	Transresistance ambient temperature sensitivity	D package $\Delta T_A = T_{A\,MAX} - T_{A\,MIN}$		0.05			0.05		%/°C
I_N	RMS noise current spectral density (referred to input)	Test Circuit 2 f = 10MHz T_A = 25°C		2.5			2.5		pA/√Hz
I_T	Integrated RMS noise current over the bandwidth (referred to input) C_S = 0[1]	T_A = 25°C Test Circuit 2 Δf = 50MHz		20			20		nA
		Δf = 100MHz		27			27		nA
		Δf = 200MHz		40			40		nA
	C_S = 1pF	Δf = 50MHz		22			22		nA
		Δf = 100MHz		32			32		nA
		Δf = 200MHz		52			52		nA
PSRR	Power supply rejection ratio[2]	Any package DC tested ΔV_{CC} = 0.1V Equivalent AC Test Circuit 3	26	33		20	33		dB
PSRR	Power supply rejection ratio[2] (ECL configuration)	Any package f = 0.1MHz[1] Test Circuit 4		23			23		dB
$V_{O\,MAX}$	Maximum differential output voltage swing	$R_L = \infty$ Test Circuit 6, Procedure 3	2.4	3.2		1.7	3.2		V_{P-P}
$V_{IN\,MAX}$	Maximum input amplitude for output duty cycle of 50 ±5%[3]	Test Circuit 5		325			325		mV_{P-P}
t_R	Rise time for 50mV output signal[4]	Test Circuit 5		2.0			2.0		ns

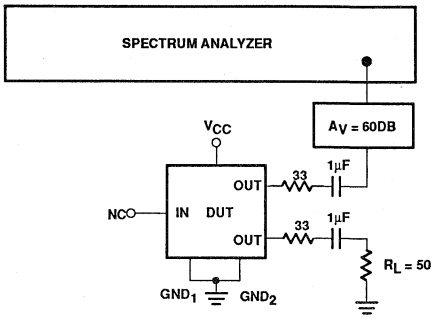
NOTES:
1. Package parasitic capacitance amounts to about 0.2pF.
2. PSRR is output referenced and is circuit board layout dependent at higher frequencies. For best performance use RF filter in V_{CC} line.
3. Guaranteed by linearity and over load tests.
4. t_R defined as 20-80% rise time. It is guaranteed by -3dB bandwidth test.
5. As in all high freuency circuits, a supply bypass capacitor should be located as close to the part as possible.

TEST CIRCUITS

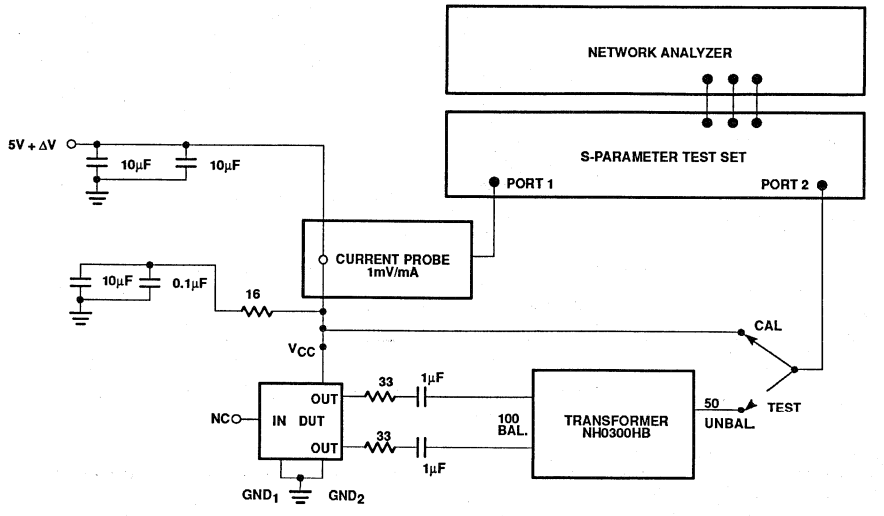
SINGLE-ENDED	DIFFERENTIAL
$R_t = \frac{V_{OUT}}{V_{IN}} 2 \cdot S21 \cdot R$	$R_t = \frac{V_{OUT}}{V_{IN}} 4 \cdot S21 \cdot R$
$R_O = Z_O \left\lvert \frac{1 + S22}{1 - S22} \right\rvert - 33$	$R_O = 2Z_O \left\lvert \frac{1 + S22}{1 - S22} \right\rvert - 66$



Test Circuit 1

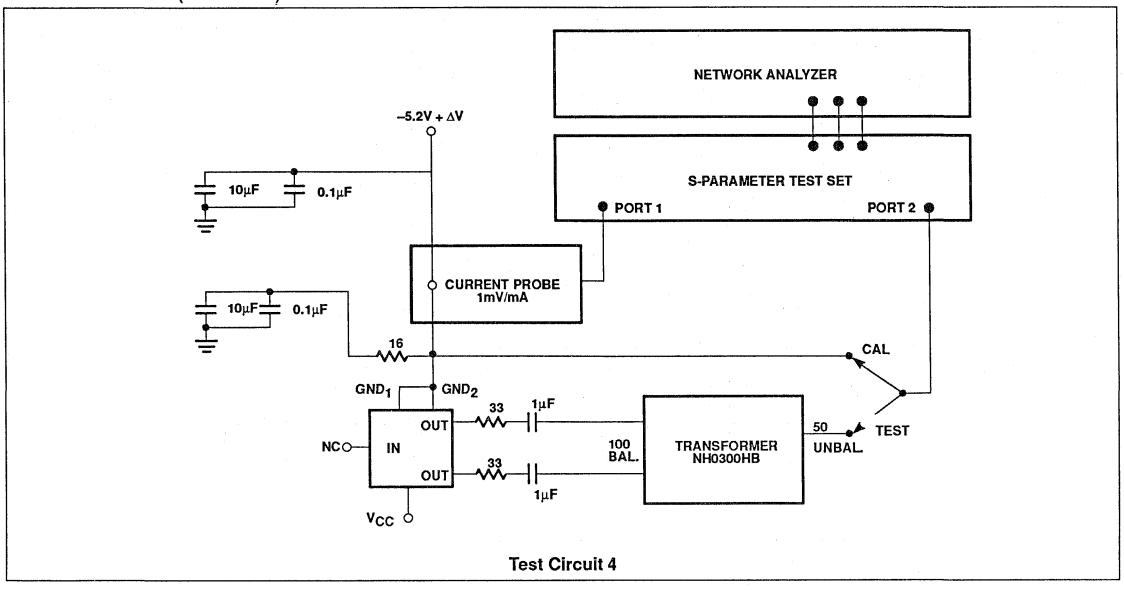


Test Circuit 2

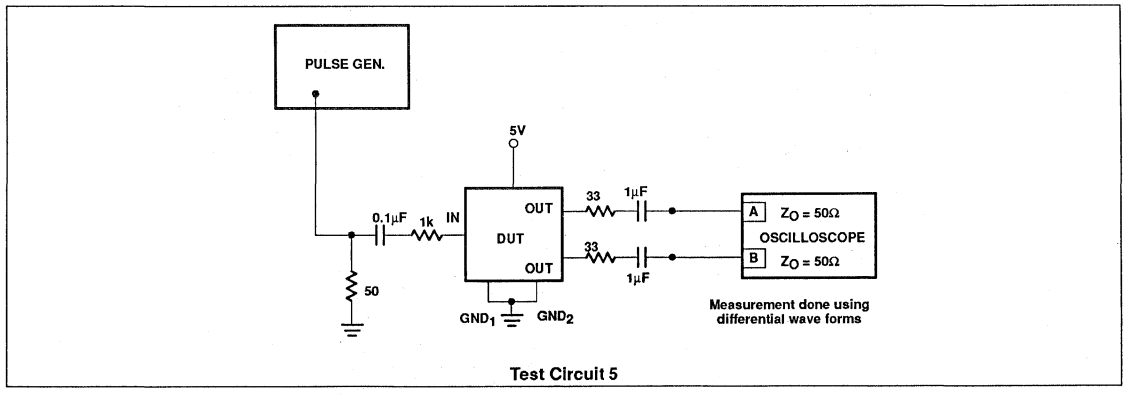


Test Circuit 3

TEST CIRCUITS (Continued)



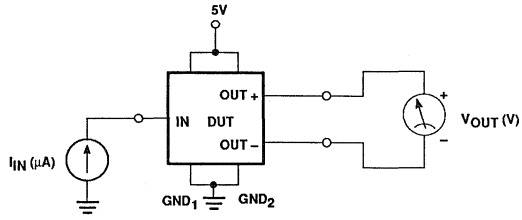
Test Circuit 4

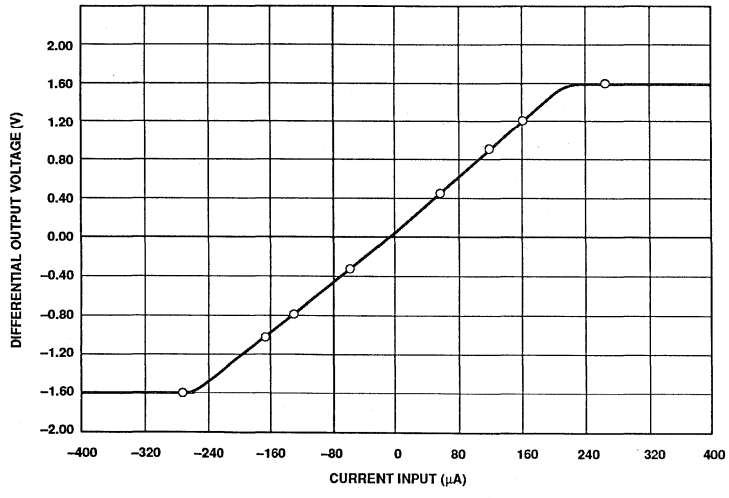


Test Circuit 5

TEST CIRCUITS (Continued)

Typical Differential Output Voltage vs Current Input





NE5212A TEST CONDITIONS

Procedure 1

R_T measured at 30μA
$R_T = (V_{O1} - V_{O2})/(+30\mu A - (-30\mu A))$
Where: V_{O1} Measured at $I_{IN} = +30\mu A$
V_{O2} Measured at $I_{IN} = -30\mu A$

Procedure 2

Linearity = 1 – ABS(($V_{OA} - V_{OB}$) / ($V_{O3} - V_{O4}$))
Where: V_{O3} Measured at $I_{IN} = +60\mu A$
V_{O4} Measured at $I_{IN} = -60\mu A$
$V_{OA} = R_T \cdot (+60\mu A) + V_{OB}$
$V_{OB} = R_T \cdot (-60\mu A) + V_{OB}$

Procedure 3

$V_{OMAX} = V_{O7} - V_{O8}$
Where: V_{O7} Measured at $I_{IN} = +130\mu A$
V_{O8} Measured at $I_{IN} = -130\mu A$

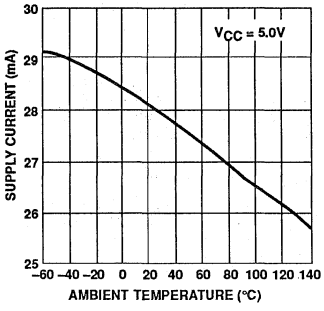
Procedure 4

I_{IN} Test Pass Conditions:
$V_{O7} - V_{O5} > 20mV$ and $V_{O6} - V_{O5} > 20mV$
Where: V_{O5} Measured at $I_{IN} = +800\mu A$
V_{O6} Measured at $I_{IN} = -80\mu A$
V_{O7} Measured at $I_{IN} = +130\mu A$
V_{O8} Measured at $I_{IN} = -130\mu A$

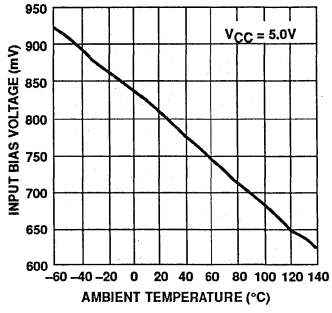
Test Circuit 8

TYPICAL PERFORMANCE CHARACTERISTICS

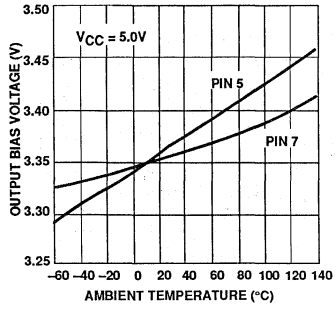
NE5212A Supply Current vs Temperature



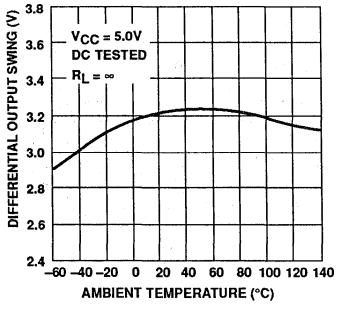
NE5212A Input Bias Voltage vs Temperature



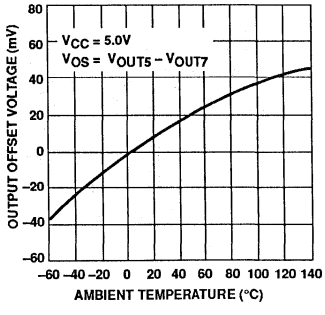
NE5212A Output Bias Voltage vs Temperature



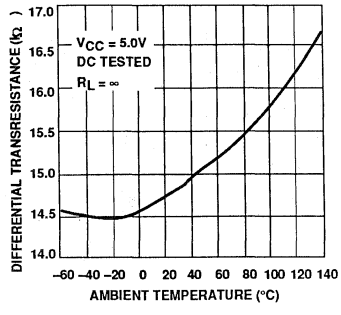
NE5212A Differential Output Swing vs Temperature



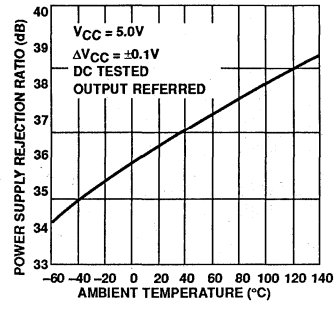
NE5212A Output Offset Voltage vs Temperature



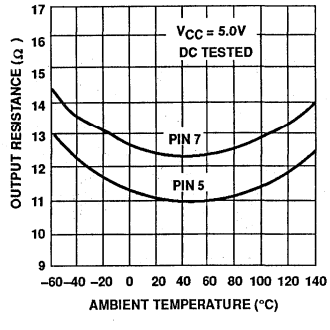
NE5212A Differential Transresistance vs Temperature



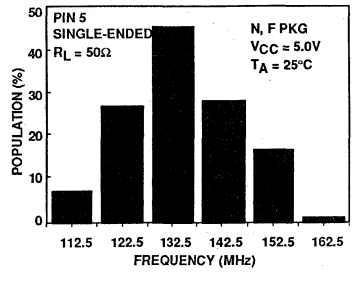
NE5212A Power Supply Rejection Ratio vs Temperature



NE5212A Output Resistance vs Temperature

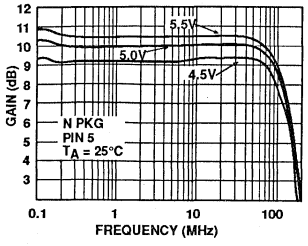


NE5212A Typical Bandwidth Distribution (75 Parts from 3 Wafer Lots)

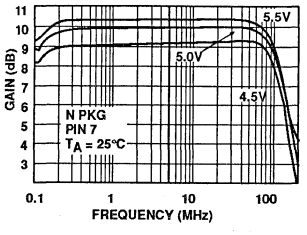


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

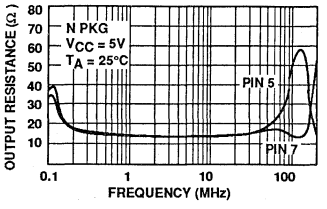
Gain vs Frequency



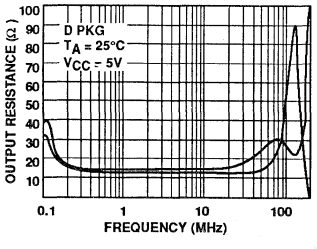
Gain vs Frequency



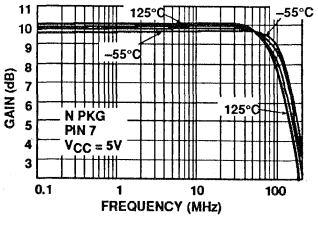
Output Resistance vs Frequency



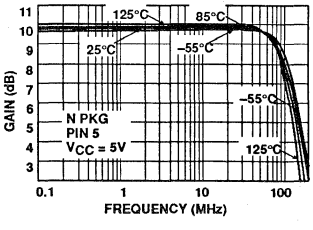
Output Resistance vs Frequency



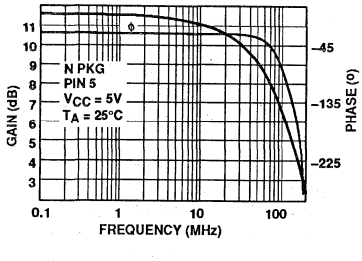
Gain vs Frequency



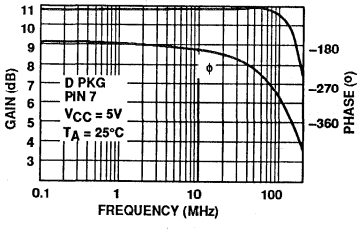
Gain vs Frequency



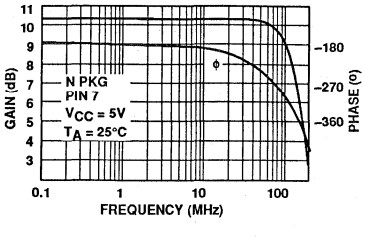
Gain and Phase Shift vs Frequency



Gain and Phase Shift vs Frequency

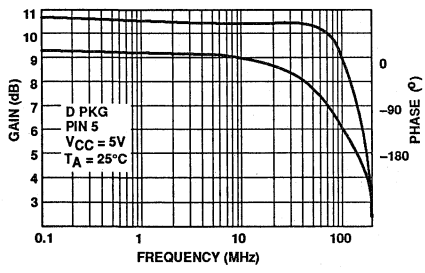


Gain and Phase Shift vs Frequency

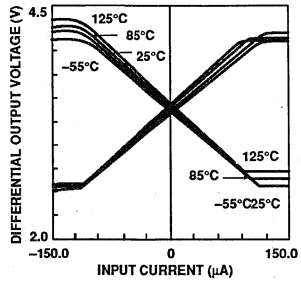


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

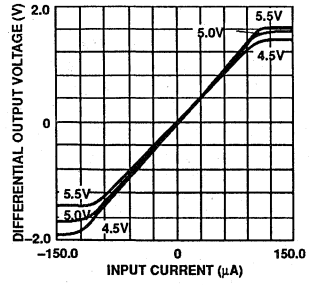
Gain and Phase Shift vs Frequency



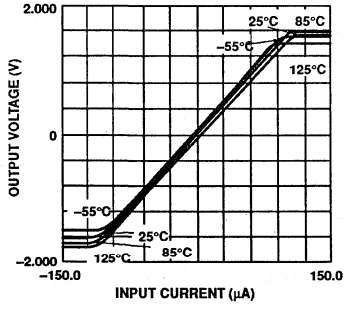
Output Voltage vs Input Current



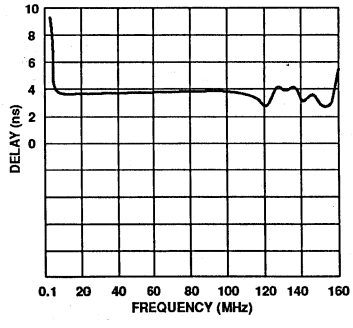
Differential Output Voltage vs Input Current



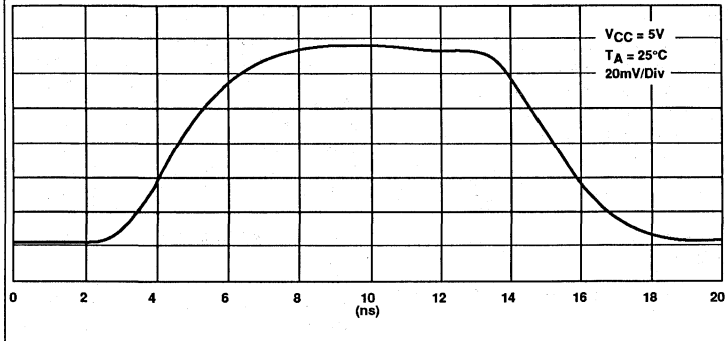
Differential Output Voltage vs Input Current



Group Delay vs Frequency



Output Step Response



THEORY OF OPERATION

Transimpedance amplifiers have been widely used as the preamplifier in fiber-optic receivers. The NE5212A is a wide bandwidth (typically 280MHz) transimpedance amplifier designed primarily for input currents requiring a large dynamic range, such as those produced by a laser diode. The maximum input current before output stage clipping occurs at typically 240μA. The NE5212A is a bipolar transimpedance amplifier which is current driven at the input and generates a differential voltage signal at the outputs. The forward transfer function is therefore a ratio of the differential output voltage to a given input current with the dimensions of ohms. The main feature of this amplifier is a wideband, low-noise input stage which is desensitized to photodiode capacitance variations. When connected to a photodiode of a few picoFarads, the frequency response will not be degraded significantly. Except for the input stage, the entire signal path is differential to provide improved power-supply rejection and ease of interface to ECL type circuitry. A block diagram of the circuit is shown in Figure 1. The input stage (A1) employs shunt-series feedback to stabilize the current gain of the amplifier. The transresistance of the amplifier from the current source to the emitter of Q_3 is approximately the value of the feedback resistor, R_F=3.6kΩ. The gain from the second stage (A2) and emitter followers (A3 and A4) is about two. Therefore, the differential transresistance of the entire amplifier, R_T is

$$R_T = \frac{V_{OUT(diff)}}{I_{IN}} = 2R_F = 2(7.2K) = 14.4k\Omega$$

The single-ended transresistance of the amplifier is typically 3.6kΩ.

The simplified schematic in Figure 2 shows how an input current is converted to a differential output voltage. The amplifier has a single input for current which is referenced to Ground 1. An input current from a laser diode, for example, will be converted into a voltage by the feedback resistor R_F. The transistor Q1 provides most of the open loop gain of the circuit, A_{VOL}≈70. The emitter follower Q_2 minimizes loading on Q_1. The transistor Q_4, resistor R_7, and V_{B1} provide level shifting and interface with the $Q_{15} - Q_{16}$ differential pair of the second stage which is biased with an internal reference, V_{B2}. The differential outputs are derived from emitter followers $Q_{11} - Q_{12}$ which are biased by constant current sources. The collectors of $Q_{11} - Q_{12}$ are bonded to an external pin, V_{CC2}, in order to reduce the feedback to the input stage. The output impedance is about 17Ω single-ended. For ease of performance evaluation, a 33Ω resistor is used in series with each output to match to a 50Ω test system.

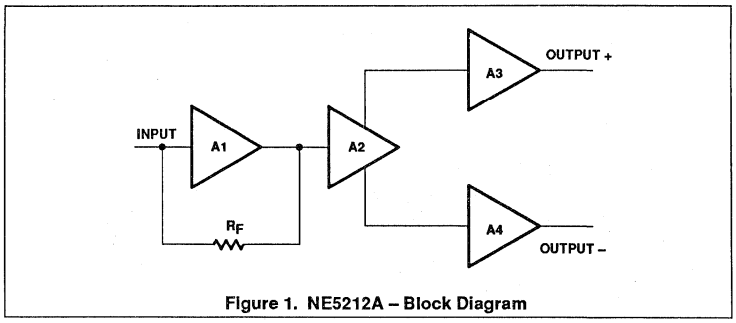


Figure 1. NE5212A – Block Diagram

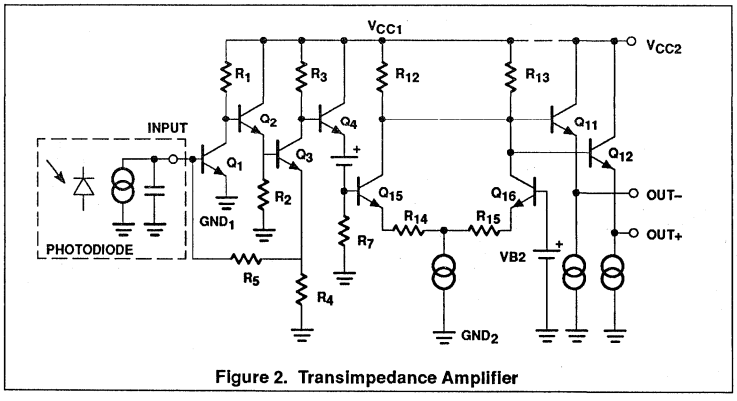


Figure 2. Transimpedance Amplifier

BANDWIDTH CALCULATIONS

The input stage, shown in Figure 3, employs shunt-series feedback to stabilize the current gain of the amplifier. A simplified analysis can determine the performance of the amplifier. The equivalent input capacitance, C_{IN}, in parallel with the source, I_S, is approximately 7.5pF, assuming that C_S=0 where C_S is the external source capacitance.

Since the input is driven by a current source the input must have a low input resistance. The input resistance, R_{IN}, is the ratio of the incremental input voltage, V_{IN}, to the corresponding input current, I_{IN} and can be calculated as:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{R_F}{1 + A_{VOL}} = \frac{7.2K}{70} = 103\Omega$$

More exact calculations would yield a higher value of 110Ω.

Thus C_{IN} and R_{IN} will form the dominant pole of the entire amplifier;

$$f_{-3dB} = \frac{1}{2\pi\ R_{IN}\ C_{IN}}$$

Assuming typical values for R_F = 7.2kΩ, R_{IN} = 110Ω, C_{IN} = 10pF

$$f_{-3dB} = \frac{1}{2\pi\ (110)\ 10 \cdot 10^{-12}} = 145MHz$$

The operating point of Q1, Figure 2, has been optimized for the lowest current noise without introducing a second dominant pole in the pass-band. All poles associated with subsequent stages have been kept at sufficiently high enough frequencies to yield an overall single pole response. Although wider bandwidths have been achieved by using a cascode input stage configuration, the present solution has the advantage of a very uniform, highly desensitized frequency response because the Miller effect dominates over the external photodiode and stray capacitances. For example, assuming a source capacitance of 1pF, input stage voltage gain of 70, R_{IN} = 60Ω then the total input capacitance, C_{IN} = (1+7.5) pF which will lead to only a 12% bandwidth reduction.

NOISE

Most of the currently installed fiber-optic systems use non-coherent transmission and detect incident optical power. Therefore, receiver noise performance becomes very

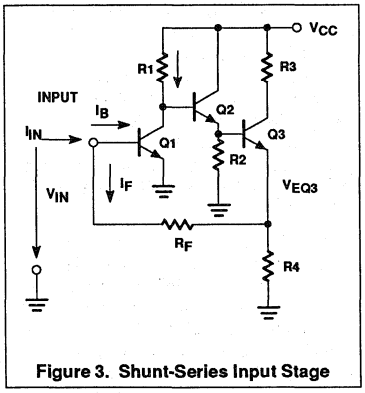


Figure 3. Shunt-Series Input Stage

important. The input stage achieves a low input referred noise current (spectral density) of 3.5pA/√Hz. The transresistance configuration assures that the external high value bias resistors often required for photodiode biasing will not contribute to the total noise system noise. The equivalent input $_{RMS}$ noise current is strongly determined by the quiescent current of Q_1, the feedback resistor R_F, and the bandwidth; however, it is not dependent upon the internal Miller-capacitance. The measured wideband noise was 66nA in a 200MHz bandwidth.

DYNAMIC RANGE

The electrical dynamic range can be defined as the ratio of maximum input current to the peak noise current:

Electrical dynamic range, D_E, in a 200MHz bandwidth assuming I_{INMAX} = 240μA and a wideband noise of I_{EQ}=52nA$_{RMS}$ for an external source capacitance of C_S = 1pF.

$$D_E = \frac{(Max.\ input\ current)}{(Peak\ noise\ current)}$$

$$D_E(dB) = 20\log\frac{(120\cdot10^{-6})}{(\sqrt{2}\ 52nA)}$$

$$D_E(dB) = 20\log\frac{(120\mu A)}{(73nA)} = 64dB$$

In order to calculate the optical dynamic range the incident optical power must be considered.

For a given wavelength λ;

Energy of one Photon = $\frac{hc}{\lambda}$ watt sec (Joule)

Where h=Planck's Constant = 6.6×10^{-34} Joule sec.

c = speed of light = 3×10^{8} m/sec

c / λ = optical frequency

No. of incident photons/sec= where P=optical incident power

No. of incident photons/sec = $\frac{\frac{P}{hs}}{\lambda}$

where P = optical incident power

No. of generated electrons/sec = $\eta\cdot\frac{\frac{P}{hs}}{\lambda}$

where η = quantum efficiency

$$= \frac{no.\ of\ generated\ electron\ hole\ paris}{no.\ of\ incident\ photons}$$

$$\therefore I = \eta\cdot\frac{\frac{P}{hs}}{\lambda}\cdot e\ Amps\ (Coulombs/sec.)$$

where e = electron charge = 1.6×10^{-19} Coulombs

Responsivity R = $\frac{\eta\cdot e}{\frac{hs}{\lambda}}$ Amp/watt

$$I = P\cdot R$$

Assuming a data rate of 400 Mbaud (Bandwidth, B=200MHz), the noise parameter Z may be calculated as:[1]

$$Z = \frac{I_{EQ}}{qB} = \frac{52\cdot10^{-9}}{(1.6\cdot10^{-19})(200\cdot10^{6})} = 1625\left(\frac{Amp}{Amp}\right)$$

where Z is the ratio of $_{RMS}$ noise output to the peak response to a single hole-electron pair. Assuming 100% photodetector quantum efficiency, half mark/half space digital transmission, 850nm lightwave and using Gaussian approximation, the minimum required optical power to achieve 10^{-9} BER is:

$$P_{avMIN} = 12\frac{hc}{\lambda}B\ Z = 12\ (2.3\cdot10^{-19})$$

$$200\cdot10^{6}\ 1625 = 897nW = -30.5dBm,$$

where h is Planck's Constant, c is the speed of light, λ is the wavelength. The minimum input current to the NE5212A, at this input power is:

$$I_{avMIN} = qP_{avMIN}\frac{\lambda}{hc}$$

$$= \frac{897\cdot10^{-9}\cdot1.6\cdot10^{-19}}{2.3\cdot10^{-19}}$$

$$= 624nA$$

Choosing the maximum peak overload current of I_{avMAX}=120μA, the maximum mean optical power is:

$$P_{avMAX} = \frac{hcI_{avMAX}}{\lambda q} = \frac{2.3\cdot10^{-19}(120\cdot10^{-6})}{1.6\cdot10^{-19}}$$

$$= 172\mu W \text{ or } -7.6dBm$$

Thus the optical dynamic range, D_O is:

$D_O = P_{avMAX} - P_{avMIN}$ = -30.5 -(-7.6) = 22.8dB.

This represents the maximum limit attainable with the NE5212A operating at 200MHz bandwidth, with a half mark/half space digital transmission at 820nm wavelength.

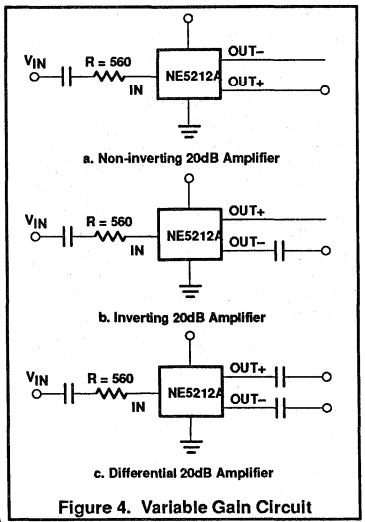


Figure 4. Variable Gain Circuit

APPLICATION INFORMATION

Package parasitics, particularly ground lead inductances and parasitic capacitances, can significantly degrade the frequency response. Since the NE5212A has differential outputs which can feed back signals to the input by parasitic package or board layout capacitances, both peaking and attenuating type frequency response shaping is possible. Constructing the board layout so that Ground 1 and Ground 2 have very low impedance paths has produced the best results. This was accomplished by adding a ground-plane stripe underneath the device connecting Ground 1, Pins 8–11, and Ground 2, Pins 1 and 2 on opposite ends of the SO14 package. This ground-plane stripe also provides isolation between the output return currents flowing to either V_{CC2} or Ground 2 and the input photodiode currents to flowing to Ground 1. Without this ground-plane stripe and with large lead inductances on the board, the part may be unstable and oscillate near 800MHz. The easiest way to realize that the part is not functioning normally is to measure the DC voltages at the outputs. If they are not close to their quiescent values of 3.3V (for a 5V supply), then the circuit may be oscillating. Input pin layout necessitates that the photodiode be physically very close to the input and Ground 1. Connecting Pins 3 and 5 to Ground 1 will tend to shield the input but it will also tend to increase the capacitance on the input and slightly reduce the bandwidth.

As with any high-frequency device, some precautions must be observed in order to

enjoy reliable performance. The first of these is the use of a well-regulated power supply. The supply must be capable of providing varying amounts of current without significantly changing the voltage level. Proper supply bypassing requires that a good quality 0.1µF high-frequency capacitor be inserted between V_{CC1} and V_{CC2}, preferably a chip capacitor, as close to the package pins as possible. Also, the parallel combination of 0.1µF capacitors with 10µF tantalum capacitors from each supply, V_{CC1} and V_{CC2}, to the ground plane should provide adequate decoupling. Some applications may require an RF choke in series with the power supply line. Separate analog and digital ground leads must be maintained and printed circuit board ground plane should be employed whenever possible.

BASIC CONFIGURATION

A trans resistance amplifier is a current-to-voltage converter. The forward transfer function then is defined as voltage out divided by current in, and is stated in ohms. The lower the source resistance, the higher the gain. The NE5212A has a differential transresistance of 14kΩ typically and a single-ended transresistance of 7kΩ typically. The device has two outputs: inverting and non-inverting. The output voltage in the differential output mode is twice that of the output voltage in the single-ended mode. Although the device can be used without coupling capacitors, more care is required to avoid upsetting the internal bias nodes of the device. Figure 4 shows some basic configurations.

VARIABLE GAIN

Figure 5 shows a variable gain circuit using the NE5212A and the NE5230 low voltage op amp. This op amp is configured in a non-inverting gain of five. The output drives the gate of the SD210 DMOS FET. The series resistance of the FET changes with this output voltage which in turn changes the gain of the NE5212A. This circuit has a distortion of less than 1% and a 25dB range, from -42.2dBm to -15.9dBm at 50MHz, and a 45dB range, from -60dBm to -14.9dBm at 10MHz with 0 to 1V of control voltage at V_{CC}.

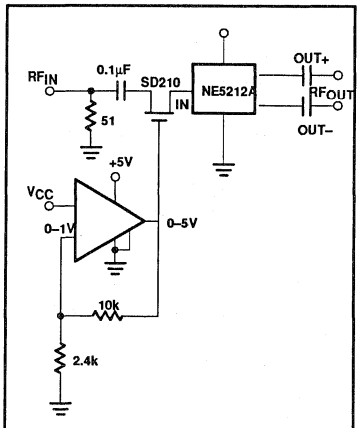


Figure 5. Variable Gain Circuit

16MHZ CRYSTAL OSCILLATOR

Figure 6 shows a 16MHz crystal oscillator operating in the series resonant mode using the NE5212A. The non-inverting input is fed back to the input of the NE5212A in series with a 2pF capacitor. The output is taken from the inverting output.

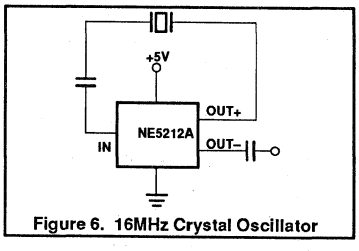


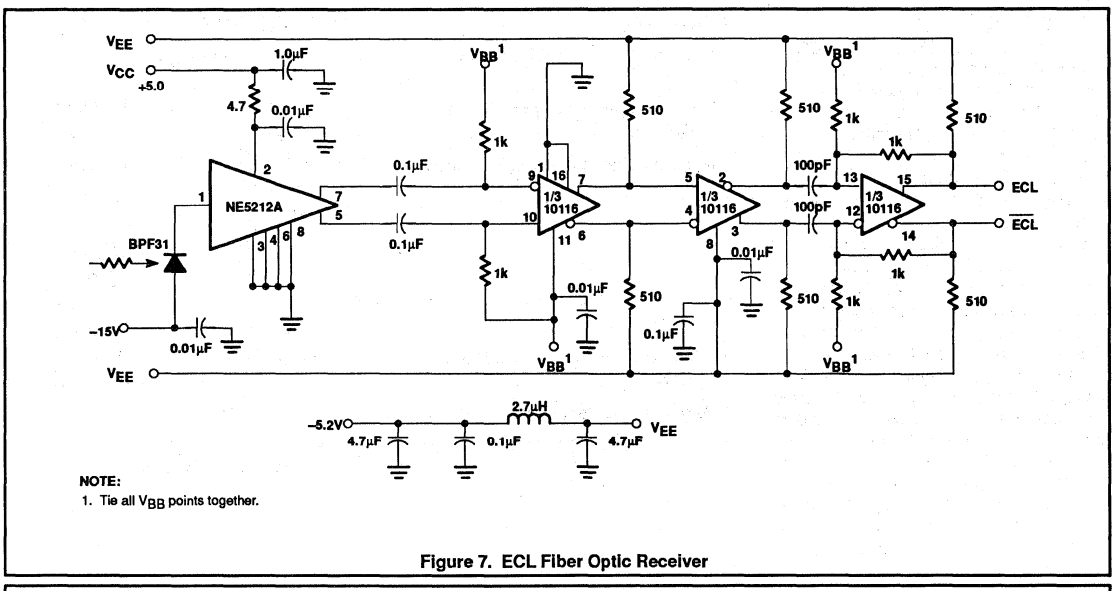
Figure 6. 16MHz Crystal Oscillator

DIGITAL FIBER OPTIC RECEIVER

Figures 7 and 8 show a fiber optic receiver using off-the-shelf components.

The receiver shown in Figure 7 uses the NE5212A, the Signetics 10116 ECL line receiver, and Philips/Amperex BPF31 PIN diode. The circuit is a capacitor-coupled receiver and utilizes positive feedback in the last stage to provide the hysteresis. The amount of hysteresis can be tailored to the individual application by changing the values of the feedback resistors to maintain the desired balance between noise immunity and sensitivity. At room temperature, the circuit operates at 50Mbaud with a BER of 10E-10 and over the automotive temperature range at 40Mbaud with a BER of 10E-9. Higher speed experimental diodes have been used to operate this circuit at 220Mbaud with a BER of 10E-10.

Figure 8 depicts a TTL receiver using the NE5212A and the NE5214 fast amplifier system along with the Philips/Amperex PIN diode. The system shown is optimized for 50 Mb/s Non Return to Zero (NRZ) data. A link status indication is provided along with a jamming function when the input level is below a user-programmable threshold level.



NOTE:
1. Tie all V_{BB} points together.

Figure 7. ECL Fiber Optic Receiver

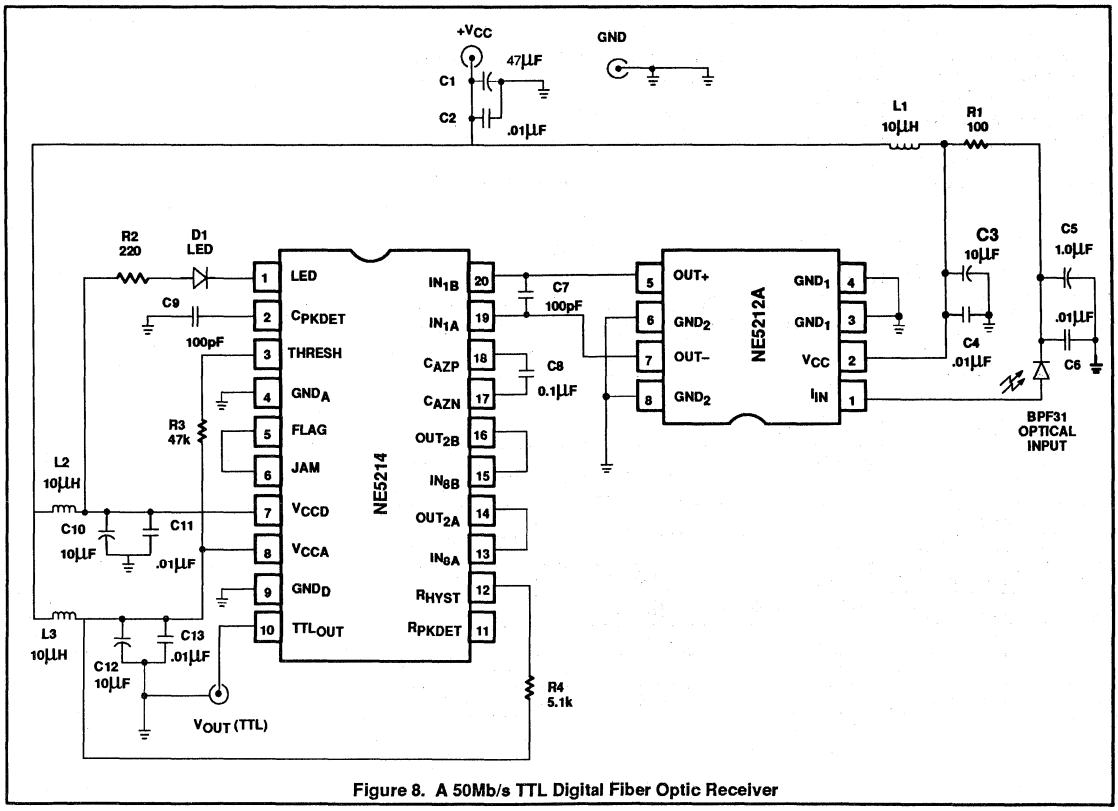


Figure 8. A 50Mb/s TTL Digital Fiber Optic Receiver

Postamplifier with link status indicator — NE/SA5214

DESCRIPTION

THE NE/SA5214 is a 75MHz postamplifier system designed to accept low level high-speed signals. These signals are converted into a TTL level at the output. The NE5214 can be DC coupled with the previous transimpedance stage using NE5210, NE5211 or NE5212 transimpedance amplifiers. This "system on a chip" features an auto-zeroed first stage with noise shaping, a symmetrical limiting second stage, and a matched rise/fall time TTL output buffer. The system is user-configurable to provide noise filtering, adjustable input thresholds and hysteresis. The threshold capability allows the user to maximize signal-to-noise ratio, insuring a low Bit Error Rate (BER). An Auto-Zero loop can be used to minimize the number of external coupling capacitors to one. A signal absent flag indicates when signals are below threshold. Additionally, the low signal condition forces the overall TTL output to a logical Low level. User interaction with this "jamming" system is available. The NE/SA5214 is packaged in a standard 20-pin surface-mount package and typically consumes 42mA from a standard 5V supply. The NE/SA5214 is designed as a companion to the NE/SA5211/5212 transimpedance amplifiers. These differential preamplifiers may be directly coupled to the post-amplifier inputs. The NE/SA5212/5214 or NE/SA5211/5214 combinations convert nanoamps of photodetector current into standard digital TTL levels.

FEATURES

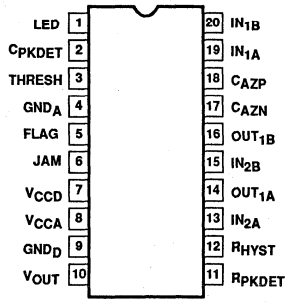
- Postamp for the NE/SA5211/5212 preamplifier family
- Wideband operation: typical 75MHz (100MBaud NRZ)
- Interstage filtering/equalization possible
- Single 5V supply
- Low signal flag
- Low signal output disable
- Link status threshold and hysteresis programmable
- LED driver (normally ON with above threshold signal)
- Fully differential for excellent PSRR
- Auto-zero loop for DC offset cancellation
- 2kV ElectroStatic Discharge (ESD) protection

APPLICATIONS

- Fiber optics
- Communication links in Industrial and/or Telecom environment with high EMI/RFI
- Local Area Networks (LAN)
- Metropolitan Area Networks (MAN)
- Synchronous Optical Networks (SONET)
- RF limiter

PIN CONFIGURATION

D[1] Package



TOP VIEW

NOTE:
1. SOL – Released in large SO package only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SOL	0 to +70°C	NE5214D
20-Pin Plastic SOL	-40°C to +85°C	SA5214D

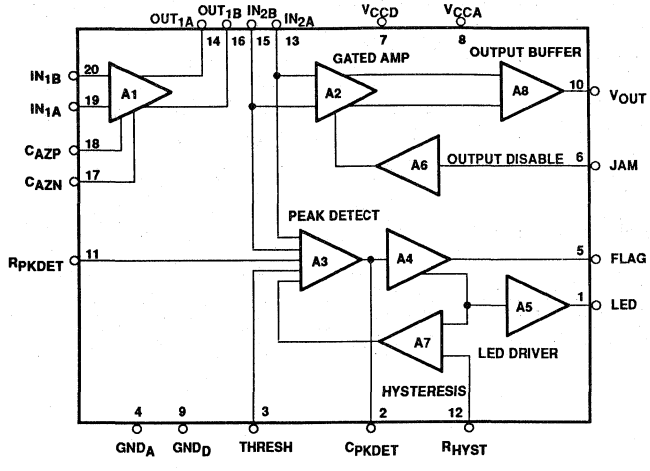
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNIT
		NE5214	SA5214	
V_{CCA}	Power supply	+6	+6	V
V_{CCD}	Power supply	+6	+6	V
T_A	Operating ambient temperature range	0 to +70	-40 to +85	°C
T_J	Operating junction temperature range	-55 to +150	-55 to +150	°C
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C
P_D	Power dissipation	300	300	mW
V_{IJ}	Jam input voltage	-0.5 to 5.5	-0.5 to 5.5	V

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	LED	Output for the LED driver. Open collector output transistor with 125Ω series limiting resistor. An above threshold signal turns this transistor ON.
2	C_{PKDET}	Capacitor for the peak detector. The value of this capacitor determines the detector response time to the signal, supplementing the internal 10pF capacitor.
3	THRESH	Peak detector threshold resistor. The value of this resistor determines the threshold level of the peak detector.
4	GND_A	Device analog ground pin.
5	FLAG	Peak detector digital output. When this output is LOW, there is data present above the threshold. This pin is normally connected to the JAM pin and has a TTL fanout of two.
6	JAM	Input to inhibit data flow. Sending the pin HIGH forces TTL DATA OUT ON, Pin 10, LOW. This pin is normally connected to the FLAG pin and is TTL-compatible.
7	V_{CCD}	Power supply pin for the digital portion of the chip.
8	V_{CCA}	Power supply pin for the analog portion of the chip.
9	GND_D	Device digital ground pin.
10	V_{OUT}	TTL output pin with a fanout of five.
11	R_{PKDET}	Peak detector current resistor. The value of this resistor determines the amount of discharge current available to the peak detector capacitor, C_{PKDET}.
12	R_{HYST}	Peak detector hysteresis resistor. The value of this resistor determines the amount of hysteresis in the peak detector.
13	IN_{2A}	Non-inverting input to amplifier A2.
14	OUT_{1A}	Non-inverting output of amplifier A1.
15	IN_{2B}	Inverting input to amplifier A2.
16	OUT_{1B}	Inverting output of amplifier A1.
17	C_{AZN}	Auto-Zero capacitor pin (Negative terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
18	C_{AZP}	Auto-Zero capacitor pin (Positive terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
19	IN_{1A}	Non-inverting input of the preamp A1.
20	IN_{1B}	Inverting input of the preamp A1.

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING		UNIT
		NE5214	SA5214	
V_{CCA}	Supply voltage	4.75 to 5.25	4.75 to 5.25	V
V_{CCD}	Power supply	4.75 to 5.25	4.75 to 5.25	V
T_A	Ambient temperature range	0 to +70	-40 to +85	°C
T_J	Operating junction temperature range	0 to +95	-40 to +110	°C
P_D	Power dissipation	250	250	mW

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over the operating temperature range at V_{CCA}=V_{CCD}=+5.0V unless otherwise specified. Typical data applies at V_{CCA}=V_{CCD}=+5.0V and T_A=25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE5214			SA5214			
			Min	Typ	Max	Min	Typ	Max	
I_{CCA}	Analog supply current			30	36		30	37.2	mA
I_{CCD}	Digital supply current (TTL, Flag, LED)			10	13.3		10	13.5	mA
V_{I1}	A1 input bias voltage (+/- inputs)		3.16	3.4	3.63	3.13	3.4	3.65	V
V_{O1}	A1 output bias voltage (+/- outputs)		3.17	3.8	4.45	3.10	3.8	4.50	V
A_{V1}	A1 DC gain (without Auto-Zero)			30			30		dB
$A1_{PSRR}$	A1 PSRR (V_{CCA}, V_{CCD})	V_{CCA}=V_{CCD}=4.75 to 5.25V		60			60		dB
$A1_{CMRR}$	A1 CMRR	ΔV_{CM}=200mV		60			60		dB
V_{I2}	A2 input bias voltage (+/- inputs)		3.59	3.7	3.85	3.56	3.7	3.86	V
V_{OH}	High-level TTL output voltage	I_{OH}=-200µA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level TTL output voltage	I_{OL}=8mA		0.3	0.4		0.3	0.4	V
I_{OH}	High-level TTL output current	V_{OUT}=2.4V		-40	-26		-40	-24.4	mA
I_{OL}	Low-level TTL output current	V_{OUT}=0.4V	8.0	30		7.0	30		mA
I_{OS}	Short-circuit TTL output current	V_{OUT}=0.0V		-95			-95		mA
V_{THRESH}	Threshold bias voltage	Pin 3 Open		0.75			0.75		V
V_{RPKDET}	RPKDET	Pin 11 Open		0.72			0.72		V
V_{RHYST}	RHYST bias voltage	Pin 12 Open		0.72			0.72		V
V_{IHJ}	High-level jam input voltage		2.0			2.0			V
V_{ILJ}	Low-level jam input voltage				0.8			0.8	V
I_{IHJ}	High-level jam input current	V_{IJ}=2.7V			20			30	µA
I_{ILJ}	Low-level jam input current	V_{IJ}=0.4V	-450	-240		-485	-240		µA
V_{OHF}	High-level flag output voltage	I_{OH}=-80µA	2.4	3.8		2.4	3.8		V
V_{OLF}	Low-level flag output voltage	I_{OL}=3.2mA		0.33	0.4		0.33	0.4	V
I_{OHF}	High-level flag output current	V_{OUT}=2.4V		-18	-5.3		-18	-5	mA
I_{OLF}	Low-level flag output current	V_{OUT}=0.4V	3.6	10		3.25	10		mA
I_{SCF}	Short-circuit flag output current	V_{OUT}=0.0V	-60	-40	-25	-61	-40	-26	mA
I_{LEDH}	LED ON maximum sink current	V_{LED}=3.0V	13	22	80	8	22	80	mA

AC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE5214			SA5214			
			Min	Typ	Max	Min	Typ	Max	
f_{OP}	Maximum operating frequency	Test circuit	60	75		60	75		MHz
BW_{A1}	Small signal bandwidth (differential OUT_1/IN_1)	Test circuit		75			75		MHz
V_{INH}	Maximum Functional A1 input signal (single ended)	Test Circuit		1.6			1.6		V_{P-P}
V_{INL}	Minimum Functional A1 input signal (single ended)	Test CIrcuit[1]		12			12		mV_{P-P}
R_{IN1}	Input resistance (differential at IN_1)			1200			1200		Ω
C_{IN1}	Input capacitance (differential at IN_1)			2			2		pF
R_{IN2}	Input resistance (differential at IN_2)			1200			1200		Ω
C_{IN2}	Input capacitance (differential at IN_2)			2			2		pF
R_{OUT1}	Output resistance (differential at OUT_1)			25			25		Ω
C_{OUT1}	Output capacitance (differential at OUT_1)			2			2		pF
V_{HYS}	Hysteresis voltage	Test circuit		3			3		mV_{P-P}
V_{THR}	Threshold voltage range (FLAG ON)	Test circuit, @ 50MHz R_{RHYST}=5k R_{THRESH}=47k		12			12		mV_{P-P}
t_{TLH}	TTL Output Rise Time 20% to 80%	Test Circuit		1.3			1.3		ns
t_{THL}	TTL Output Fall Time 80% to 20%	Test Circuit		1.2			1.2		ns
t_{RFD}	t_{TLH}/t_{THL} mismatch			0.1			0.1		ns
t_{PWD}	Pulse width distortion of output	50mV_{P-P}, 1010. . .input Distortion= $\frac{T_H-T_L}{T_H+T_L} 10^2$		2.5			2.5		%

NOTES:

1. The NE/SA5214 is capable of detecting a much lower input level. Operation under 12mV_{P-P} cannot be guaranteed by present day automatic testers.

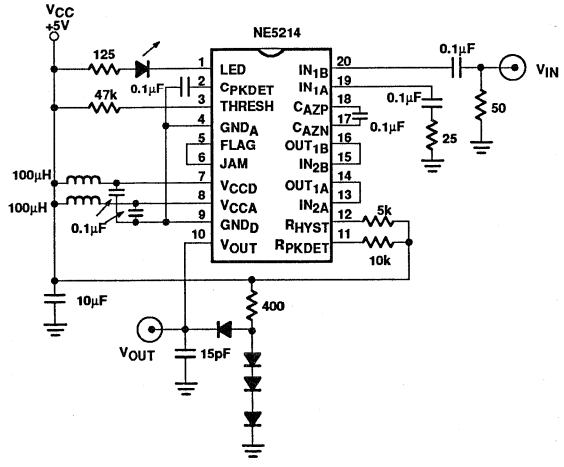
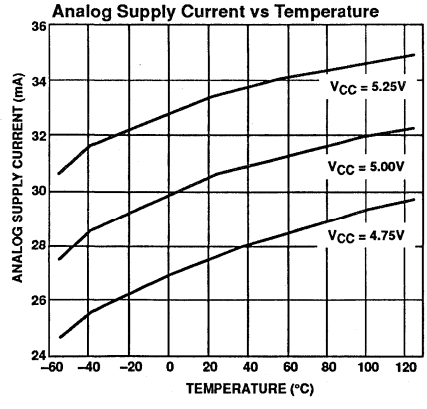
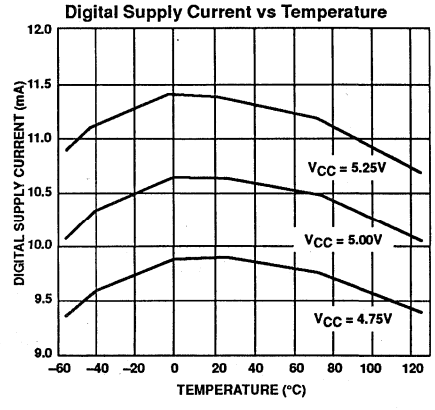
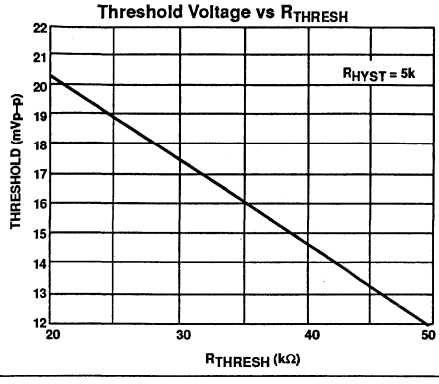


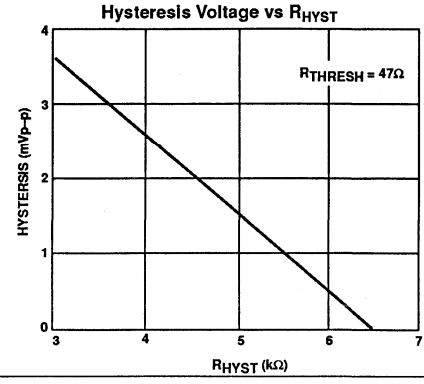
Figure 1. AC Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS









THEORY OF OPERATION AND APPLICATION INFORMATION

The NE 5214 postamplifier system is a highly integrated chip that provides up to 60dB of gain at 60MHz, to bring mV level signals up to TTL levels.

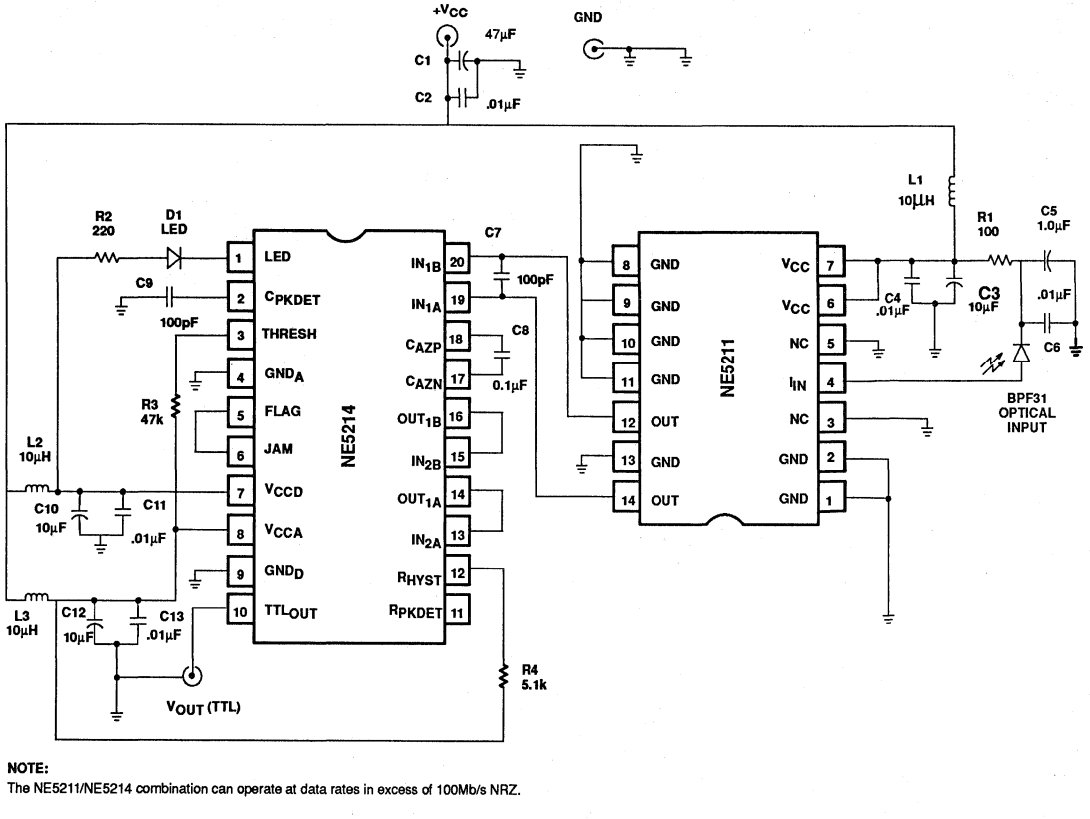
The NE5214 contains eight amplifier blocks (see Block Diagram). The main signal path is made up of a cascade of limiting stages: A1, A2 and A8. The A3-A4-A7 path performs a wideband full-wave rectification of the input signal with adjustable hysteresis and decay times. It outputs a TTL HIGH on the "FLAG" output (Pin 5) when the input is below a user adjustable threshold. An on-chip LED driver turns the external LED to the ON state when the input signal is above the threshold. In a typical application the "FLAG" output is tied back to the "JAM" input; this forces the TTL data OUT into a LOW state when no signal is present at the input.

An auto zero loop allows the NE5214 to be directly connected to a transimpedance amplifier such as the NE5210, NE5211, or NE5212 without coupling capacitors. This auto-zero loop cancels the transimpedance amplifier's DC offset, the NE5214 A1 offset, and the data-dependent offset in the PIN diode/transimpedance amplifier combination. For more information on the NE5214 Theory of Operation, please refer to paper titled "A Low Cost 100 MBaud Fiber-Optic Receiver" by W. Mack et al.

A typical application of the NE5214 postamplifier is depicted in Figure 2. The system uses the NE5211 transimpedance amplifier which has a 28k differential transimpedance gain and a -3dB bandwidth of 140MHz. This typical application is optimized for a 50 Mb/s Non Return to Zero (NRZ) bit stream.

As the system's gain bandwidth product is very high, it is crucial to employ good RF design and printed circuit board layout techniques to prevent the system from becoming unstable.

For more information on this application, please refer to AB 1432.



NOTE:
The NE5211/NE5214 combination can operate at data rates in excess of 100Mb/s NRZ.

Figure 2. A 50Mb/s Fiber Optic Receiver

Postamplifier with link status indicator — NE/SA5217

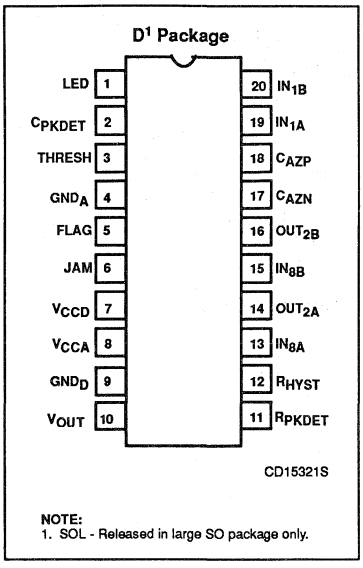
DESCRIPTION

The NE/SA5217 is a 75MHz postamplifier system designed to accept low level high-speed signals. These signals are converted into a TTL level at the output. The NE5217 can be DC coupled with the previous transimpedance stage using NE5210, NE5211 or NE5212A transimpedance amplifiers. The main difference between the NE5217 and the NE5214 is that the NE5217 does not make the output of A1 and input of A2 accessible; instead, it brings out the output of A2 and the input of A8 thus activating the on-chip Schmitt trigger function by connecting two external capacitors. The result is that a much longer string of 1s and 0s, in the bit stream, can be tolerated. This "system on a chip" features an auto-zeroed first stage with noise shaping, a symmetrical limiting second stage, and a matched rise/fall time TTL output buffer. The system is user-configurable to provide adjustable input threshold and hysteresis. The threshold capability allows the user to maximize signal-to-noise ratio, thereby insuring a low Bit Error Rate (BER). An auto-zero loop can be used to replace two input coupling capacitors with a single Auto Zero (AZ) capacitor. A signal absent flag indicates when signals are below threshold. The low signal condition forces the TTL output to the last logic state. User interaction with this "jamming" system is available. The NE/SA5217 is packaged in a standard 20-pin surface-mount package and typically consumes 40mA from a standard 5V supply. The NE/SA5217 is designed as a companion to the NE/SA5211/5212A and NE5210 transimpedance amplifiers. These differential preamplifiers may be directly coupled to the postamplifier inputs. The NE5210/5217, NE/SA5211/5217 or NE/SA5212A/5217 combinations convert nanoamps of photodetector current into standard digital TTL levels.

FEATURES

- Postamp for the NE/SA5211/5212A. NE5210 preamplifier family
- Wideband operation: typical 75MHz (150MBaud NRZ)
- Interstage filtering/equalization possible
- Single 5V supply
- Low signal flag
- Output disable
- Link status threshold and hysteresis programmable
- LED driver (normally ON with above threshold signal)
- Fully differential for excellent PSRR
- Auto-zero loop for DC offset cancellation
- 2kV ElectroStatic Discharge (ESD) protection

PIN CONFIGURATION



NOTE:
1. SOL - Released in large SO package only.

APPLICATIONS

- Fiber optics
- Communication links in Industrial and/or Telecom environment with high EMI/RFI
- Local Area Networks (LAN)
- Synchronous Optical Networks (SONET) STS-1
- RF limiter
- Good for 2^{23} -1 pseudo random bit stream

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SOL	0 to +70°C	NE5217D
20-Pin Plastic SOL	-40 to +85°C	SA5217D

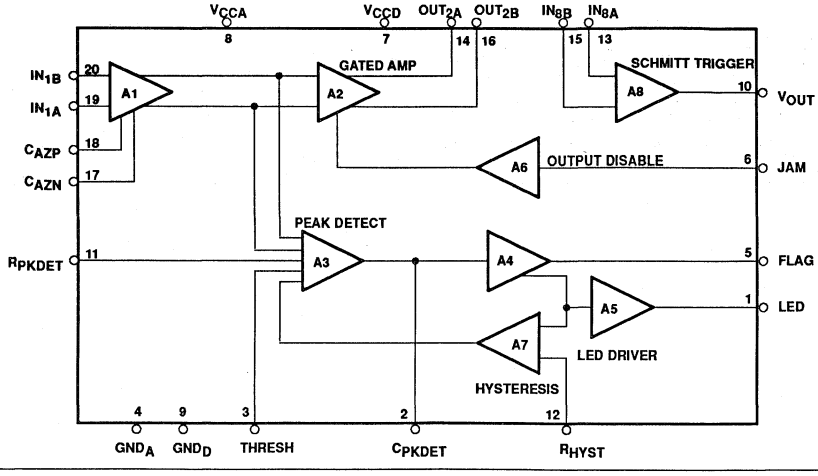
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNIT
		NE5214	SA5214	
V_{CCA}	Power supply	+6	+6	V
V_{CCD}	Power supply	+6	+6	V
T_A	Operating ambient temperature range	0 to +70	-40 to +85	°C
T_J	Operating junction temperature range	-55 to +150	-55 to +150	°C
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C
P_D	Power dissipation	1.4	1.4	W
V_{IJ}	Jam input voltage	-0.5 to 5.5	-0.5 to 5.5	V

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	LED	Output for the LED driver. Open collector output transistor with 125Ω series limiting resistor. An above threshold signal turns this transistor ON.
2	C_{PKDET}	Capacitor for the peak detector. The value of this capacitor determines the detector response time to the signal, supplementing the internal 10pF capacitor.
3	THRESH	Peak detector threshold resistor. The value of this resistor determines the threshold level of the peak detector.
4	GND_A	Device analog ground pin.
5	FLAG	Peak detector digital output. When this output is LOW, there is data present above the threshold. This pin is normally connected to the JAM pin and has a TTL fanout of two.
6	JAM	Input to inhibit data flow. Sending the pin HIGH forces TTL DATA OUT ON, Pin 10, LOW. This pin is normally connected to the FLAG pin and is TTL-compatible.
7	V_{CCD}	Power supply pin for the digital portion of the chip.
8	V_{CCA}	Power supply pin for the analog portion of the chip.
9	GND_D	Device digital ground pin.
10	V_{OUT}	TTL output pin with a fanout of five.
11	R_{PKDET}	Peak detector current resistor. The value of this resistor determines the amount of discharge current available to the peak detector capacitor, C_{PKDET}.
12	R_{HYST}	Peak detector hysteresis resistor. The value of this resistor determines the amount of hysteresis in the peak detector.
13	IN_{8A}	Non-inverting input to amplifier A8.
14	OUT_{2A}	Non-inverting output of amplifier A2.
15	IN_{8B}	Inverting input to amplifier A8.
16	OUT_{2B}	Inverting output of amplifier A2.
17	C_{AZN}	Auto-Zero capacitor pin (Negative terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
18	C_{AZP}	Auto-Zero capacitor pin (Positive terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
19	IN_{1A}	Non-inverting input of the preamp A1.
20	IN_{1B}	Inverting input of the preamp A1.

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING		UNIT
		NE5217	SA5217	
V_{CCA}	Power supply	4.5 to 5.5	4.5 to 5.5	V
V_{CCD}	Power supply	4.5 to 5.5	4.5 to 5.5	V
T_A	Ambient temperature range	0 to +70	-40 to +85	°C
T_J	Operating junction temperature range	0 to +95	-40 to +110	°C
P_D	Power dissipation	300	300	mW

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE5217			SA5217			
			Min	Typ	Max	Min	Typ	Max	
I_{CCA}	Analog supply current			30	36		30	37.2	mA
I_{CCD}	Digital supply current (TTL, Flag, LED)			10	13.3		10	13.5	mA
V_{I1}	A1 input bias voltage (A,B inputs)		3.16	3.4	3.63	3.13	3.4	3.65	V
V_{O2}	A1 output bias voltage (A,B outputs)		3.17	3.8	4.45	3.10	3.8	4.50	V
V_{I8L}	A8 input bias voltage Low (A,B inputs)		3.40	3.55	3.68	3.40	3.55	3.68	V
V_{I8H}	A8 input bias voltage High (A,B inputs)		3.70	3.91	4.10	3.68	3.91	4.12	V
V_{OH}	High-level TTL output voltage	I_{OH}=-200µA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level TTL output voltage	I_{OL}=8mA		0.3	0.4		0.3	0.4	V
I_{OH}	High-level TTL output current	V_{OUT}=2.4V		-40	-26		-40	-24.4	mA
I_{OL}	Low-level TTL output current	V_{OUT}=0.4V	8.0	30		7.0	30		mA
I_{OS}	Short-circuit TTL output current	V_{OUT}=0.0V		-95			-95		mA
V_{THRESH}	Threshold bias voltage	Pin 3 Open		0.75			0.75		V
V_{RPKDET}	RPKDET	Pin 11 Open		0.72			0.72		V
V_{RHYST}	RHYST bias voltage	Pin 12 Open		0.72			0.72		V
V_{IHJ}	High-level jam input voltage		2.0			2.0			V
V_{ILJ}	Low-level jam input voltage				0.8			0.8	V
I_{IHJ}	High-level jam input current	V_{IJ}=2.7V			20			30	µA
I_{ILJ}	Low-level jam input current	V_{IJ}=0.4V	-450	-240		-485	-240		µA
V_{OHF}	High-level flag output voltage	I_{OH}=-80µA	2.4	3.8		2.4	3.8		V
V_{OLF}	Low-level flag output voltage	I_{OL}=3.2mA		0.33	0.4		0.33	0.4	V
I_{OHF}	High-level flag output current	V_{OUT}=2.4V		-18	-5.3		-18	-5	mA
I_{OLF}	Low-level flag output current	V_{OUT}=0.4V	3.6	10		3.25	10		mA
I_{SCF}	Short-circuit flag output current	V_{OUT}=0.0V	-60	-40	-25	-61	-40	-26	mA
I_{LEDH}	LED ON maximum sink current	V_{LED}=3.0V	13	22	80	8	22	80	mA

AC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE5217			SA5217			
			Min	Typ	Max	Min	Typ	Max	
f_{OP}	Maximum operating frequency	Test circuit	60	75		60	75		MHz
V_{INH}	Maximum Functional A1 input signal (single ended)	Test Circuit		1.6			1.6		V_{P-P}
V_{INL}	Minimum Functional A1 input signal (single-ended)	Test CIrcuit		6			6		mV_{P-P}
	Minimum Functional A1 input signal (differential)			3			3		mV_{P-P}
	Minimum input sensitivity for output BER $\leq 10^{-9}$ (single-ended)	PRBS = $2^{23}-1$		9			9		mV_{P-P}
	Minimum input sensitivity for output BER $\leq 10^{-9}$ (differential)			4.5			4.5		mV_{P-P}
R_{IN1}	Input resistance (differential at IN_1)			1200			1200		Ω
C_{IN1}	Input capacitance (differential at IN_1)			2			2		pF
R_{IN8}	Input resistance (differential at IN_2)			2000			2000		Ω
C_{IN2}	Input capacitance (differential at IN_2)			2			2		pF
R_{OUT2}	Output resistance (differential at OUT_2)			25			25		Ω
C_{OUT2}	Output capacitance (differential at OUT_2)			2			2		pF
V_{HYS}	Hysteresis voltage range (single-ended)	Test circuit, $T_A = 25°C$		10			10		mV_{P-P}
	Hysteresis voltage range (differential)	R_{RHYST}=5k R_{THRESH}=33k		5			5		mV_{P-P}
V_{THR}	Threshold voltage (single-ended)	(FLAG Low) Test circuit, @ 50MHz		19			19		mV_{P-P}
	Threshold voltage (differential)	R_{RHYST}=4k R_{THRESH}=33k		9.5			9.5		mV_{P-P}
t_{TLH}	TTL Output Rise Time 20% to 80%	Test Circuit		1.3			1.3		ns
t_{THL}	TTL Output Fall Time 80% to 20%	Test Circuit		1.2			1.2		ns
t_{RFD}	t_{TLH}/t_{THL} mismatch			0.1			0.1		ns
t_{PWD}	Pulse width distortion of output	50mV_{P-P}, 1010. . .input Distortion = $\frac{T_H - T_L}{T_H + T_L} 10^2$		TBD			TBD		%

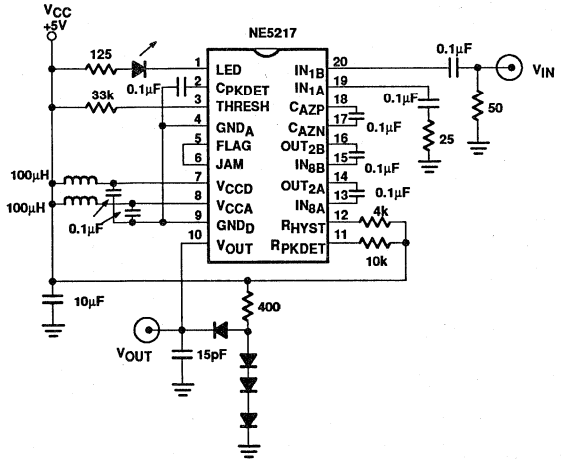
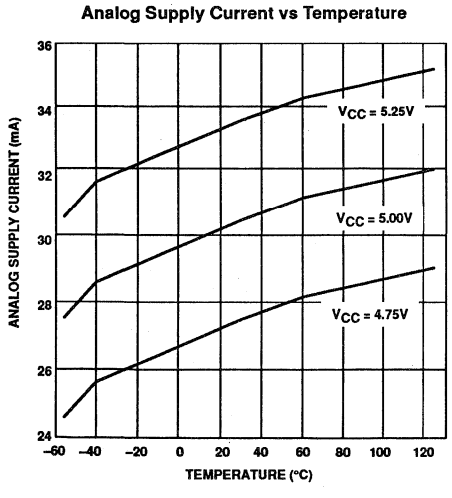
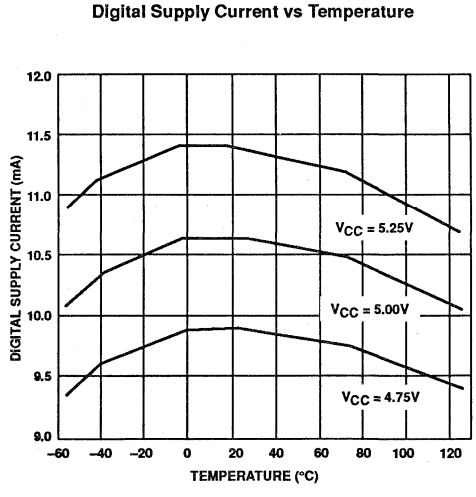


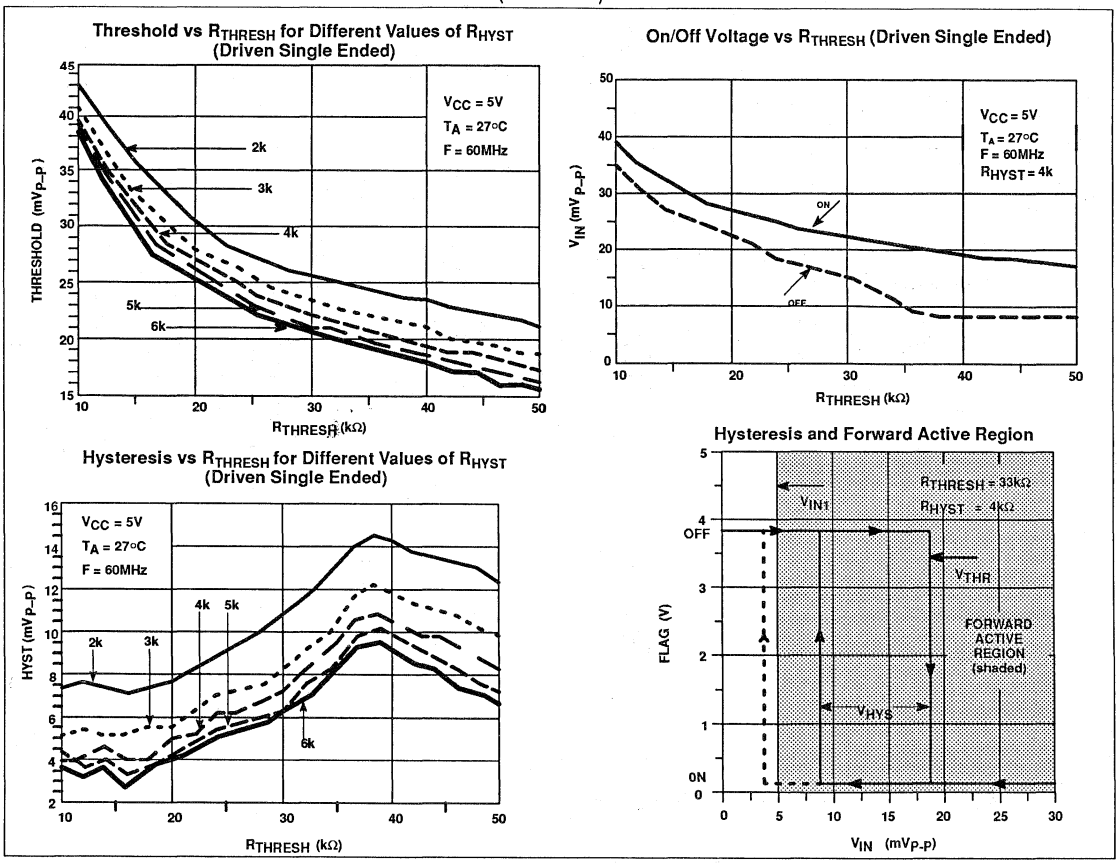
Figure 1. AC Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS





TYPICAL PERFORMANCE CHARACTERISTICS (continued)



THEORY OF OPERATION AND APPLICATION

The NE5217 postamplifier is a highly integrated chip that provides up to 60dB of gain at 60MHz, to bring mV level signals up to TTL levels.

The NE5217 contains eight amplifier blocks (see Block Diagram). The main signal path is made up of a cascade of limiting stages: A1, A2 and A8. The A3-A4-A7 path performs a wideband full-wave rectification of the input signal with adjustable hysteresis and decay times. It outputs a TTL High on the "FLAG" output (Pin 5) when the input is below a user adjustable threshold. An on-chip LED driver turns the external LED to the On state when the input signal is above the threshold. In a typical application the "FLAG" output is tied back tot he "JAM" input; forcing the "JAM" input to TTL High will latch the TTL Data Out at the last logical state.

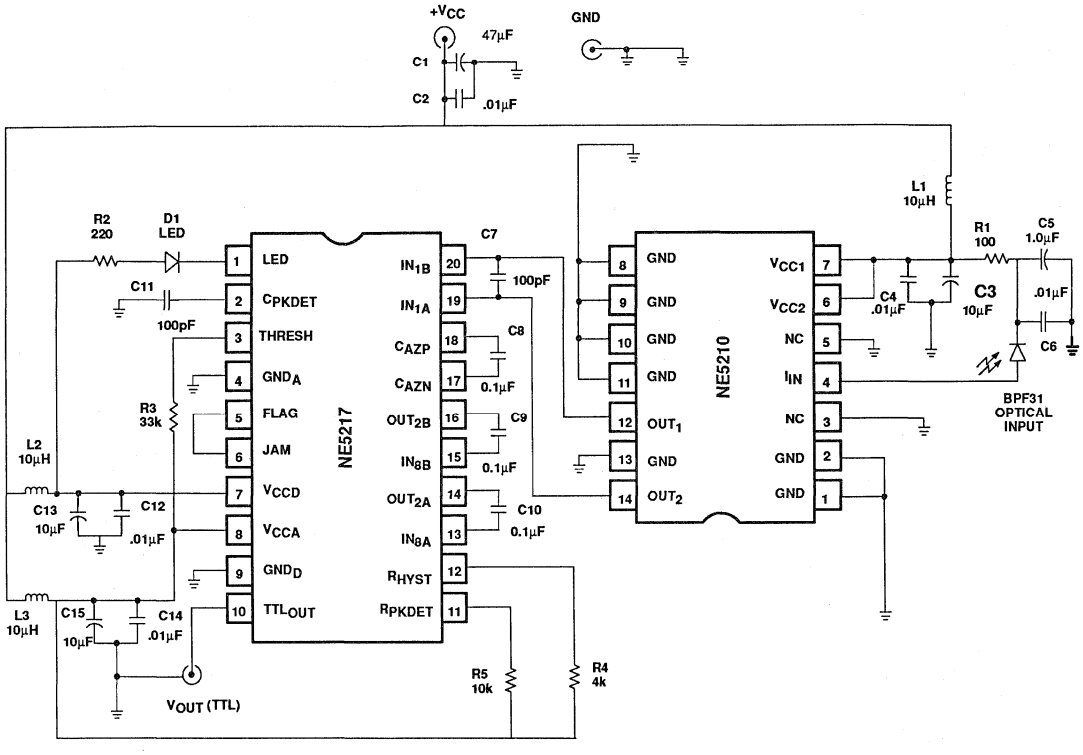
Threshold voltage and hysteresis voltage range are adjustable with resistors R_{THRESH} and R_{HYST}. The typical values given in the data sheet will result in performance shown in the graph "Hysteresis and Forward Active Region". A minority of parts may be sensitive enough that FLAG High (Off) occurs below the minimum functional input signal level, V_{IN1}. This condition is shown by the dotted line in the graph. Such parts may require adjustment of R_{THRESH} if it is important to guarantee that an output signal is present for the full hysteresis range. If this is not important, R_{THRESH} may be adjusted to give a FLAG Low for lower level input signals.

An auto-zero loop allows the NE5217 to be directly connected to a transimpedance amplifier such as the NE5210, NE5211, or NE5212A without coupling capacitors. This auto-zero loop cancels the transimpedance amplifier's DC offset, the NE5217 A1 offset, and the data-dependent offset in the PIN diode/transimpedance amplifier combination. For more information on the NE5217 Theory of Operation, please refer to paper titled "A Low Cost 100MBaud Fiber Optic Receiver" by W. Mack, et. al.

A typical application of the NE5217 postamplifier is depicted in Figure 2. The system uses the NE5211 transimpedance amplifier which has a 28k differential transimpedance gain and a -3dB bandwidth of 140MHz. this typical application is optimized for a 50Mb/s Non Return to Zero (NRZ) bit stream.

As the system's gain bandwidth product is very high, it is crucial to employ good RF design and printed circuit board layout techniques to prevent the system from becoming unstable.

For more information on this application, please refer to Application Brief AB1432.



NOTE:
THE NE5210/NE5217 combination can operate at data rates in excess of 100Mb/s NRZ

Figure 2. A 50Mb/s Fiber Optic Receiver

Low-power FDDI transimpedance amplifier — SA5222

DESCRIPTION

The NE/SA5222 is a low-power, wide-band, low noise transimpedance amplifier with differential outputs, optimized for signal recovery in FDDI fiber optic receivers. The part is also suited for many other RF and fiber optic applications as a general purpose gain block.

FEATURES

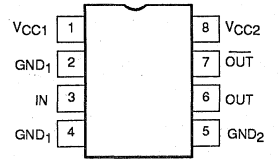
- Extremely low noise: $2.0pA/\sqrt{Hz}$
- Single 5V supply
- Low supply current: 9mA
- Large bandwidth: 165MHz
- Differential outputs
- Low output offset
- Low input/output impedances
- High power-supply-rejection ratio: 55dB
- Tight transresistance control
- High input overload: 115µA
- ESD protected

APPLICATIONS

- FDDI preamp
- Current-to-voltage converters
- Wide-band gain block
- Medical and scientific instrumentation
- Sensor preamplifiers
- Single-ended to differential conversion
- Low noise RF amplifiers
- RF signal processing

PIN DESCRIPTION

D Package



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	-40 to +85°C	SA5222D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
$V_{CC1,2}$	Power supply voltage	6	V
T_A	Ambient temperature range	-40 to +85	°C
T_J	Junction temperature range	-55 to +150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
P_D	Power dissipation T_A = 25°C (still air)[1]	0.78	W
I_{INMAX}	Maximum input current	5	mA

NOTE:

1. Maximum power dissipation is determined by the operating ambient temperature and the thermal resistance θ_{JA} = 158°C/W. Derate 6.2mW/°C above 25°C.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
$V_{CC1,2}$	Power supply voltage	4.5 to 5.5	V
T_A	Ambient temperature range: SA grade	-40 to +85	°C
T_J	Junction temperature range: SA grade	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

Typical data and Min and Max limits apply at T_A = 25°C, and $V_{CC1} = V_{CC2}$ = +5V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SA5222			UNIT
			Min	Typ	Max	
V_{IN}	Input bias voltage		1.3	1.55	1.8	V
$V_{O\pm}$	Output bias voltage		2.9	3.2	3.5	V
V_{OS}	Output offset voltage			0	±100	mV
I_{CC}	Supply current		6	9	12	mA
I_{OMAX}	Output sink/source current		1.5	2		mA
I_{IN}	Input current (2% linearity)	Test circuit 5, Procedure 2	±60	±90		µA
I_{INMAX}	Maximum input current overload threshold	Test circuit 5, Procedure 4	±80	±115		µA
V_{OMAX}	Maximum differential output voltage swing	$R_L = \infty$, Test Circuit 5, Procedure 3		3.6		V_{P-P}

AC ELECTRICAL CHARACTERISTICS

Typical data and Min and Max limits apply at T_A = 25°C and $V_{CC1} = V_{CC2}$ =+5V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SA5222			UNIT
			Min	Typ	Max	
R_T	Transresistance (differential output)	DC tested, $R_L = \infty$, Test Circuit 5, Procedure 1	13.3	16.6	19.9	kΩ
R_O	Output resistance (differential output)	DC tested	30	60	90	Ω
R_T	Transresistance (single-ended output)	DC tested, $R_L = \infty$	6.65	8.3	9.95	kΩ
R_O	Output resistance (single-ended output)	DC tested	15	30	45	Ω
f_{3dB}	Bandwidth (-3dB)[1]	Test Circuit 1	110	140		MHz
R_{IN}	Input resistance			150		Ω
C_{IN}	Input capacitance[2]			1		pF
$\Delta R/\Delta V$	Transresistance power supply sensitivity	$V_{CC1} = V_{CC2}$ = 5 ±0.5V		1.0		%/V
$\Delta R/\Delta T$	Transresistance ambient temperature sensitivity	$\Delta T_A = T_{A\,MAX} - T_{A\,MIN}$		0.07		%/°C
I_{IN}	RMS noise current spectral density (referred to input)	Test Circuit 2, f = 10MHz		2.0		$pA/\sqrt{Hz}$
I_T	Integrated RMS noise current over the bandwidth (referred to input)	Test circuit 2, Δf = 50MHz		15		nA
	C_S = 0pF	Δf = 100MHz		25		nA
		Δf = 150MHz		36		nA
	C_S = 1pF	Δf = 50MHz		17		nA
		Δf = 100MHz		35		nA
		Δf = 150MHz		55		nA
PSRR	Power supply rejection ratio	DC Tested, ΔV_{CC} = ±0.5V		–55		dB
PSRR	Power supply rejection ratio[3]	f = 1.0MHz, Test Circuit 3		–34		dB

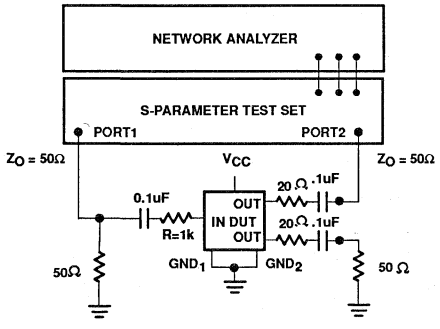
AC ELECTRICAL CHARACTERISTICS (continued)

I_{INMAX}	Maximum input amplitude for output duty cycle of 50 ±5%[4]	Test circuit 4		±120		µA
t_r, t_f	Rise and fall times	10 – 90%		2.2		ns
t_D	Group delay	f = 10MHz		2.2		ns

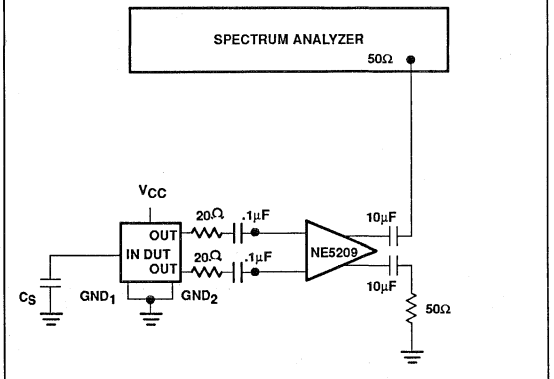
NOTES:
1. Bandwidth is tested into 50Ω load. Bandwidth into 1kΩ load is approximately 165MHz.
2. Does not include Miller-multiplied capacitance of input device.
3. PSRR is output referenced and is circuit board layout dependent at higher frequencies. For best performance use a RF filter in V_{CC} line.
4. Monitored in production via linearity and over load tests.

TEST CIRCUITS

SINGLE-ENDED	DIFFERENTIAL
$R_T = \frac{V_{OUT}}{V_{IN}}\ R = 2 \cdot S_{21} \cdot R$	$R_T = \frac{V_{OUT}}{V_{IN}}\ R = 4 \cdot S_{21} \cdot R$
$R_O = Z_O \left\lvert \frac{1 + S22}{1 - S22} \right\rvert$ -20	$R_O = 2Z_O \left\lvert \frac{1 + S22}{1 - S22} \right\rvert$ -40

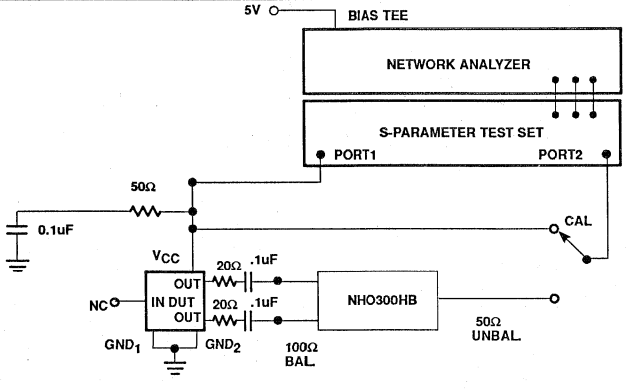


Test Circuit 1: Bandwidth



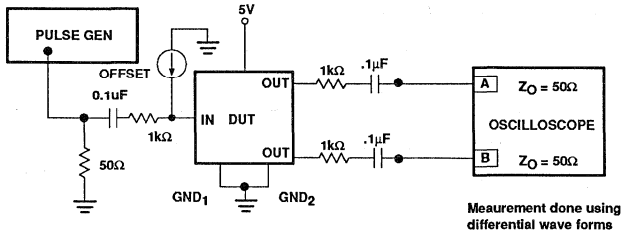
Test Circuit 2: Noise

TEST CIRCUITS (continued)



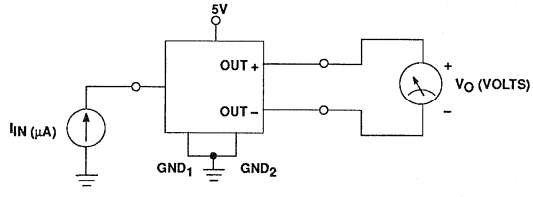
Test Circuit 3: PSRR

TEST CIRCUITS (continued)

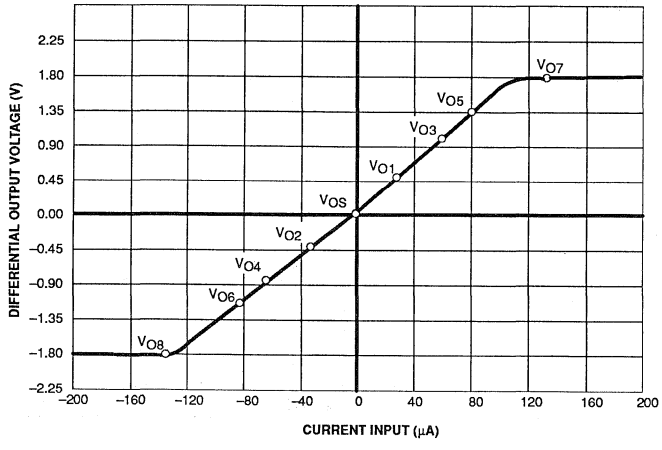


Test Circuit 4: Duty Cycle Distortion

TEST CIRCUITS (continued)



Typical V_O (Differential) vs I_{IN}



SA5222 TEST CONDITIONS

Procedure 1 R_T measured at 30μA
$R_T = (V_{O1} - V_{O2}) / (+30\mu A - (-30\mu A))$
Where: V_{O1} Measure at I_{IN} = +30μA
V_{O2} Measured at I_{IN} = -30μA

Procedure 2 Linearity = 1 - ABS(($V_{OA} - V_{OB}$ / ($V_{O3} - V_{O4}$))
Where: V_{O3} Measured at I_{IN} = +60μA
V_{O4} Measured at I_{IN} = -60μA
$V_{OA} = R_T$ x (+60μA) + V_{OS}
$V_{OB} = R_T$ x (-60μA) + V_{OS}

Procedure 3 $V_{OMAX} = V_{O7} - V_{O8}$
Where: V_{O7} Measured at I_{IN} = +130μA
V_{O8} Measured at I_{IN} = -130μA

Procedure 4 I_{INMAX} Test Pass Conditions:
$V_{O7} - V_{O5} > 50mV$ and $V_{O6} - V_{O8} < 50mV$
Where: V_{O5} Measured at I_{IN} = +80μA
V_{O6} Measured at I_{IN} = -80μA
V_{O7} Measured at I_{IN} = +130μA
V_{OB} Measured at I_{IN} = -130μA

Test Circuit 5: DC Tests

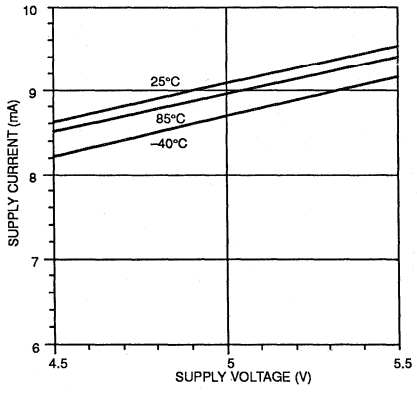


Figure 1. I_{CC} vs. V_{CC} and Temperature

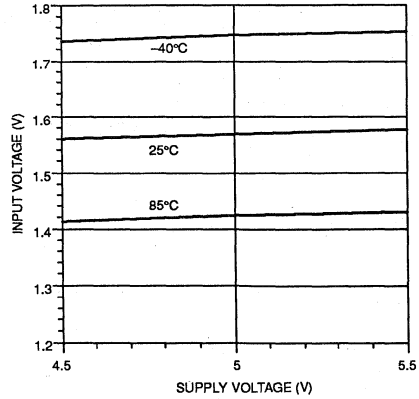


Figure 2. Input Voltage vs. V_{CC} and Temperature

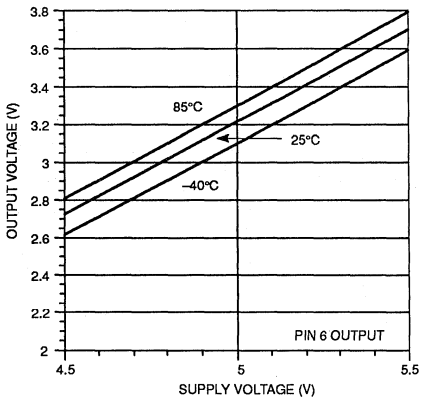


Figure 3. Output Voltage vs. V_{CC} and Temperature

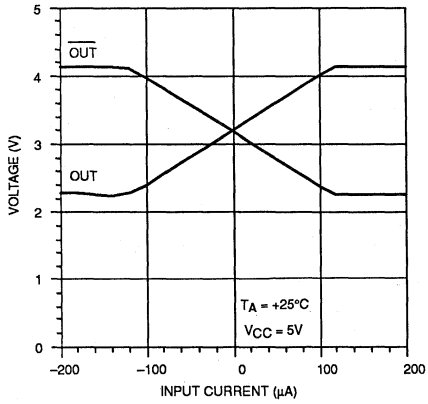


Figure 4. Differential Output Voltages vs. Input Current

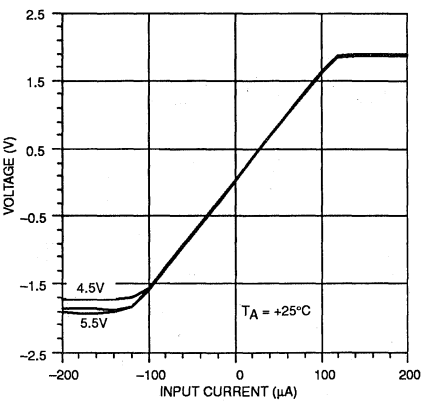


Figure 5. Differential Output Voltage vs Input Current and V_{CC}

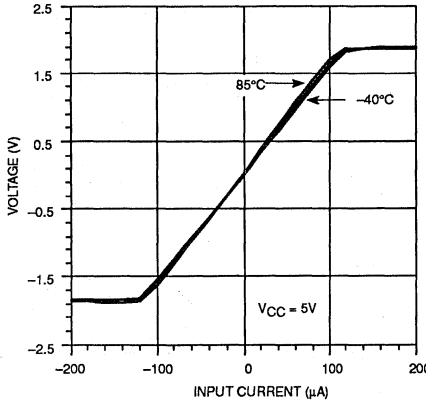


Figure 6. Differential Output Voltage vs. Input Current and Temperature

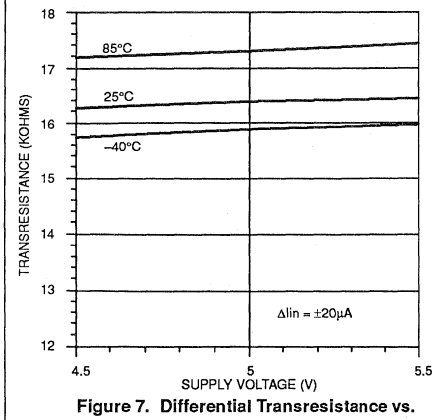


Figure 7. Differential Transresistance vs. V_{CC} and Temperature

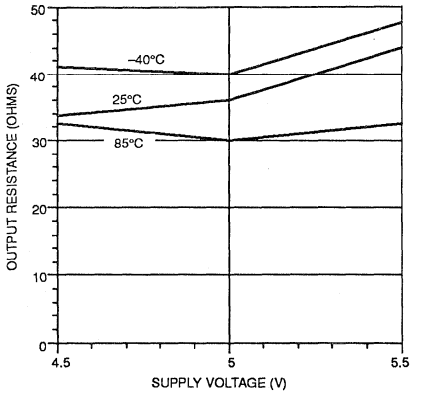


Figure 8. Output Resistance vs. V_{CC} and Temperature

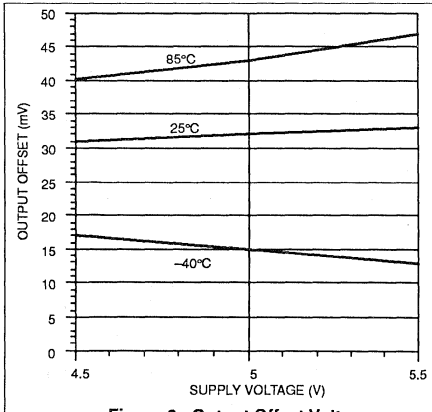


Figure 9. Output Offset Voltage vs. V_{CC} and Temperature

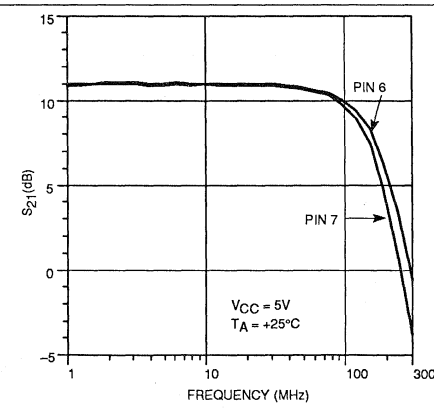


Figure 10. Insertion Gain vs. Frequency

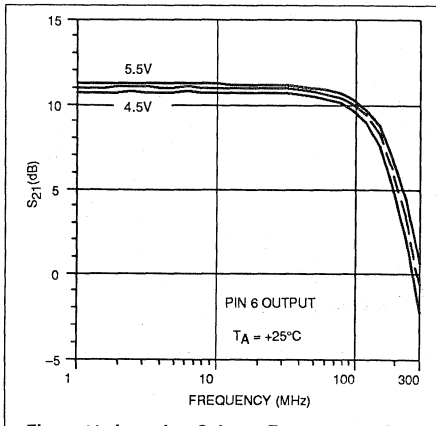


Figure 11. Insertion Gain vs. Frequency and V_{CC}

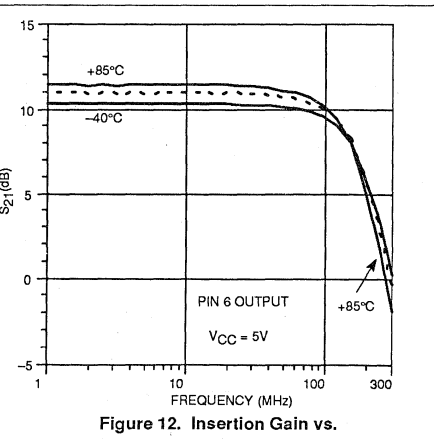


Figure 12. Insertion Gain vs. Frequency and Temperature

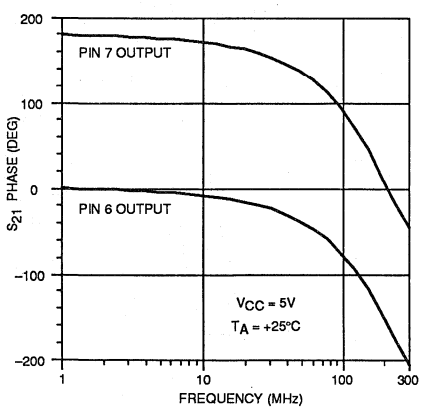


Figure 13. Phase vs. Frequency

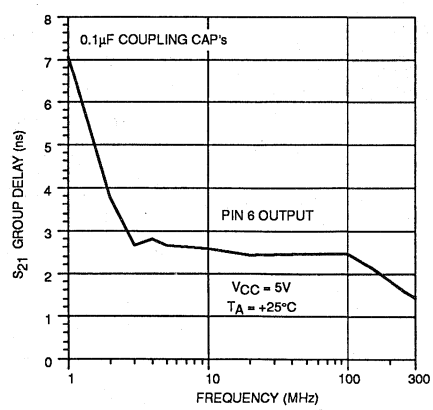


Figure 14. Group Delay vs. Frequency

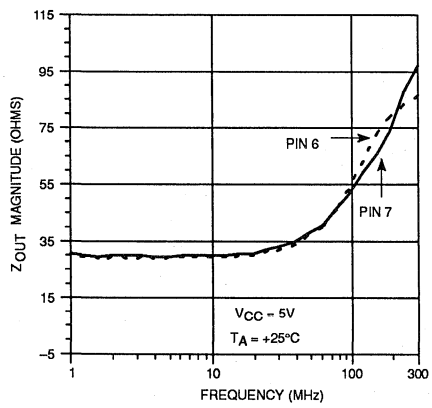


Figure 15. Output Impedance vs. Frequency

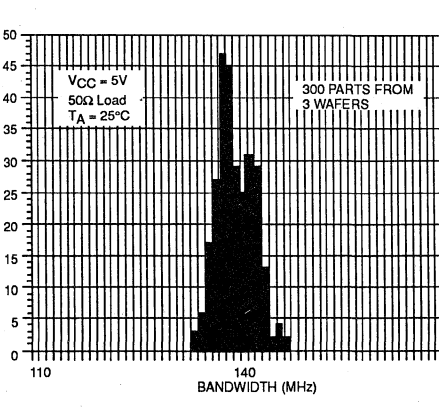


Figure 16. –3dB Bandwidth Distribution

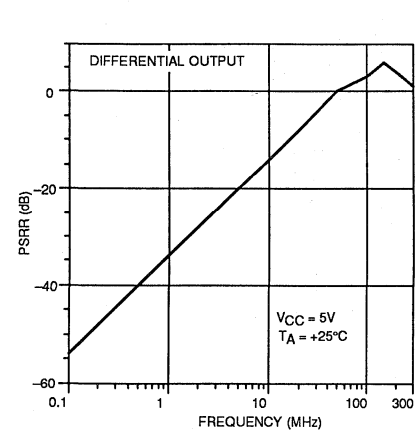


Figure 17. Power–Supply Rejection Ratio vs. Frequency

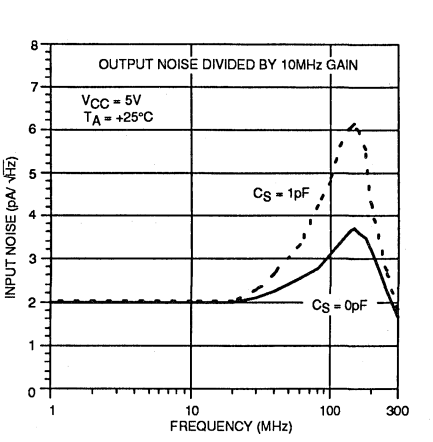


Figure 18. Input Noise Spectral Density vs. Frequency

FDDI fiber optic postamplifier — NE/SA5224

DESCRIPTION

The NE/SA5224 is a high-gain limiting amplifier that is designed to process signals from fiber optic preamplifiers. Capable of operating at 125Mb/s, the chip is FDDI compatible and has input signal level-detection with a user-adjustable threshold. The DATA and LEVEL-DETECT outputs are differential for optimum noise margin and ease of use. Also available is the NE/SA5225 which is an ECL 10K version of the NE/SA5224.

FEATURES

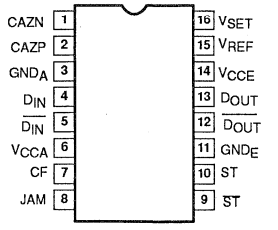
- Wideband operation: 1.0kHz to 120MHz typical
- Operation with single +5V or –5.2V supply
- Differential 100k ECL outputs
- Programmable input signal level-detection
- Fully differential for excellent PSRR to 1GHz

APPLICATIONS

- FDDI
- Data communication in noisy industrial environments
- LANs

PIN DESCRIPTION

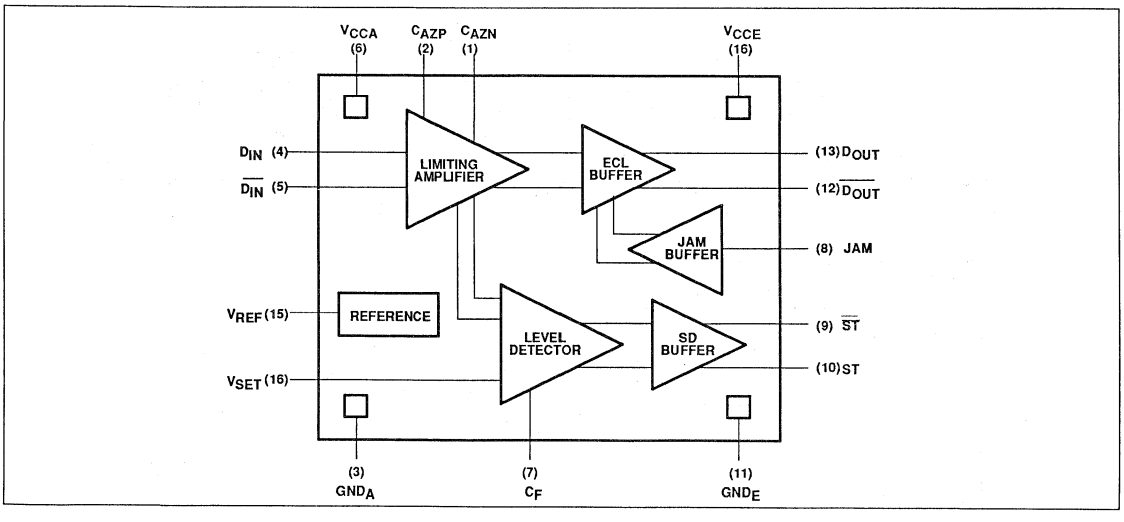
D Package



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE5224D
16-Pin Plastic SO	–40 to +85°C	SA5224D

BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NO.	NAME	FUNCTION
1	C_{AZN}	Auto-zero capacitor pin. Connecting a capacitor between this pin and C_{AZP} will cancel the offset voltage of the limiting amplifier.
2	C_{AZP}	Auto-zero capacitor pin. Connecting a capacitor between this pin and C_{AZN} will cancel the offset voltage of the limiting amplifier.
3	GND_A	Analog GND pin. Connect to ground for +5V upshifted ECL operation. Connect to –5.2V for standard ECL operation. Must be at same potential as GND_E (Pin 11).
4	D_{IN}	Differential input. DC bias level is set internally at approximately 2.9V. Complimentary to $\overline{D_{IN}}$ (Pin 5).
5	$\overline{D_{IN}}$	Differential input. DC bias level is set internally at approximately 2.9V. Complimentary to D_{IN} (Pin 4).
6	V_{CCA}	Analog power supply pin. Connect to a +5V supply for upshifted ECL operation. Connect to ground for standard ECL operation. Must be at same potential as V_{CCE} (Pin 14).
7	C_F	Filter capacitor for level detector. Capacitor should be connected between this pin and V_{CCA}.
8	JAM	This ECL-compatible input controls the output buffers $\overline{D_{OUT}}$ and D_{OUT} (Pins 12 and 13). When an ECL LOW signal is applied, the outputs will follow the input signal. When an ECL HIGH signal is applied, the D_{OUT} and $\overline{D_{OUT}}$ pins will latch into LOW and HIGH states, respectively. When left unconnected, this pin is actively pulled-low (JAM OFF).
9	$\overline{ST}$	Input signal level-detect $\overline{STATUS}$. This ECL output is high when the input signal is below the user programmable threshold level.
10	ST	ECL compliment of $\overline{ST}$ (Pin 9).
11	GND_E	Digital GND pin. Connect to ground for +5V upshifted ECL operation. Connect to a negative supply for normal ECL operation. Must be at the same potential as GND_A (Pin 3).
12	$\overline{D_{OUT}}$	ECL-compatible output. Nominal level is V_{CCE}–1.3V. When JAM is HIGH, this pin will be forced into an ECL HIGH condition. Complimentary to D_{OUT} (Pin 13).
13	D_{OUT}	ECL-compatible output. Nominal level is V_{CCE}–1.3V. When JAM is HIGH, this pin will be forced into an ECL LOW condition. Complimentary to $\overline{D_{OUT}}$ (Pin 12).
14	V_{CCE}	Digital power supply pin. Connect to a +5V supply for upshifted ECL operation. Connect to ground during normal ECL operation. Must be at the same potential as V_{CCA} (Pin 6).
15	V_{REF}	Reference voltage for threshold level voltage divider. Nominal value is approximately 2.64V.
16	V_{SET}	Input threshold level setting circuit. This input can come from a voltage divider between V_{REF} and GND_A.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE	SA	
V_{CC}	Power supply (V_{CC} - GND)	6	6	V
T_A	Operating ambient	0 to +70	–45 to +85	°C
T_J	Operating junction	–55 to +150	–55 to +150	°C
T_{STG}	Storage	–65 to +150	–65 to +150	°C
P_D	Power dissipation, T_A = 25°C (still air)[2] 16-pin Plastic SO	1100	1100	mW

NOTE:

1. Maximum dissipation is determined by the ambient temperature and the thermal resistance,
   θ_{JA}: 16-pin SO: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	4.5 to 5.5	V
T_A	Ambient temperature ranges NE grade SA grade	 0 to +70 –40 to +85	 °C °C
T_J	Junction temperature ranges NE grade SA grade	 0 to +95 –40 to +110	 °C °C

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over operating temperature at V_{CC} = 5V ±10%, unless otherwise specified. Typical data apply at T_A = 25°C and V_{CC} = +5V.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA5224			UNIT
			Min	Typ	Max	
V_{IN}	Input signal voltage single-ended differential		 .002 .004		 1.5 3.0	V_{P-P}
V_{OS}	Input offset voltage[2]				50	µV
V_N	Input RMS noise[2]				60	µV
V_{TH}	Input level-detect programmability single-ended	V_{IN} = 200kHz square wave	2		12	mV_{P-P}
V_{HYS}	Level-detect hysteresis		4	5	6	dB
I_{CC}	V_{CCA} + V_{CCE} supply current	No ECL loading		27	35	mA
I_{INL}	JAM input current	Pin 8 = 0V	–10		10	µA
V_{OHMAX}	Maximum logic high[1]				–0.880	V_{DC}
V_{OHMIN}	Minimum logic high[1]		–1.055			V_{DC}
V_{OLMAX}	Maximum logic low[1]				–1.620	V_{DC}
V_{OLMIN}	Minimum logic low[1]		–1.870			V_{DC}
V_{IH}	Minimum input for JAM = high[1]		–1.165			V_{DC}
V_{IL}	Maximum input for JAM = low[1]				–1.490	V_{DC}

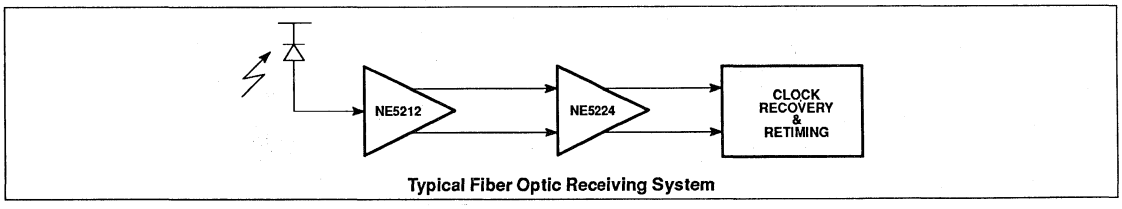
NOTES:
1. These ECL specifications are referenced to the V_{CCE} rail and apply for T_A = 0°C to 85°C.
2. Guaranteed by design.

AC ELECTRICAL CHARACTERISTICS

Typical data apply at T_A = 25°C and V_{CC} = +5V. Min and Max limits apply for 4.5 ≤ V_{CC} ≤ 5.5V and specified NE or SA temperature range.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA5224			UNIT
			Min	Typ	Max	
BW_1	Lower –3dB bandwidth	C_{AZ} = 0.1µF	0.5	1.0	1.5	kHz
BW_2	Upper –3dB bandwidth		90	120	150	MHz
R_{IN}	Input resistance	Pin 4 or 5	2.9	4.5	7.6	kΩ
C_{IN}	Input capacitance	Pin 4 or 5			2.5	pF
t_r, t_f	ECL output[3] risetime, falltime	R_L = 50Ω To V_{CCE} - 2V 20-80%	1.2		2.2	ns
t_{PWD}	Pulsewidth distortion				0.3	ns_{P-P}
R_{AZ}	Auto zero output resistance	Pin 1 or 2	155	250	423	kΩ
R_F	Level-detect filter resistance	Pin 7	14	24	41	kΩ
t_{LD}	Level-detect time constant	C_F = 0	0.5	1.0	2.0	µs

NOTES:
3. Both outputs should be terminated identically to minimize differential feedback to the device inputs on a PC board or substrate.



Typical Fiber Optic Receiving System

INPUT BIASING

The DATA INPUT pins (4 and 5) are DC biased at approximately 2.9V by an internal reference generator. The NE5224 can be DC coupled, but the driving source must operate within the allowable 1.4V to 4.4V input signal range (for V_{CC} = 5V). If AC coupling is used to remove any DC compatibility requirement, the coupling capacitors C1 and C2 must be large enough to pass the lowest input frequency of interest. For example, .001µF coupling capacitors react with the internal 4.5k input bias resistors to yield a lower –3dB frequency of 35kHz. This then sets a limit on the maximum number of consecutive "1"s or "0"s that can be sensed accurately at the system data rate. Capacitor tolerance and resistor variation (2.9k to 7.6k) must be included for an accurate calculation.

AUTO-ZERO CIRCUIT

Figure 1 also shows the essential details of the auto-zero circuit. A feedback amplifier (A4) is used to cancel the offset voltage of the forward signal path, so the input to the internal ECL comparator (A6) is at its toggle point in the absence of any input signal. The time constant of the cancelling circuitry is set by an external capacitor (C_{AZ}) connected between Pins 1 and 2. The formula for the lower –3dB frequency is:

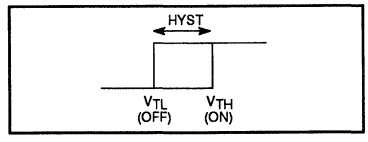
$$f_{-3dB} = \frac{150}{2\pi \cdot R_{AZ} \cdot C_{AZ}}$$

where R_{AZ} is the internal driving impedance which can vary from 155k to 423k over temperature and device fabrication limits. The input coupling time constant must also be considered in determining the lower frequency response of the NE5224.

INPUT SIGNAL LEVEL-DETECTION

The NE5224 allows for user programmable input signal level-detection and can automatically disable the switching of its ECL data outputs if the input is below a set threshold. This prevents the outputs from reacting to noise in the absence of a valid input signal, and insures that data will only be transmitted when the input signal-to-noise ratio is sufficient for low bit-error-rate system operation. Complimentary ECL flags (ST and STB) indicate whether the input signal is above or below the desired threshold level.

Figure 2 shows a simplified block diagram of the NE5224 level-detect system. The input signal is amplified and rectified before being compared to a programmable reference. A filter is included to prevent noise spikes from triggering the level-detector. This filter has a nominal 1µs time constant, and additional filtering can be achieved by using an external capacitor (CF) from Pin 7 to V_{CCA} (the internal driving impedance is nominally 24k). The resultant signal is then compared to a programmable level, V_{SET}, which is set by an internal voltage reference (2.64V) and an external resistor divider (R1 and R2). The value of R1 + R2 should be maintained at approximately 5k.



The circuit is designed to operate accurately over a differential 2-12mV_{P-P} square-wave input level detect range. This level, V_{SET}/100, is the average of V_{TH} and V_{TL}.

Nominal hysteresis of 5dB is provided by the complimentary ECL output comparator yielding $V_{TL} = \frac{V_{SET}}{139}$ and $V_{TH} = \frac{V_{SET}}{78}$. For example, with V_{SET} = 1.2V, a 15.4mV_{P-P} square-wave differential input will drive the ST pin high, and an input level below 8.6mV_{P-P} will drive the ST pin low.

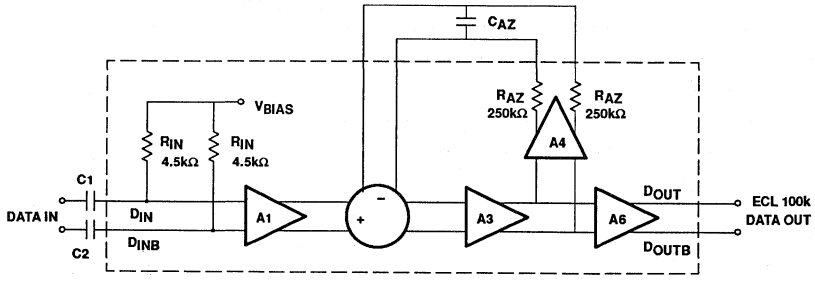


Figure 1. NE5224 Forward Gain Path Including Auto-Zero

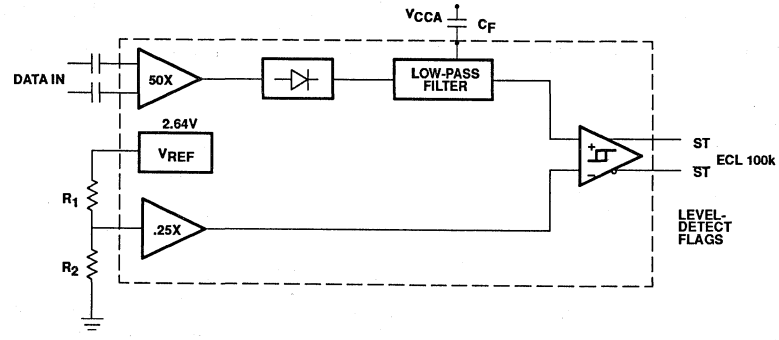


Figure 2. NE5224 Input Signal Level-Detect System

Since a "JAM" function is provided (Pin 8) and can force the data outputs to a predetermined state (D_{OUT} = LOW, $\overline{D_{OUT}}$ = HIGH), the $\overline{ST}$ and JAM pins can be connected together to automatically disable signal transmission when the chip senses that the input signal is below the desired threshold. JAM (Pin 8) low enables the Data Outputs. $\overline{ST}$ will be in a high ECL state for input signals below threshold.

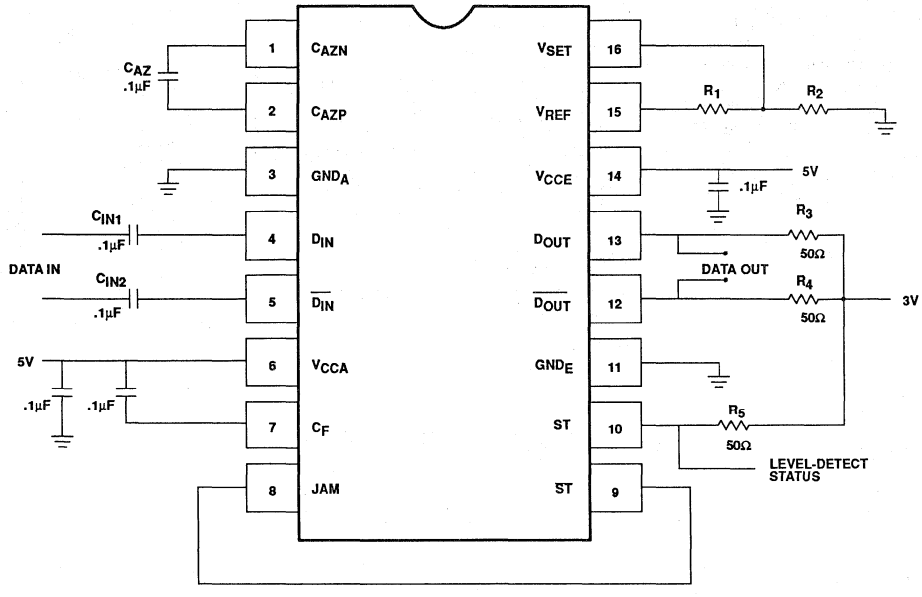


Figure 3. Application with V_{CC} = 5.0V

NOTE: A 50Ω resistor is required from Pin 9 to 3V only if the $\overline{ST}$ pin is required to meet 100k ECL specifications.

Fiber optic postamplifier — NE/SA5225

DESCRIPTION

The NE/SA5225 is a high-gain limiting amplifier that is designed to process signals from fiber optic preamplifiers. Capable of operating at 125Mb/s, the chip has input signal level-detection with a user-adjustable threshold. The DATA and LEVEL-DETECT outputs are differential for optimum noise margin and ease of use. Also available is the NE/SA5224 which is optimized for FDDI applications.

FEATURES

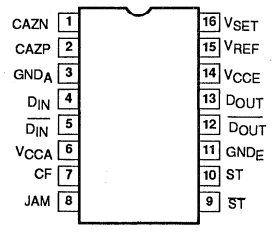
- Wideband operation: 1.0kHz to 120MHz typical
- Operation with single +5V or –5.2V supply
- Differential 10k ECL outputs
- Programmable input signal level-detection
- Fully differential for excellent PSRR to 1GHz

APPLICATIONS

- Data communication in noisy industrial environments
- LANs

PIN DESCRIPTION

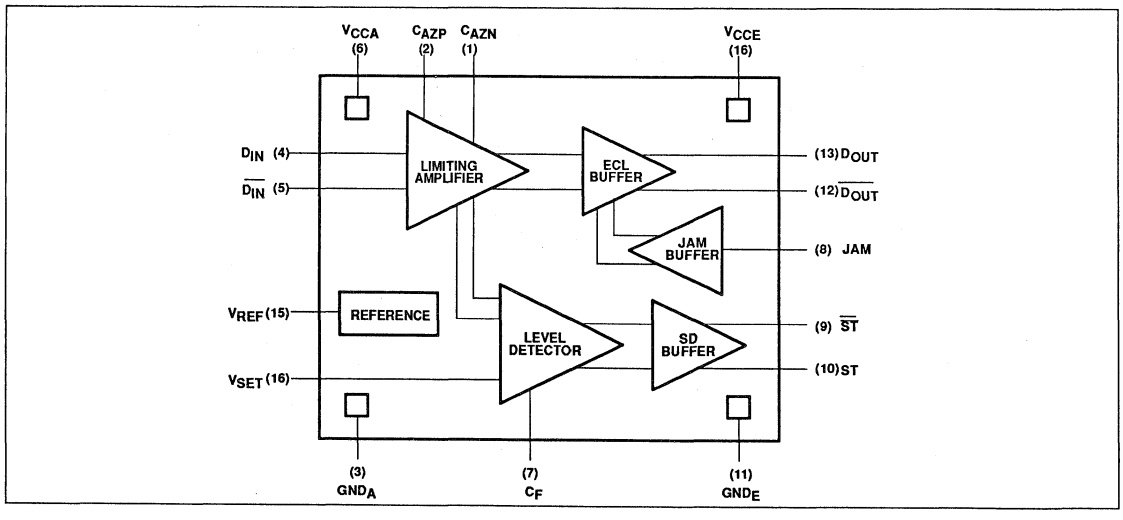
D Package



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE5225D
16-Pin Plastic SO	–40 to +85°C	SA5225D

BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NO.	NAME	FUNCTION
1	C_{AZN}	Auto-zero capacitor pin. Connecting a capacitor between this pin and C_{AZP} will cancel the offset voltage of the limiting amplifier.
2	C_{AZP}	Auto-zero capacitor pin. Connecting a capacitor between this pin and C_{AZN} will cancel the offset voltage of the limiting amplifier.
3	GND_A	Analog GND pin. Connect to ground for +5V upshifted ECL operation. Connect to –5.2V for standard ECL operation. Must be at same potential as GND_E (Pin 11).
4	D_{IN}	Differential input. DC bias level is set internally at approximately 2.9V. Complimentary to $\overline{D_{IN}}$ (Pin 5).
5	$\overline{D_{IN}}$	Differential input. DC bias level is set internally at approximately 2.9V. Complimentary to D_{IN} (Pin 4).
6	V_{CCA}	Analog power supply pin. Connect to a +5V supply for upshifted ECL operation. Connect to ground for standard ECL operation. Must be at same potential as V_{CCE} (Pin 14).
7	C_F	Filter capacitor for level detector. Capacitor should be connected between this pin and V_{CCA}.
8	JAM	This ECL-compatible input controls the output buffers $\overline{D_{OUT}}$ and D_{OUT} (Pins 12 and 13). When an ECL LOW signal is applied, the outputs will follow the input signal. When an ECL HIGH signal is applied, the D_{OUT} and $\overline{D_{OUT}}$ pins will latch into LOW and HIGH states, respectively. When left unconnected, this pin is actively pulled-low (JAM OFF).
9	$\overline{ST}$	Input signal level-detect $\overline{STATUS}$. This ECL output is high when the input signal is below the user programmable threshold level.
10	ST	ECL compliment of $\overline{ST}$ (Pin 9).
11	GND_E	Digital GND pin. Connect to ground for +5V upshifted ECL operation. Connect to a negative supply for normal ECL operation. Must be at the same potential as GND_A (Pin 3).
12	$\overline{D_{OUT}}$	ECL-compatible output. Nominal level is V_{CCE}–1.3V. When JAM is HIGH, this pin will be forced into an ECL HIGH condition. Complimentary to D_{OUT} (Pin 13).
13	D_{OUT}	ECL-compatible output. Nominal level is V_{CCE}–1.3V. When JAM is HIGH, this pin will be forced into an ECL LOW condition. Complimentary to $\overline{D_{OUT}}$ (Pin 12).
14	V_{CCE}	Digital power supply pin. Connect to a +5V supply for upshifted ECL operation. Connect to ground during normal ECL operation. Must be at the same potential as V_{CCA} (Pin 6).
15	V_{REF}	Reference voltage for threshold level voltage divider. Nominal value is approximately 2.64V.
16	V_{SET}	Input threshold level setting circuit. This input can come from a voltage divider between V_{REF} and GND_A.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE	SA	
V_{CC}	Power supply (V_{CC} - GND)	6	6	V
T_A	Operating ambient	0 to +70	–45 to +85	°C
T_J	Operating junction	–55 to +150	–55 to +150	°C
T_{STG}	Storage	–65 to +150	–65 to +150	°C
P_D	Power dissipation, T_A = 25°C (still air)[2] 16-pin Plastic SO	1100	1100	mW

NOTE:

1. Maximum dissipation is determined by the ambient temperature and the thermal resistance, θ_{JA}: 16-pin SO: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	4.5 to 5.5	V
T_A	Ambient temperature ranges NE grade SA grade	 0 to +70 –40 to +85	 °C °C
T_J	Junction temperature ranges NE grade SA grade	 0 to +95 –40 to +110	 °C °C

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over operating temperature at V_{CC} = 5V ±10%, unless otherwise specified. Typical data apply at T_A = 25°C and V_{CC} = +5V.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA5225			UNIT
			Min	Typ	Max	
V_{IN}	Input signal voltage single-ended differential		 .002 .004		 1.5 3.0	V_{P-P}
V_{OS}	Input offset voltage[2]				50	µV
V_N	Input RMS noise[2]				60	µV
V_{TH}	Input level-detect programmability single-ended	V_{IN} = 200kHz square wave	2		12	mV_{P-P}
V_{HYS}	Level-detect hysteresis[3]		2	3	4	dB
I_{CC}	V_{CCA} + V_{CCE} supply current	No ECL loading		27	35	mA
I_{INL}	JAM input current	Pin 8 = 0V	–10		10	µA
V_{IH}	Minimum input for JAM = high[1]		–1.165			V_{DC}
V_{IL}	Maximum input for JAM = low[1]				–1.490	V_{DC}

NOTES:
1. These ECL specifications are referenced to the V_{CCE} rail and apply for T_A = 0°C to 85°C.
2. Guaranteed by design.
3. Also see the NE/SA5224 which has 5dB ±1dB hystersis for FDDI compatibility.

TABLE 1: 10K ECL VOLTAGE LEVELS (REFERENCED TO V_{CCE})

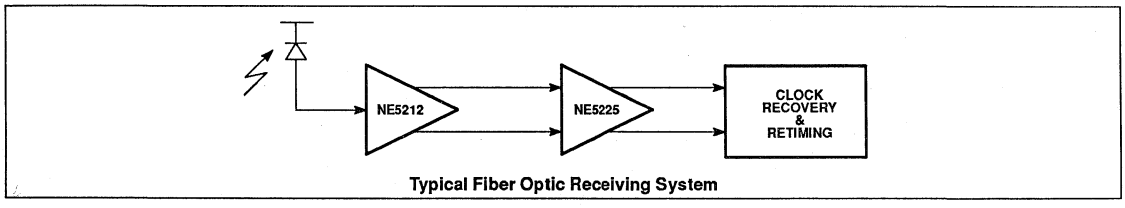
PARAMETER	-30°C	0°C	25°C	75°C	85°C	UNIT
V_{OHMAX}	-0.890	-0.840	-0.810	-0.735	-0.700	V_{DC}
V_{OHMIN}	-1.060	-1.020	-.980	-.920	-.890	V_{DC}
V_{OLMAX}	-1.650	-1.630	-1.630	-1.600	-1.615	V_{DC}
V_{OHMIN}	-1.890	-1.950	-1.950	-1.950	-1.920	V_{DC}

AC ELECTRICAL CHARACTERISTICS

Typical data apply at T_A = 25°C and V_{CC} = +5V. Min and Max limits apply for 4.5 ≤ V_{CC} ≤ 5.5V and specified NE or SA temperature range.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA5225			UNIT
			Min	Typ	Max	
BW_1	Lower –3dB bandwidth	C_{AZ} = 0.1µF	0.5	1.0	1.5	kHz
BW_2	Upper –3dB bandwidth		90	120	150	MHz
R_{IN}	Input resistance	Pin 4 or 5	2.9	4.5	7.6	kΩ
C_{IN}	Input capacitance	Pin 4 or 5			2.5	pF
t_r, t_f	ECL output[4] risetime, falltime	R_L = 50Ω To V_{CCE} - 2V 20-80%	1.2		2.2	ns
t_{PWD}	Pulsewidth distortion				0.3	ns_{P-P}
R_{AZ}	Auto zero output resistance	Pin 1 or 2	155	250	423	kΩ
R_F	Level-detect filter resistance	Pin 7	14	24	41	kΩ
t_{LD}	Level-detect time constant	C_F = 0	0.5	1.0	2.0	µs

NOTES:
1. Both outputs should be terminated identically to minimize differential feedback to the device inputs on a PC board or substrate.



Typical Fiber Optic Receiving System

INPUT BIASING

The DATA INPUT pins (4 and 5) are DC biased at approximately 2.9V by an internal reference generator. The NE5225 can be DC coupled, but the driving source must operate within the allowable 1.4V to 4.4V input signal range (for V_{CC} = 5V). If AC coupling is used to remove any DC compatibility requirement, the coupling capacitors C1 and C2 must be large enough to pass the lowest input frequency of interest. For example, .001µF coupling capacitors react with the internal 4.5k input bias resistors to yield a lower –3dB frequency of 35kHz. This then sets a limit on the maximum number of consecutive "1"s or "0"s that can be sensed accurately at the system data rate. Capacitor tolerance and resistor variation (2.9k to 7.6k) must be included for an accurate calculation.

AUTO-ZERO CIRCUIT

Figure 1 also shows the essential details of the auto-zero circuit. A feedback amplifier (A4) is used to cancel the offset voltage of the forward signal path, so the input to the internal ECL comparator (A6) is at its toggle point in the absence of any input signal. The time constant of the cancelling circuitry is set by an external capacitor (C_{AZ}) connected between Pins 1 and 2. The formula for the lower –3dB frequency is:

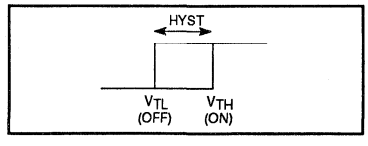
$$f_{-3dB} = \frac{150}{2\pi \cdot R_{AZ} \cdot C_{AZ}}$$

where R_{AZ} is the internal driving impedance which can vary from 155k to 423k over temperature and device fabrication limits. The input coupling time constant must also be considered in determining the lower frequency response of the NE5225.

INPUT SIGNAL LEVEL-DETECTION

The NE5225 allows for user programmable input signal level-detection and can automatically disable the switching of its ECL data outputs if the input is below a set threshold. This prevents the outputs from reacting to noise in the absence of a valid input signal, and insures that data will only be transmitted when the input signal-to-noise ratio is sufficient for low bit-error-rate system operation. Complimentary ECL flags (ST and STB) indicate whether the input signal is above or below the desired threshold level.

Figure 2 shows a simplified block diagram of the NE5225 level-detect system. The input signal is amplified and rectified before being compared to a programmable reference. A filter is included to prevent noise spikes from triggering the level-detector. This filter has a nominal 1µs time constant, and additional filtering can be achieved by using an external capacitor (CF) from Pin 7 to V_{CCA} (the internal driving impedance is nominally 24k). The resultant signal is then compared to a programmable level, V_{SET}, which is set by an internal voltage reference (2.64V) and an external resistor divider (R1 and R2). The value of R1 + R2 should be maintained at approximately 5k.



The circuit is designed to operate accurately over a differential 2-12mV_{P-P} square-wave input level detect range. This level, V_{SET}/100, is the average of V_{TH} and V_{TL}.

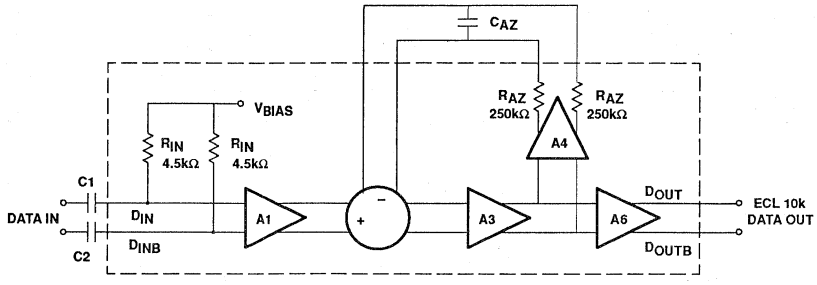


Figure 1. NE5225 Forward Gain Path Including Auto-Zero

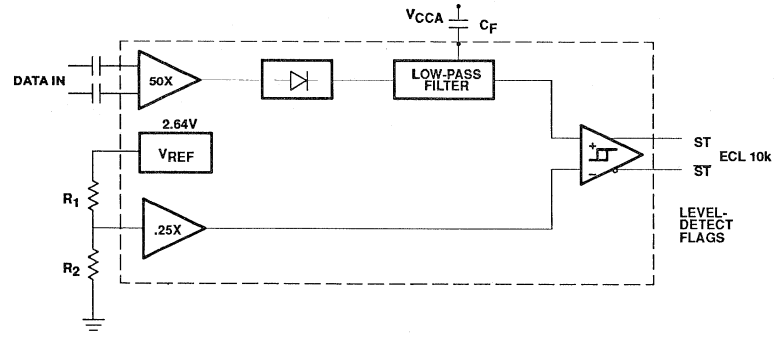


Figure 2. NE5225 Input Signal Level-Detect System

Nominal hysteresis of 3dB is provided by the complimentary ECL output comparator yielding $V_{TL} = \frac{V_{SET}}{121}$ and $V_{TH} = \frac{V_{SET}}{85}$. For example, with V_{SET} = 1.2V, a 14.05mV_{P-P} square-wave differential input will drive the ST pin high, and an input level below 9.95mV_{P-P} will drive the ST pin low.

Since a "JAM" function is provided (Pin 8) and can force the data outputs to a predetermined state (D_{OUT} = LOW, $\overline{D_{OUT}}$ = HIGH), the $\overline{ST}$ and JAM pins can be connected together to automatically disable signal transmission when the chip senses that the input signal is below the desired threshold. JAM (Pin 8) low enables the Data Outputs. $\overline{ST}$ will be in a high ECL state for input signals below threshold.

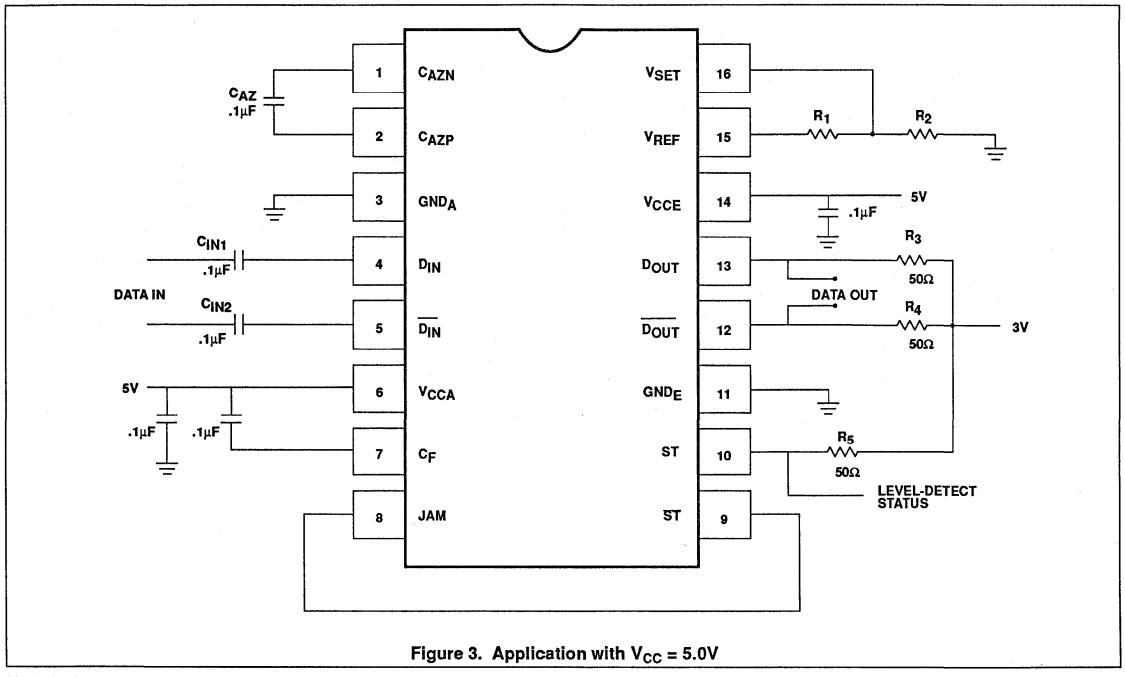


Figure 3. Application with V_{CC} = 5.0V

NOTE: A 50Ω resistor is required from Pin 9 to 3V only if the $\overline{ST}$ pin is required to meet 10k ECL specifications.

Section 5
Package Outlines

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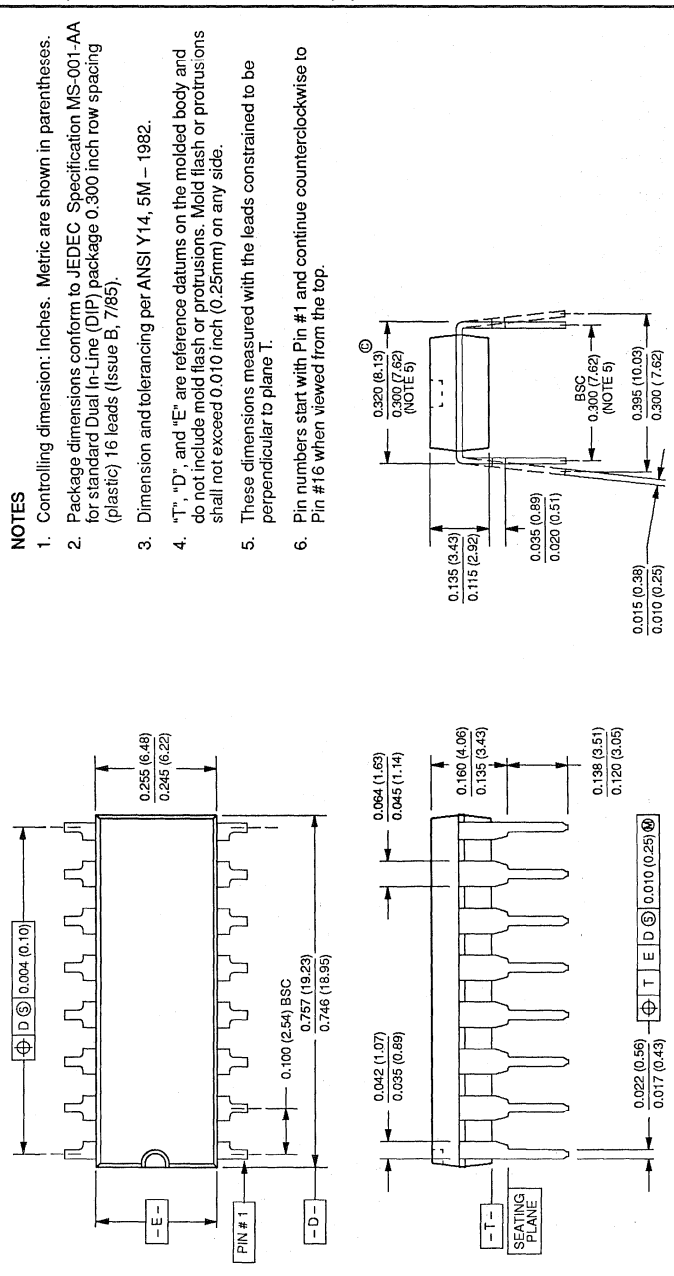
16-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



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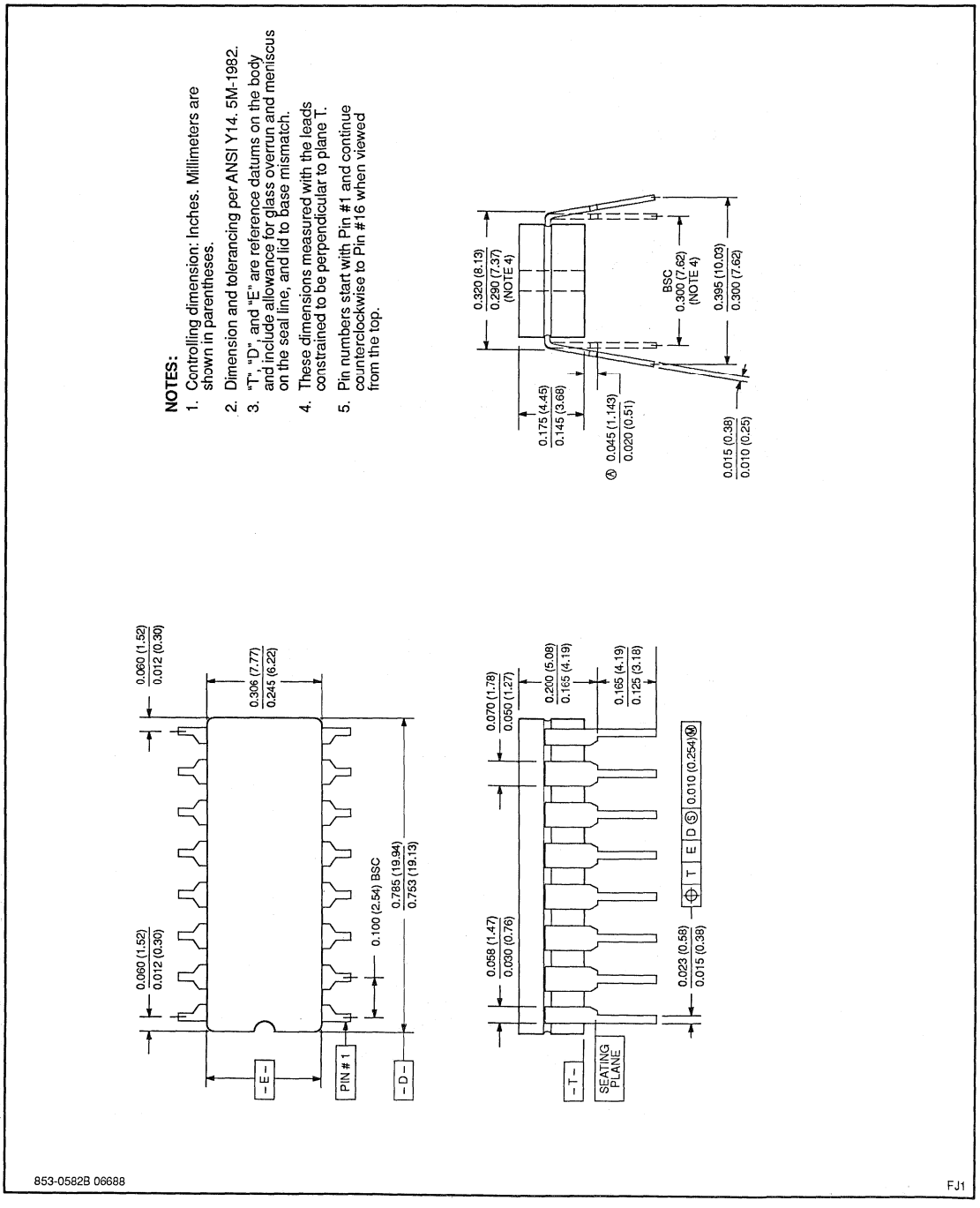

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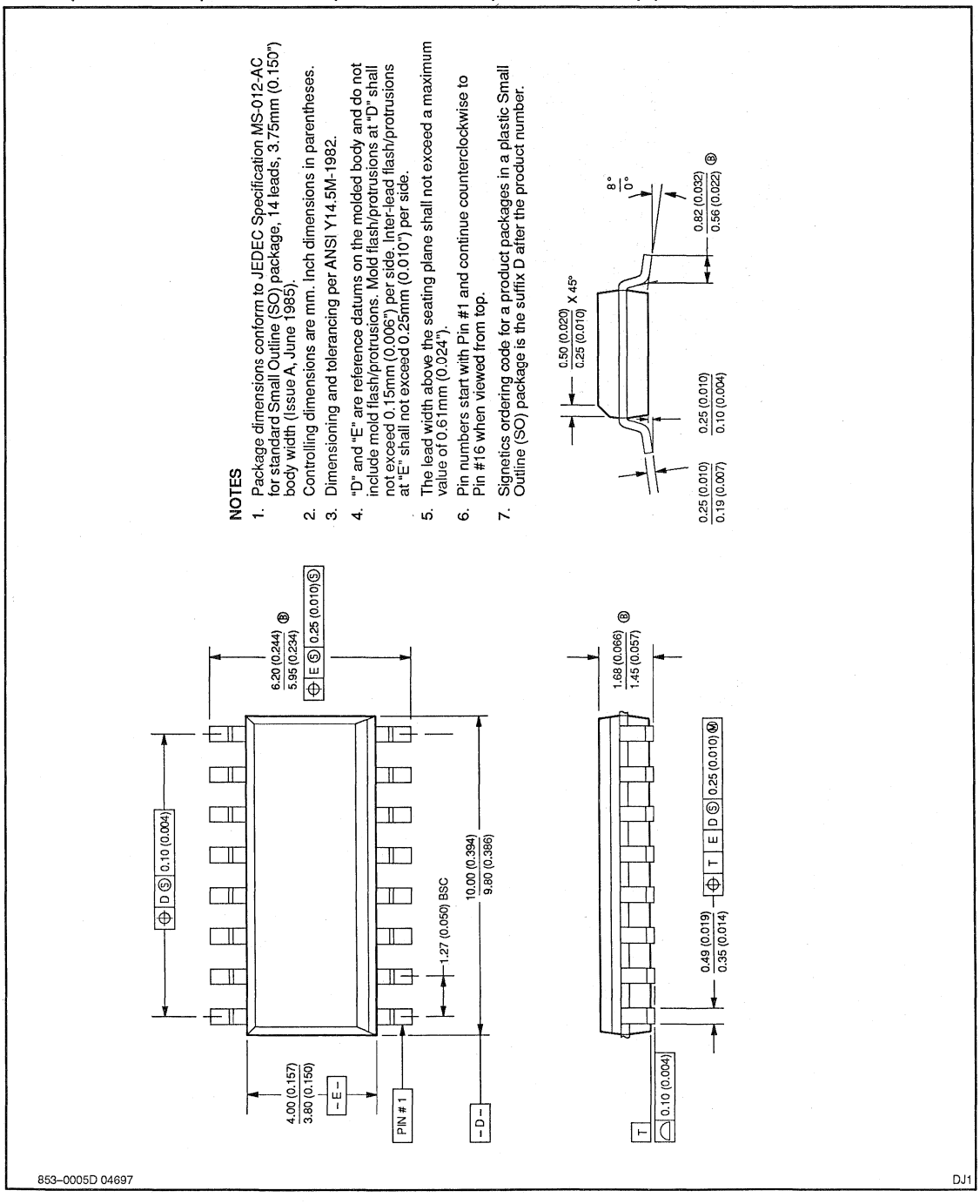

Package outlines

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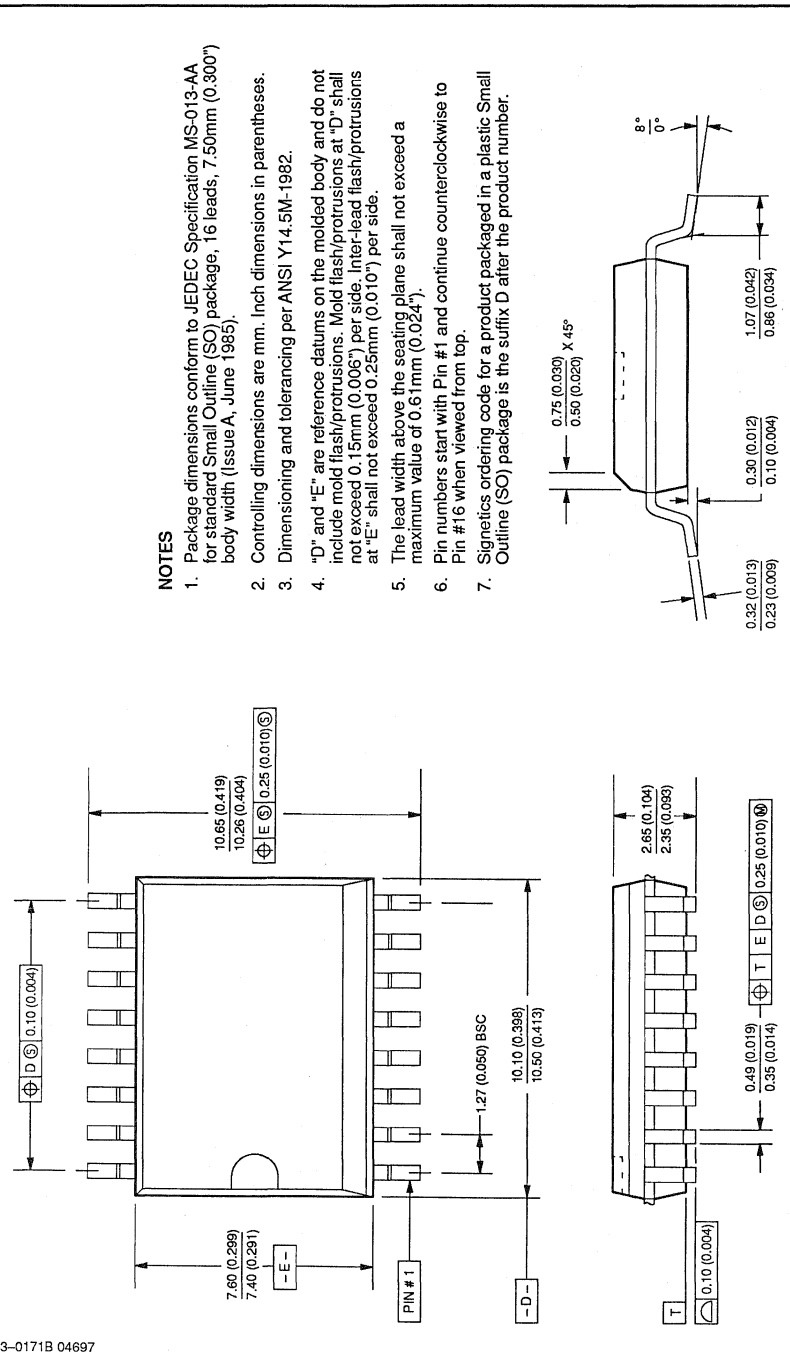

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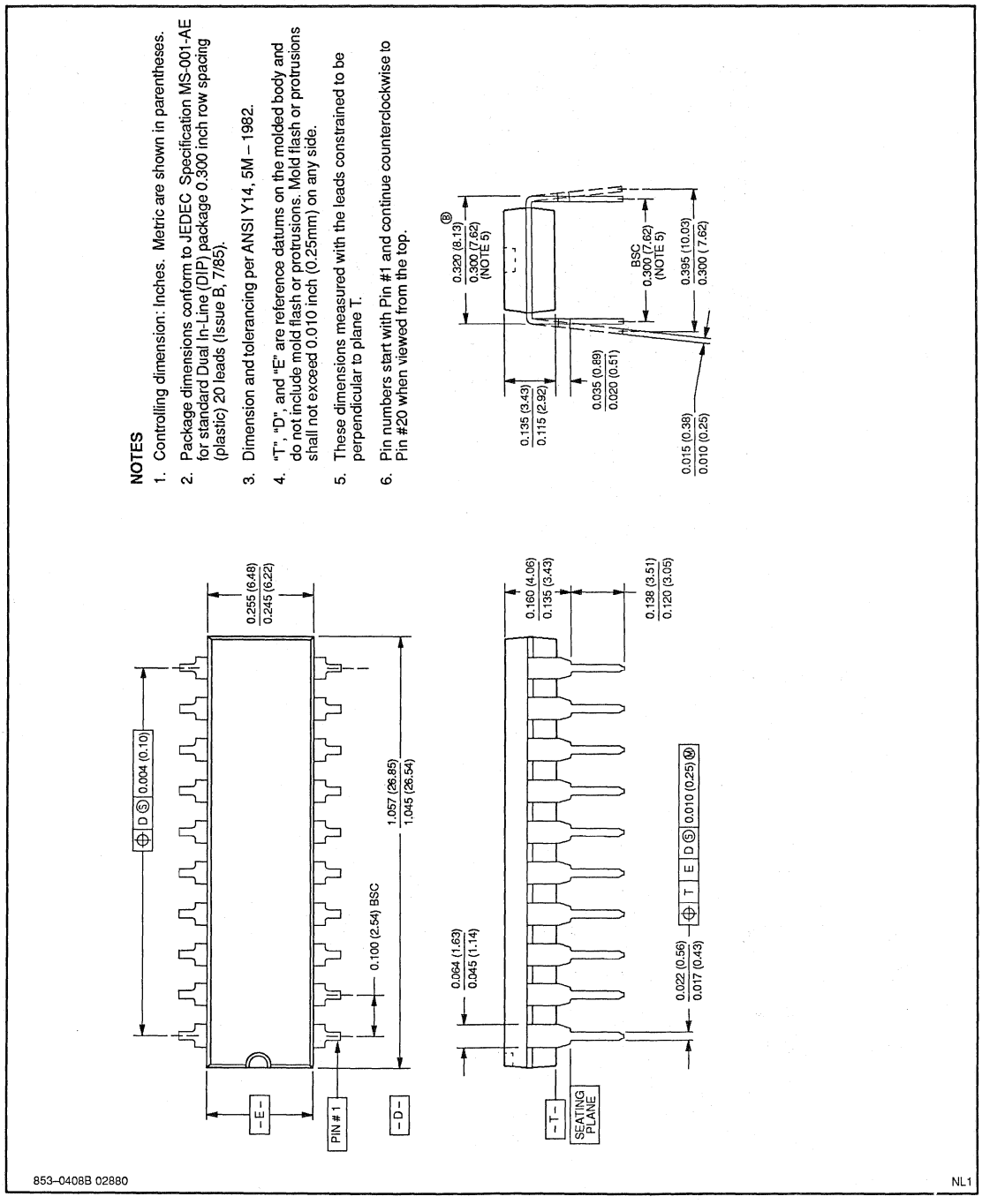

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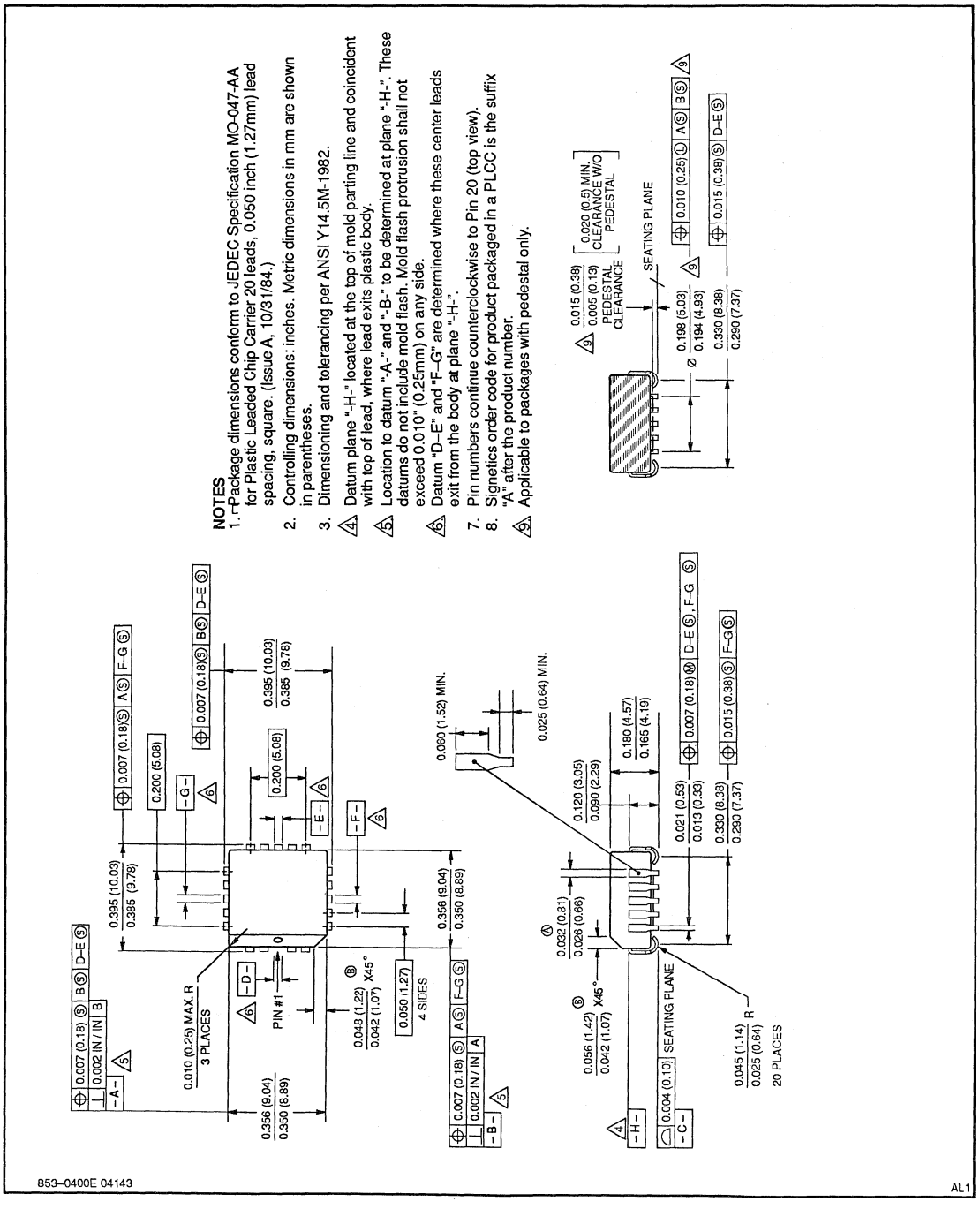

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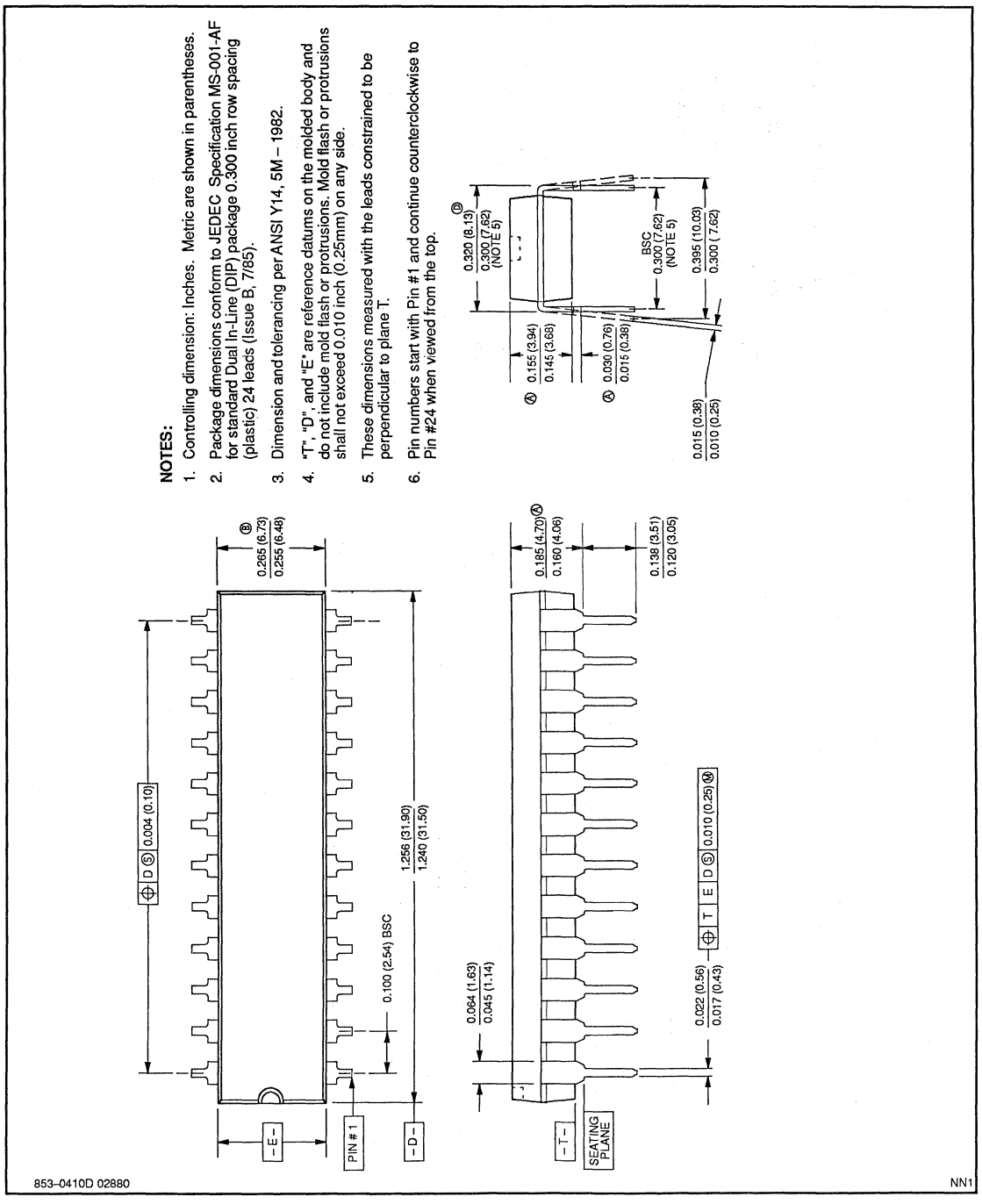

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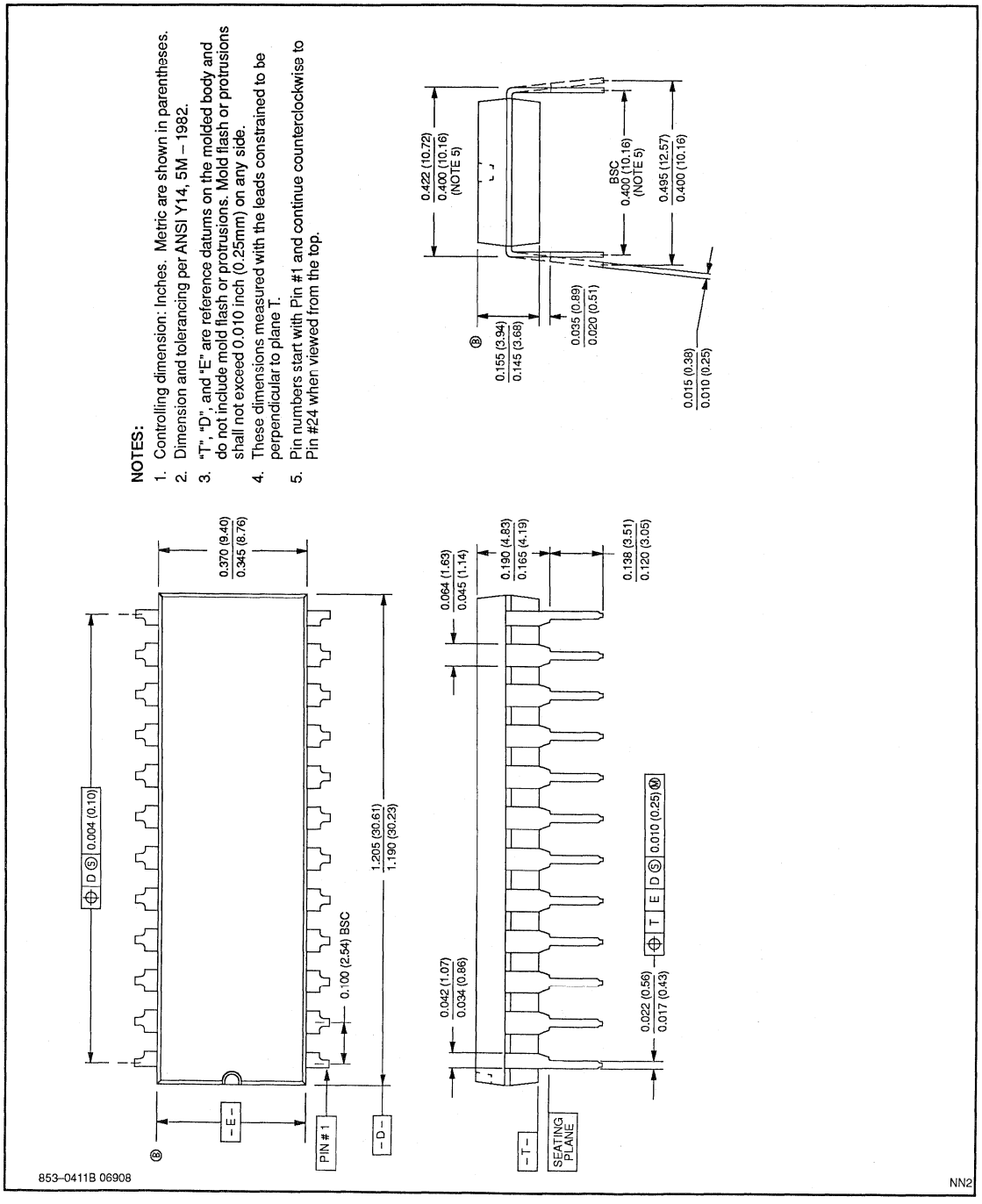

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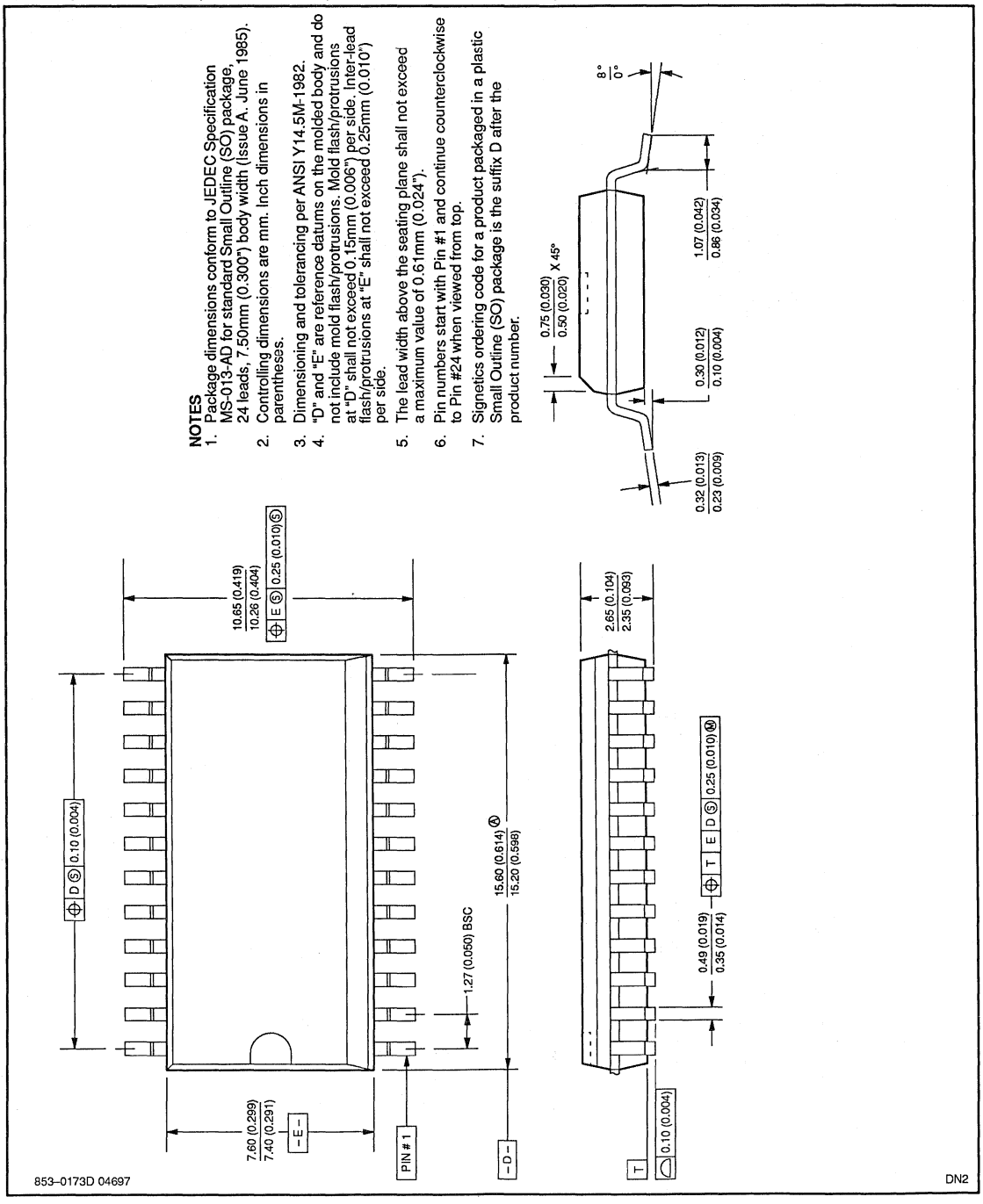
24-PIN (300 mils wide) Plastic SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D) PACKAGE



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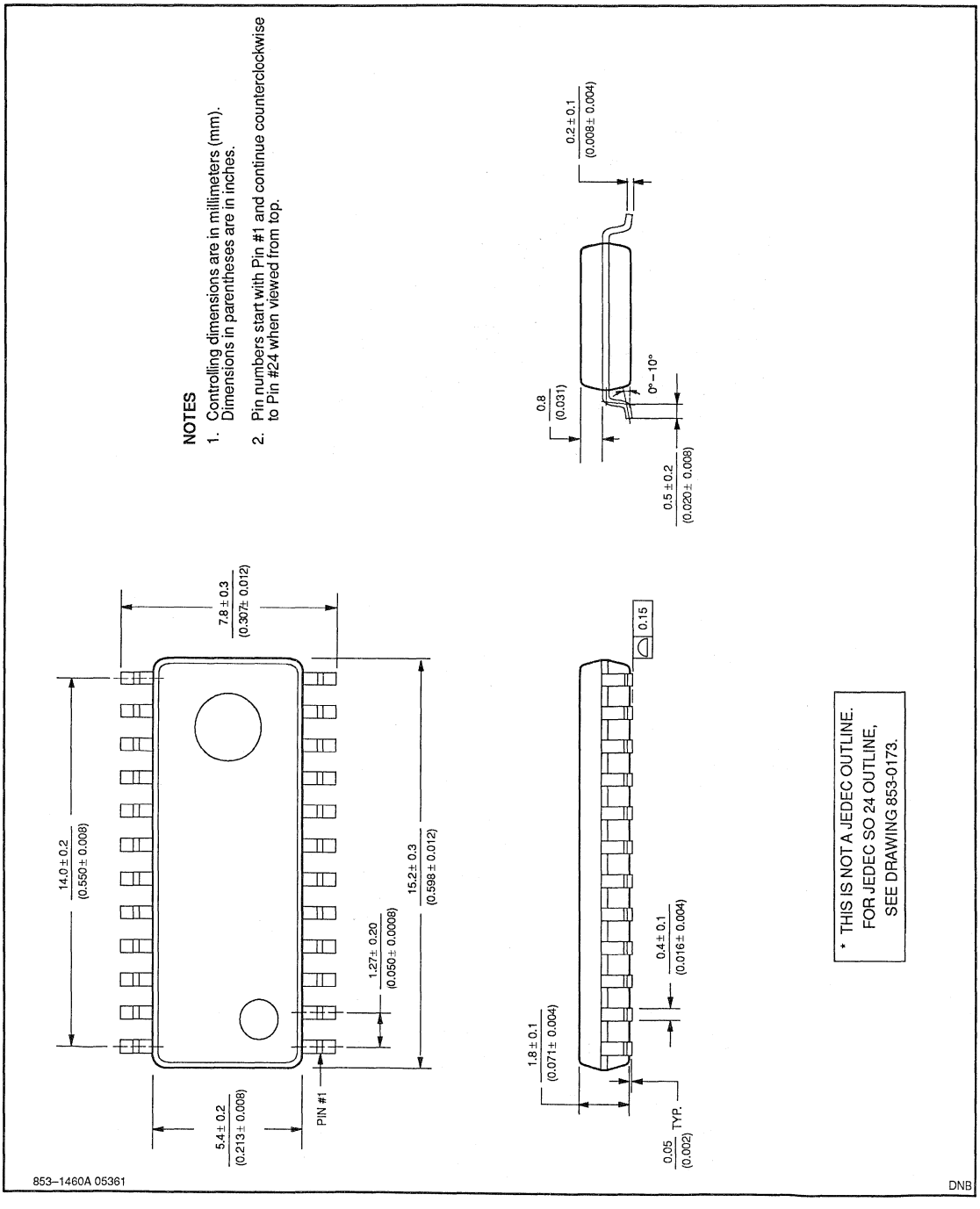

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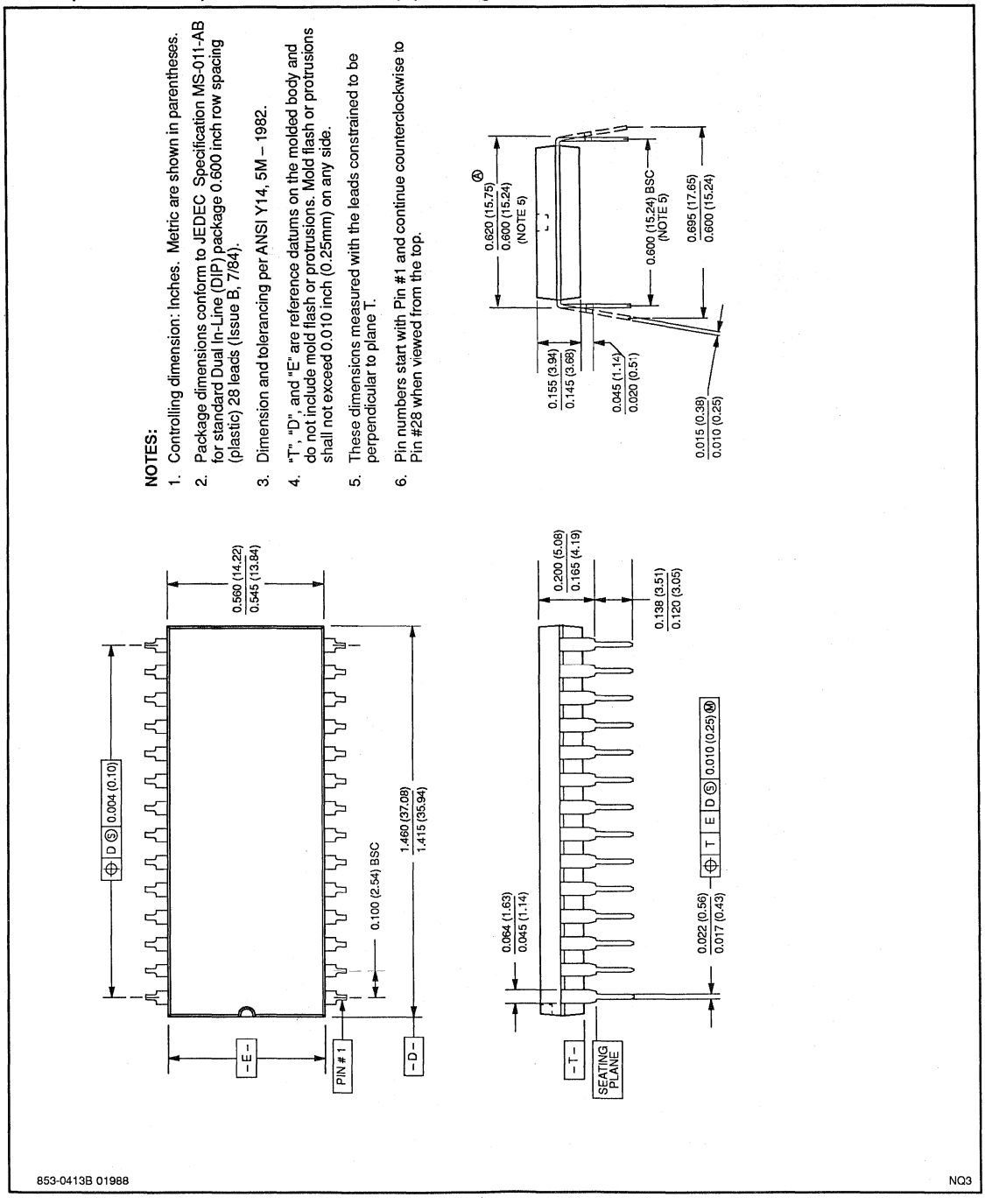
28-PIN (600 mils wide) Plastic Dual In-Line (N) Package



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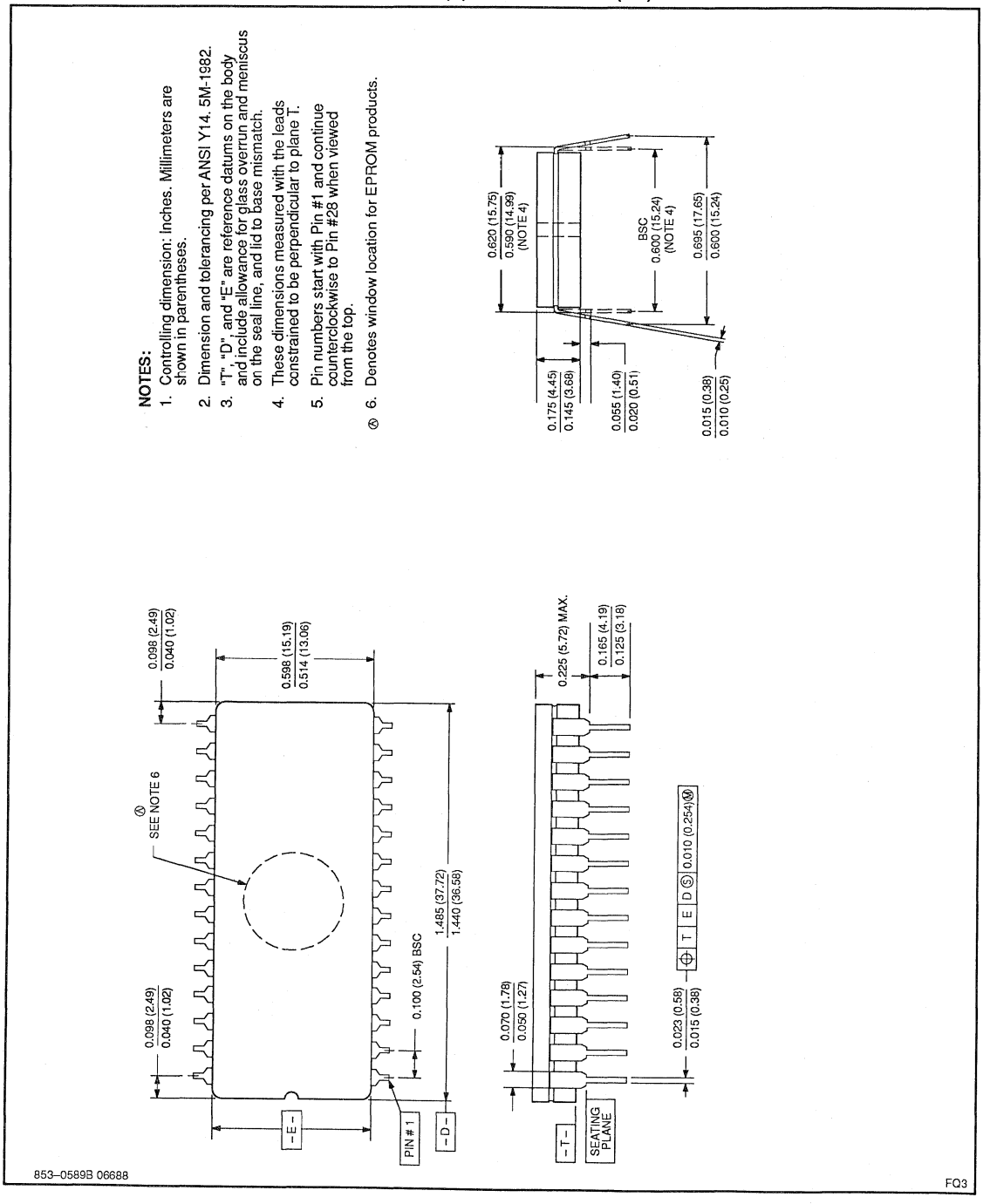

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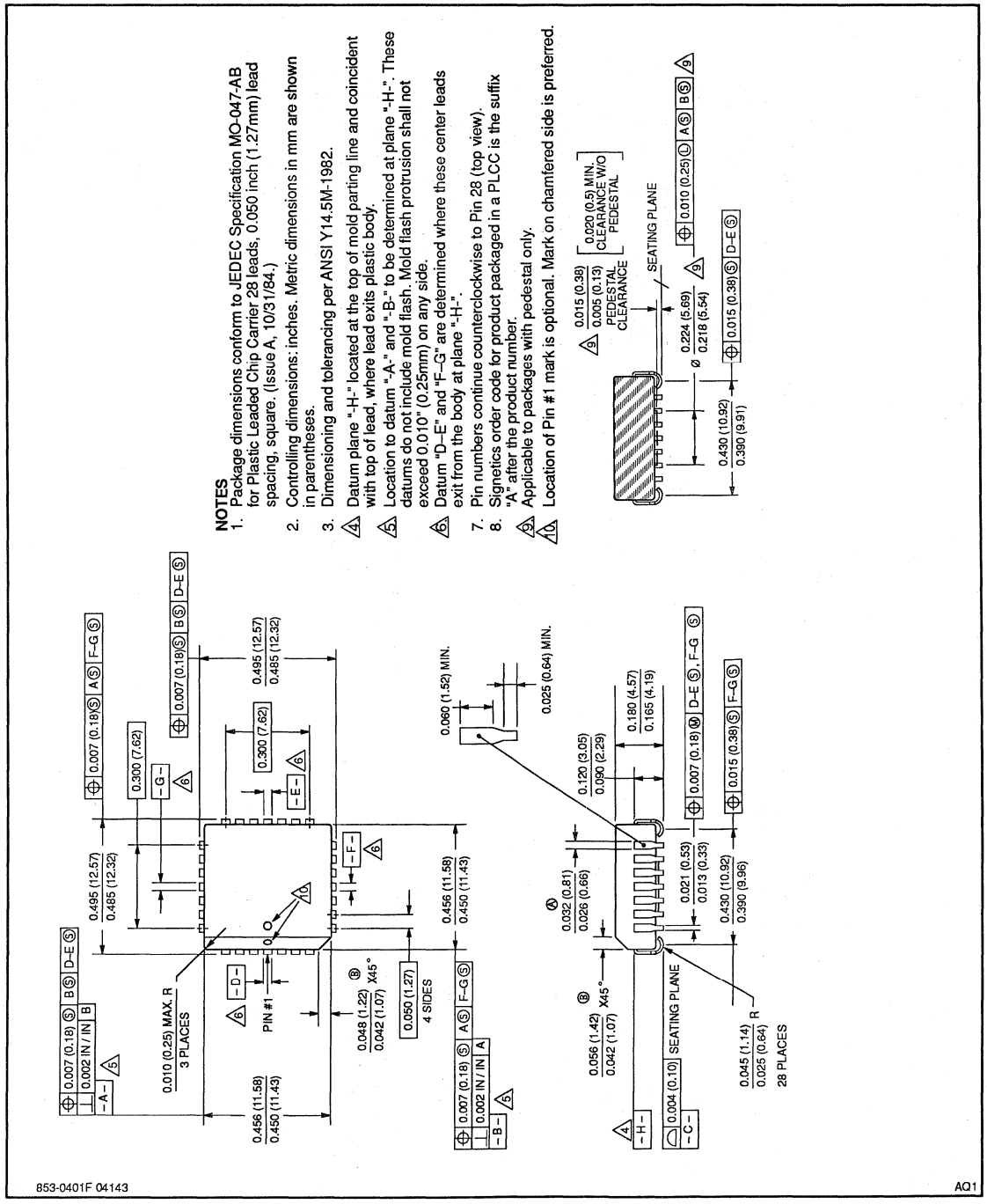

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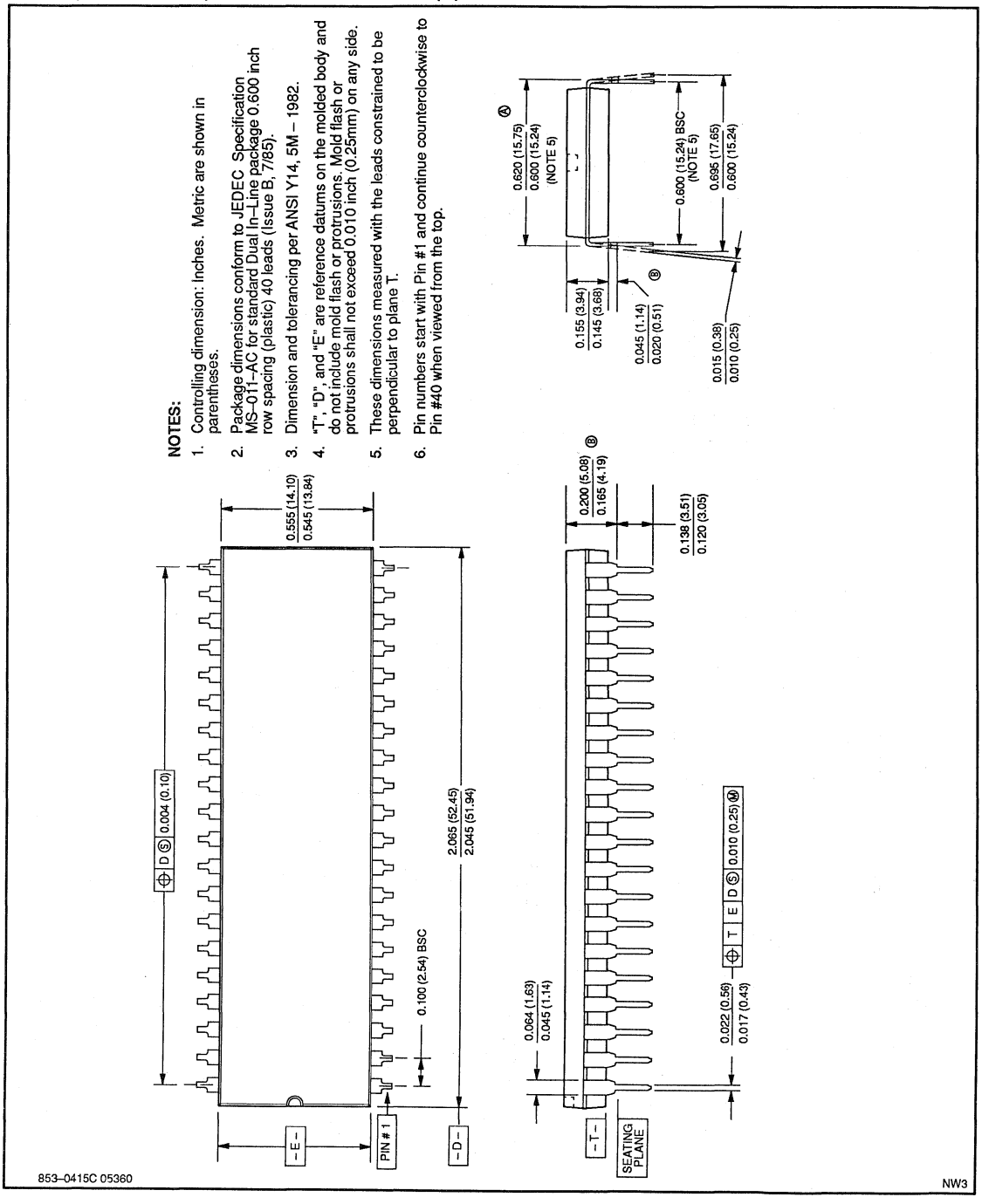

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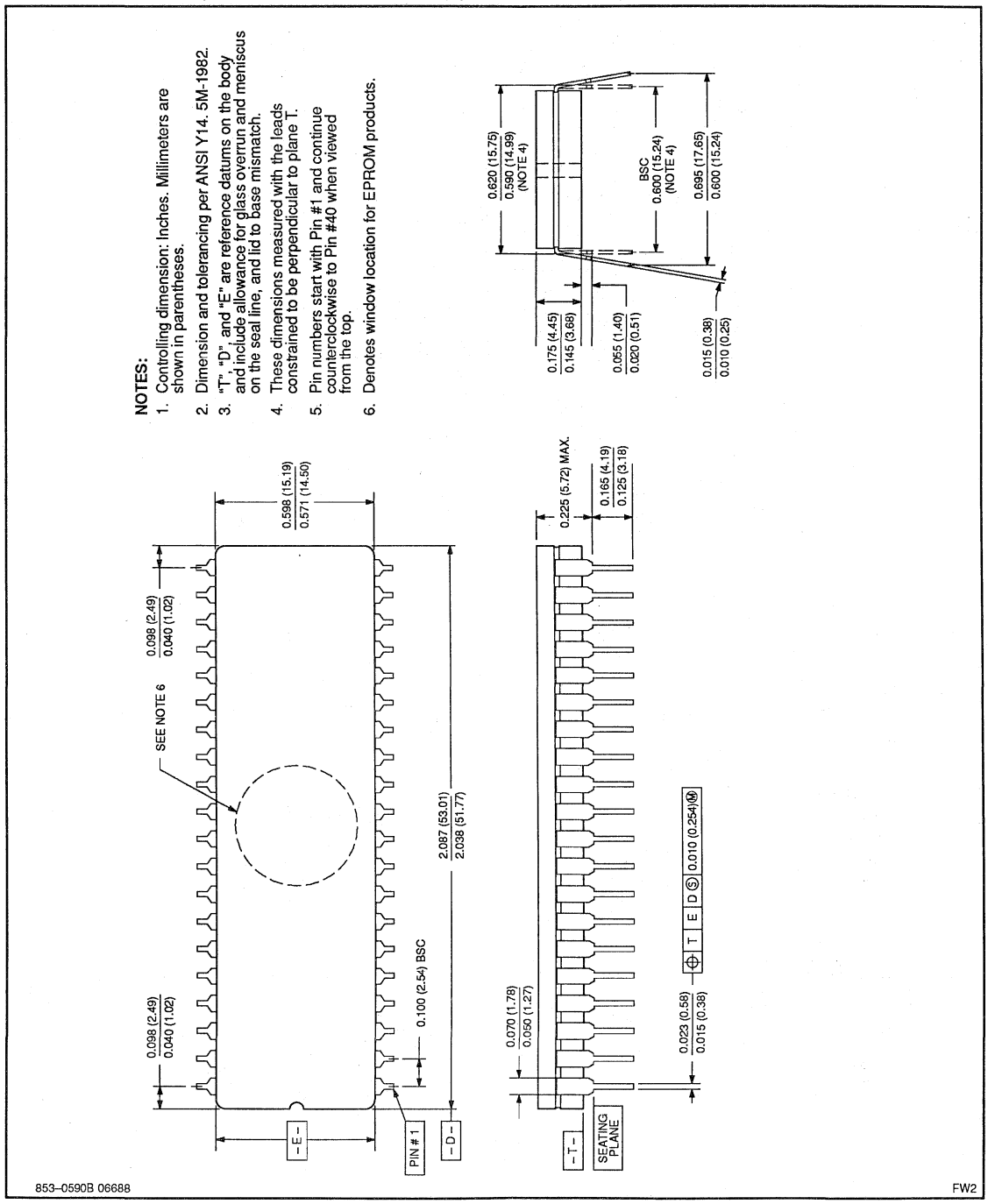

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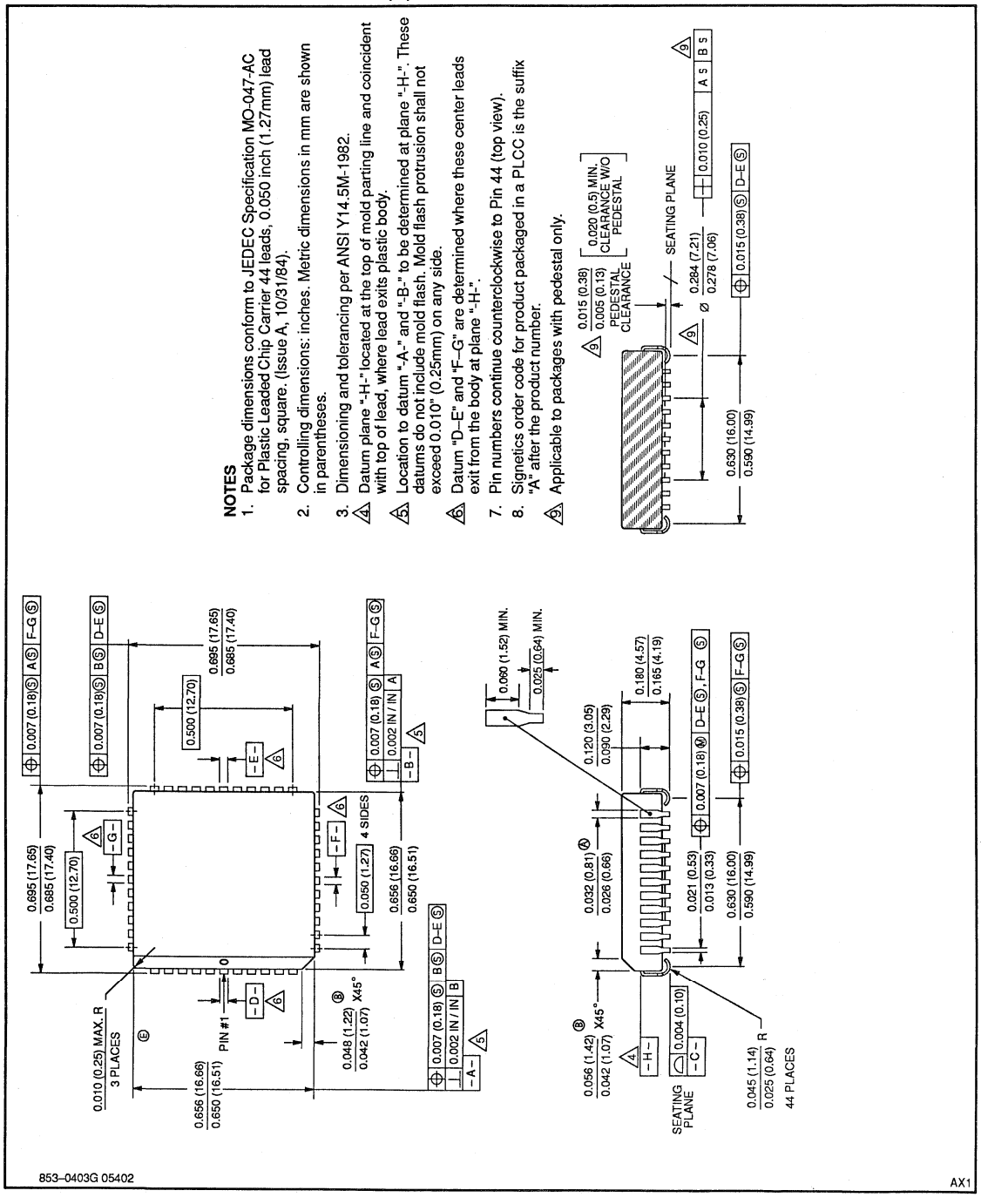

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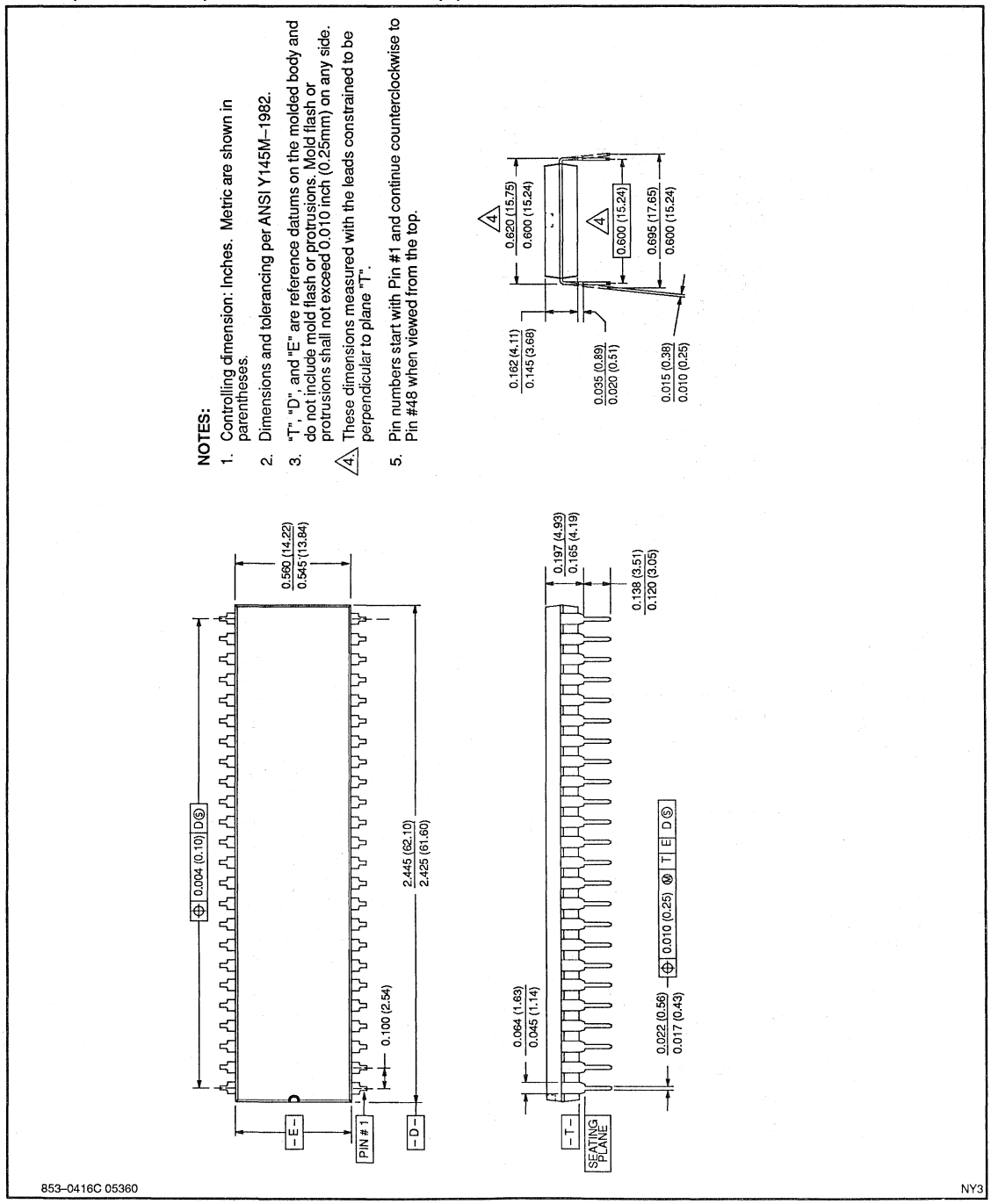

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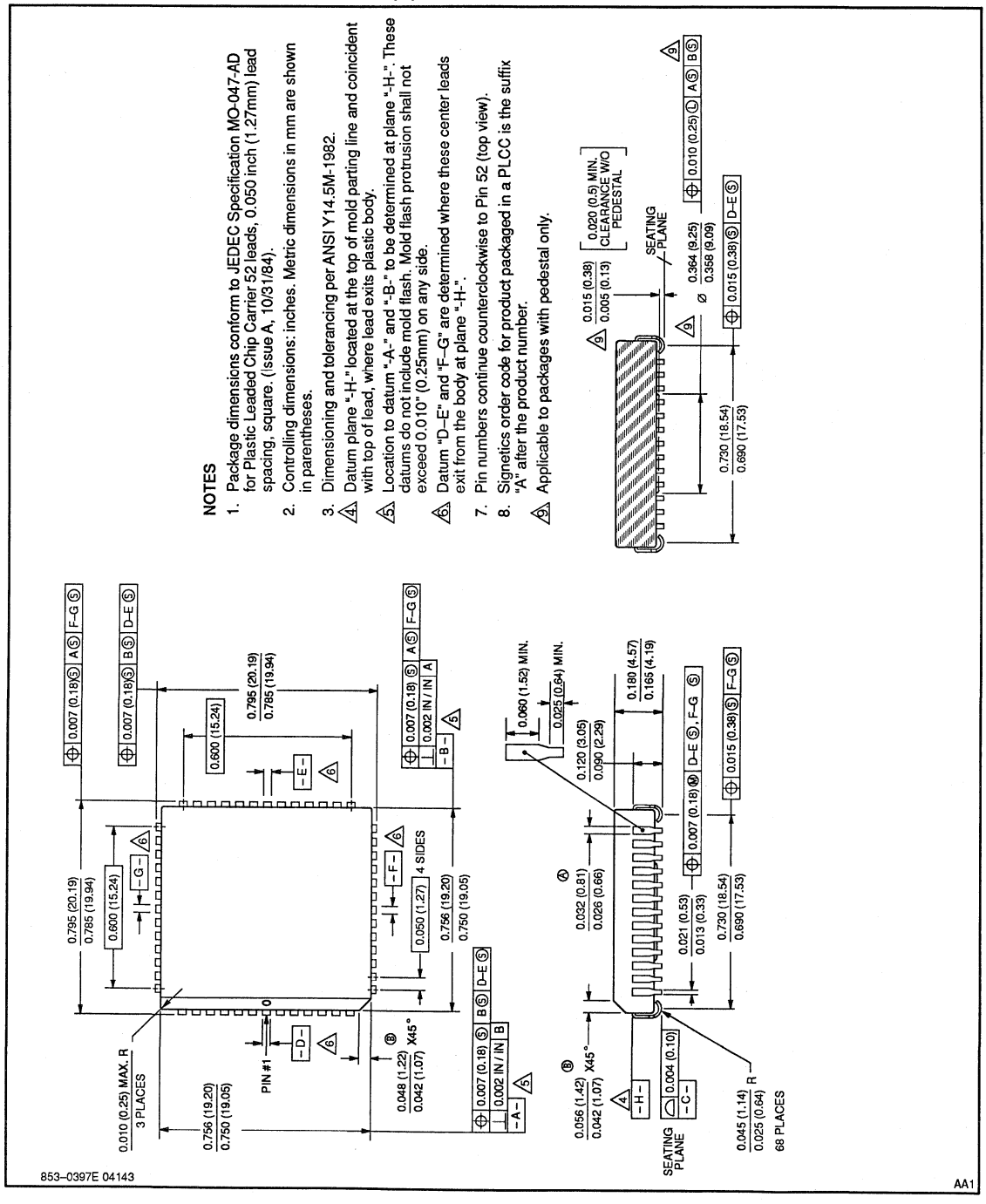

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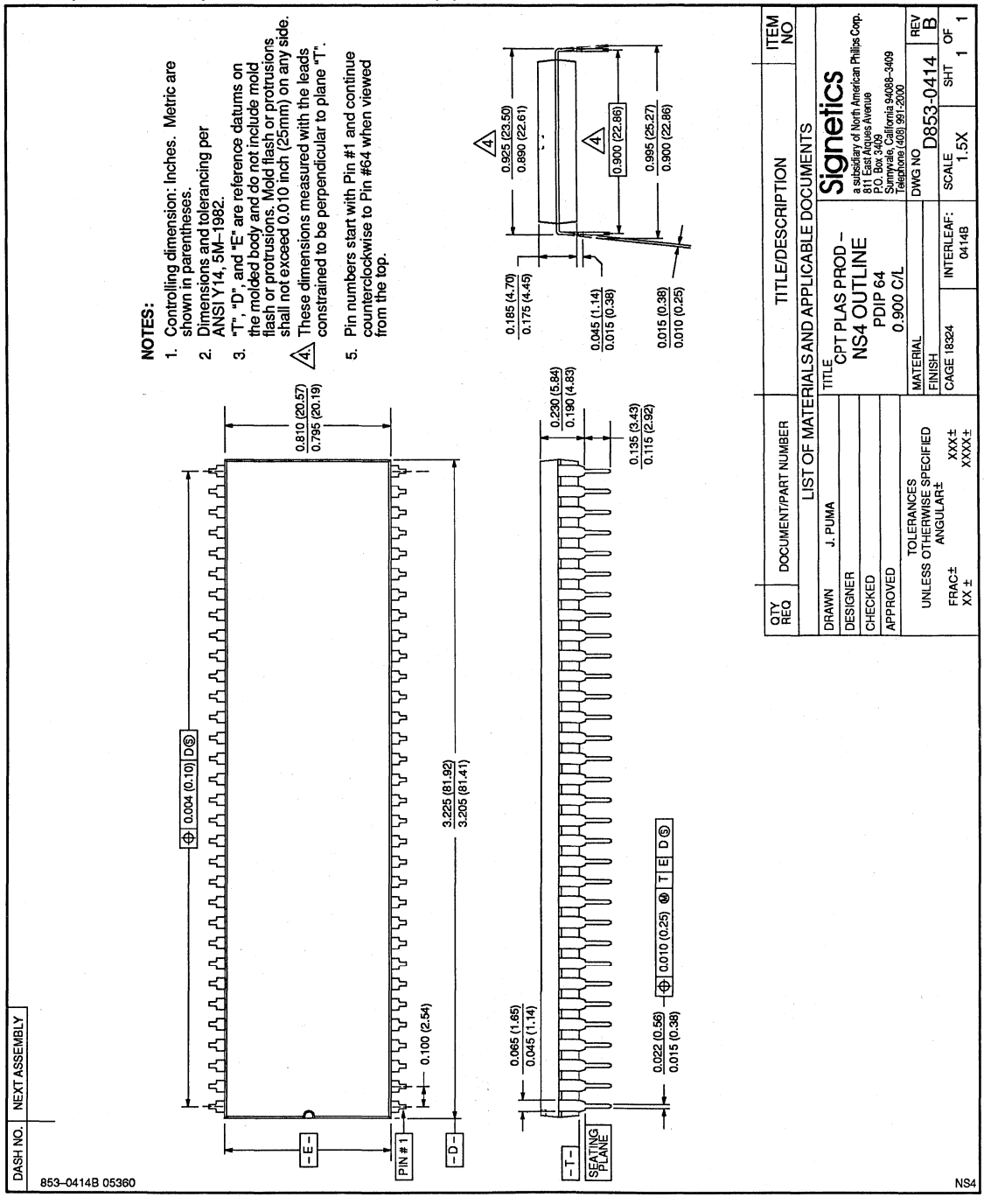

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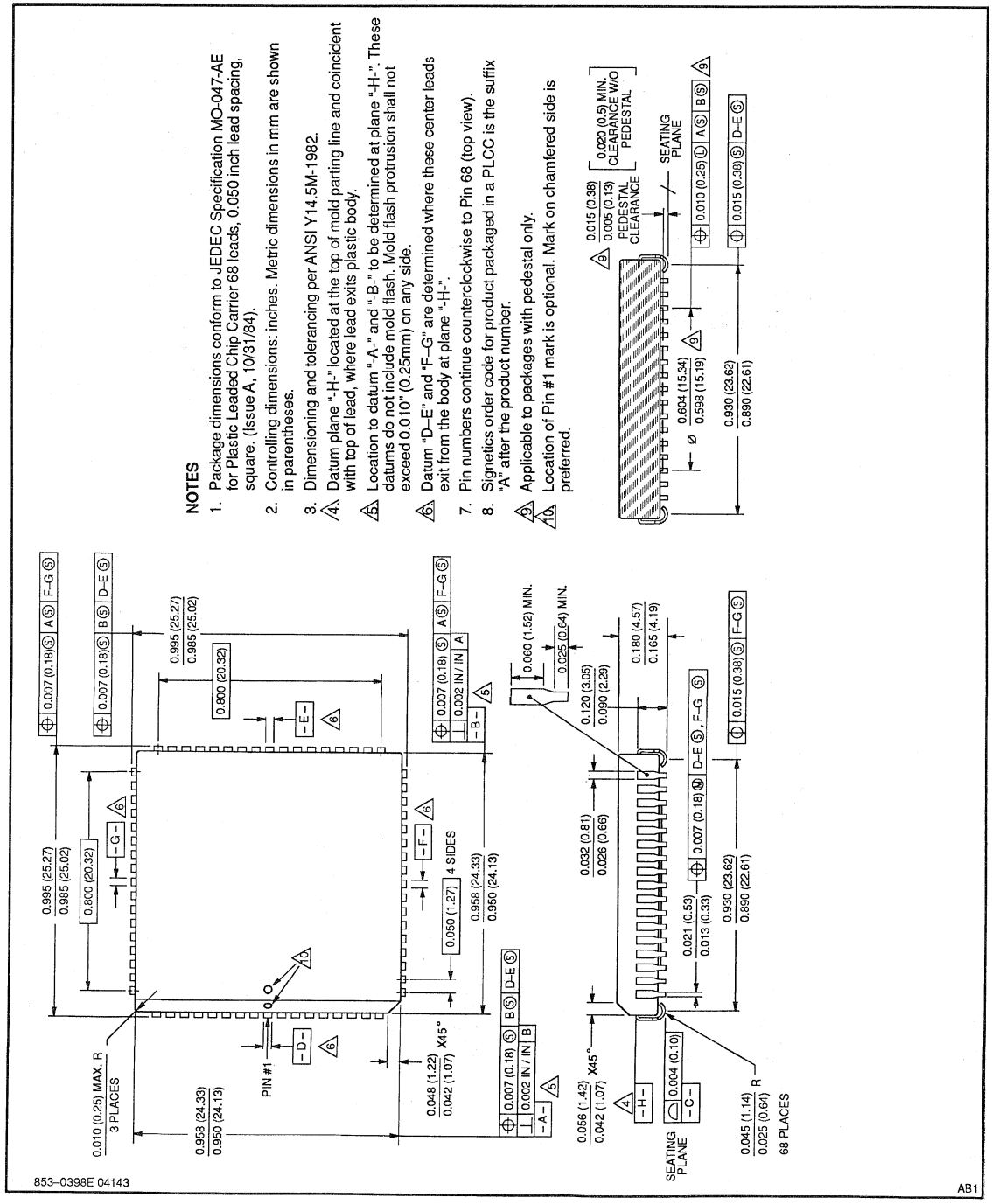

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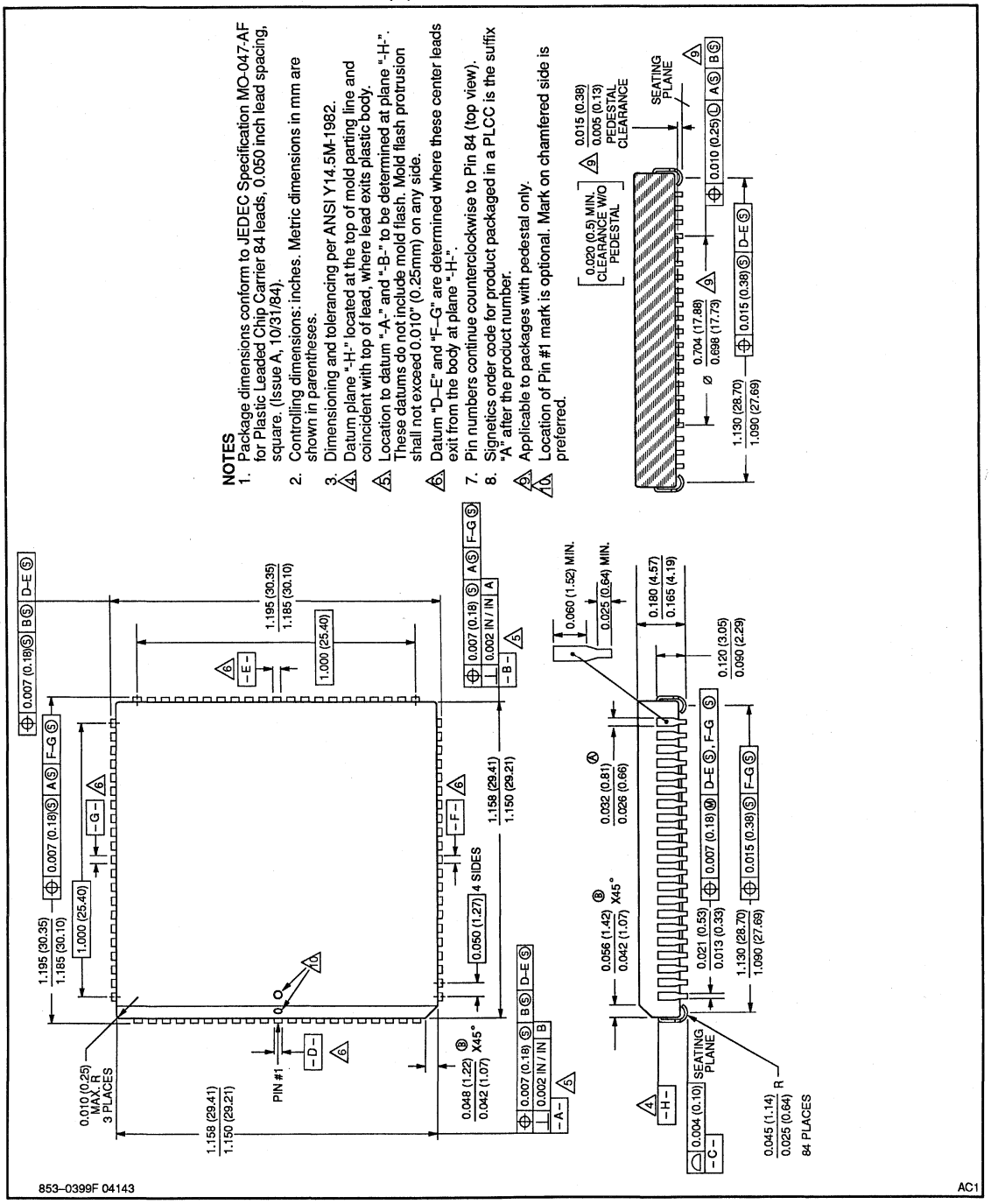

Section 6
Sales Offices

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Data handbook system — Appendix A

INTRODUCTION

Our data handbook system comprises more than 65 books with subjects including electronic components, subassemblies and magnetic products. The handbooks are classified into seven series:

INTEGRATED CIRCUITS;
DISCRETE SEMICONDUCTORS;
DISPLAY COMPONENTS;
PASSIVE COMPONENTS;
PROFESSIONAL COMPONENTS;
MAGNETIC PRODUCTS;
LIQUID CRYSTAL DISPLAYS.

Data handbooks contain all pertinent data available at the time of publication and each is revised and reissued regularly.

Loose data sheets are sent to subscribers to keep them up-to-date on additions or alterations made during the lifetime of a data handbook.

Catalogs are available for selected product ranges (some catalogs are also on floppy discs).

For more information about data handbooks, catalogs and subscriptions, contact one of the organizations listed on the back cover of this handbook. Product specialists are at your service and inquiries are answered promptly.

INTEGRATED CIRCUITS

IC01	Radio, Audio and Associated Systems Bipolar, MOS
IC02a/b	Video and Associated Systems Bipolar, MOS
IC03	ICs for Telecom Subscriber Sets, Cordless, Mobile and Cellular Telephones, Radio Pagers
IC04	HE4000B Logic Family CMOS
IC05	Advanced Low-power Schottky (ALS) Logic Series
IC06	High-speed CMOS; 74HC/HCT/HCU Logic Family
IC07	Advanced CMOS Logic (ACL)
IC08	10/100k ECL Logic/Memory/PLD
IC09	TTL Logic Series

INTEGRATED CIRCUITS (continued)

IC10	Memories MOS, TTL, ECL
IC11	Linear Products
IC12	I^2C-bus-compatible ICs
IC13	Programmable Logic Devices
IC14	8048-Based 8-Bit Microcontrollers
IC15	FAST TTL Logic Series
IC15 supplement: Additional FAST Data	
IC16	CMOS Integrated Circuits for Clocks and Watches
IC17	ICs for Telecom ISDN
IC18	Microprocessors and Peripherals
IC19	Data Communication Products
IC20	80C51-Based 8-Bit Microcontrollers
IC23	Advanced BiCMOS Interface Logic

DISCRETE SEMICONDUCTORS

SC01	Diodes
SC02	Power Diodes
SC03	Thyristors and Triacs
SC04	Small Signal Transistors
SC05	Low-frequency Power Transistors and Hybrid IC Power Modules
SC06	High-voltage and Switching Power Transistors
SC07	Small-signal Field-effect Transistors
SC08a	RF Power Bipolar Transistors
SC08b	RF Power MOS Transistors
SC09	RF Power Modules
SC10	Surface Mounted Semiconductors
SC12	Optocouplers
SC13	Power MOS Transistors
SC14	Wideband Transistors and Wideband Hybrid IC Modules
SC15	Microwave Transistors
SC17	Semiconductor Sensors

Data handbook system — Appendix A

DISPLAY COMPONENTS

DC01 Colour Display Components
Colour TV Picture Tubes and Assemblies
Color Monitor Tube Assemblies

DC02 Monochrome Monitor Tubes and Deflection Units

DC03 Television Tuners, Coaxial Aerial Input Assemblies

DC04 Loudspeakers

DC05 Flyback Transformers, Mains Transformers and General-purpose FXC Assemblies

PASSIVE COMPONENTS

PA01 Electrolytic Capacitors; Solid and Non-solid

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PA03 Potentiometers and Switches

PA04 Variable Capacitors

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PA06 Ceramic Capacitors

PA07 Piezoelectric Quartz Devices

PA08 Fixed Resistors

PA11 Quartz Oscillators

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PC01 High-power Klystrons and Accessories

PC02 Cathode-ray Tubes

PC03 Geiger-Muller Tubes

PC04 Photo Multipliers

PC05 Plumbicon Camera Tubes and Accessories

PC06 Circulators and Isolators

PC07 Vidicon and Newvicon Camera Tubes and Deflection Units

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PC09 Dry-reed Switches

PC11 Solid-state Image Sensors and Peripheral Integrated Circuits

PC12 Electron Multipliers

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MA01 Soft Ferrites

MA02 Permanent Magnet Materials

MA03 Piezoelectric Ceramics

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